Dual-Material-Gate Technique for Enhanced Transconductance and Breakdown Voltage of Trench Power MOSFETs

Raghvendra S. Saxena and M. Jagadesh Kumar, Senior Member, IEEE

Abstract—In this brief, we propose a new dual-material-gate trench power MOSFET that exhibits a significant improvement in its transconductance and breakdown voltage without any degradation in on-resistance. In the proposed structure, we have split the gate of a conventional trench MOSFET structure into two parts for work-function engineering. The two gates share the control of the inversion charge in the channel. By using 2-D numerical simulation, we have shown that by adjusting the lengths of the two gates to allow equal share of the inversion charge by them, we get the optimum device performance. By using N⁺ poly-Si as a lower gate material and P⁺ poly-Si as an upper gate material, approximately 44% improvement in peak transconductance and 20% improvement in breakdown voltage may be achieved in the new device compared to the conventional trench MOSFET.

Index Terms—Breakdown voltage, dual material gate, on-resistance, power MOSFET, trench gate.

I. INTRODUCTION

TRENCH-GATE technology [1]–[9] makes the MOSFET a more attractive device for low-to-medium voltage power applications as it provides reduced conduction power losses and lower forward voltage drop due to the absence of parasitic JFET region as compared to the planar power MOSFET. A trench-gate power MOSFET can be designed to have ultralow on-resistance [1]–[7] with high switching speed [2], [3] and can be fabricated easily using the standard Si process technology [7]–[9]. In addition, since high packing densities can be achieved using trench power MOSFETs [8], the on-resistance can be reduced significantly by the parallel conduction of a large number of unit cells in a given chip area. These features make the trench MOSFETs suitable for control switching, dc–dc converters, automotive electronics, microprocessor power supplies, etc.

In various power electronic applications, low on-resistance, higher drive current, low gate-to-drain capacitance, high transconductance, and high breakdown voltage are the desired features [10]–[13]. Designing a power MOSFET for a specific application is a compromise among these parameters because they are linked together by the technology and any attempt to improve one may adversely affect the other, making the device unsuitable in many other applications. The most desired performance specifications in all the applications are low on-resistance and high breakdown voltage. However, when we attempt to improve the breakdown voltage of a power MOSFET, the on-resistance increases drastically [13], [14]. Therefore, to overcome this difficulty, we propose a dual-material-gate trench (DMGT) MOSFET structure that shows improvement not only in breakdown characteristics but also in transconductance without any degradation in its on-resistance. A high transconductance makes the device suited for RF power amplification also [11], [15]. By using 2-D numerical simulation in ATLAS device simulator [16], we have analyzed the improved performance...
of the proposed DMGT MOSFET by comparing it with a conventional trench-gate MOSFET.

II. DEVICE STRUCTURE AND PROPOSED FABRICATION PROCEDURE

Fig. 1(a) shows the schematic top view of the proposed DMGT device, and Fig. 1(b) shows its cross-sectional view along the cut line AA'. As apparent from the figure, DMGT device contains two sections of its trench gate. The upper section (G1) has a higher work function gate material, whereas the lower section (G2) has the smaller work function material. The lengths of the two sections of the gate are denoted as L1 and L2 in Fig. 1. These sections are electrically connected by a metal. The lower section of the gate material is chosen to be N+ poly-Si (work function, $\phi_{G2} = 4.17$ eV), and the upper gate material is chosen to be P+ poly-Si (work function, $\phi_{G1} = 5.25$ eV). However, to analyze how the work function difference between the two gate materials ($\Delta \phi_G = \phi_{G1} - \phi_{G2}$) affects the device performance, we have also varied the value of $\phi_{G1}$ from ($\phi_{G2} + 0.25$ eV) to ($\phi_{G2} + 1.25$ eV) in our simulations.

The fabrication process of the DMGT structure is shown in Fig. 2. First, by using some initial processing steps of a conventional trench-gate MOSFET fabrication [7]–[9], we create a structure, as shown in Fig. 2(a), consisting of the N+ substrate ($N_D = 1 \times 10^{19}$ cm$^{-3}$) as the drain, a 0.1-μm-thick N+ source ($N_D = 1 \times 10^{19}$ cm$^{-3}$) on the top side, a 2.7-μm-thick N-type drift region ($N_D = 1 \times 10^{16}$ cm$^{-3}$), and a 0.7-μm-thick P-type body region ($N_A = 5 \times 10^{17}$ cm$^{-3}$). It also has a 1.2-μm-wide and 1.2-μm-deep trench with a 50-nm-thick gate oxide layer grown inside the trench. In the next step, N+ poly-Si is done and CMP is carried out to get the structure shown in Fig. 2(b). A selective etching of the upper part of the poly-Si, followed by the oxide etching, forms the N+ poly lower gate electrode as shown in Fig. 2(c). Again, by growing a 50-nm-thick gate oxide followed by P+ poly deposition and CMP, we realize the structure shown in Fig. 2(d). Finally, to take the gate contact, we make a contact hole in the middle of the main trench as shown in Fig. 2(e), having a depth just enough to reach the lower gate material. It is then filled with a metal using standard metallization process. The final structure is shown in Fig. 2(f).

For device simulation, we have created the DMGT structure in ATLAS and compared it with the conventional device.
having the same parameters as mentioned earlier except that the conventional device has only one gate material of N⁺ poly-Si.

III. SIMULATION RESULTS AND DISCUSSION

The performance of DMGT device depends on the work function difference $\Delta \phi_G$ of the two gates and their lengths $L_1$ and $L_2$. We have first simulated the DMGT device by varying $\phi_{G1}$, keeping $\phi_{G2}$ constant at 4.17 eV. For this analysis, we kept $L_1$ fixed at 0.3 $\mu$m. We have also analyzed the effect of gate length variation of the DMGT device by varying $L_1$ but keeping the total gate length constant ($L_1 + L_2 = L$). With this analysis, we found the optimum gate length $L_1$ to be 0.3 $\mu$m for achieving the best performance. Then, we compared the optimized DMGT device with the conventional device for current–voltage characteristics, transconductance, on-resistance, and breakdown voltage.

The difference in the work function of the two gates causes a change in the surface potential as shown in Fig. 3(a). It is clear from the figure that as $\Delta \phi_G$ increases, the step in the surface potential profile also increases, modifying the channel electric field as shown in Fig. 3(b). The channel electric field for different values of $L_1$ is shown in Fig. 3(c) for a fixed $\Delta \phi_G$ (1.08 eV, poly-Si gate case) in comparison with the conventional device. In addition to the peaks at the body-source junction and at the body-drift junction, the channel electric field has one more peak in the DMGT device at the location where gate $G_1$ ends, whereas in a conventional device, the electric field increases gradually in the channel. This modified electric field profile results in a higher acceleration and higher velocity of the charge carriers coming from the source, as shown in Fig. 3(d), in the DMGT device ($\Delta \phi_G = 1.08$ eV). Hence, a higher transconductance is expected in the DMGT device. The additional peak in the channel electric field also provides screening to the increased drain voltage, making the DMGT device better from the hot-carrier suppression point of view. The value of this peak has almost linear dependence on $L_1$, as shown in Fig. 4.

If the gate length is fixed at $L = L_1 + L_2$, for $L_1 = 0$, the device behaves like a conventional trench-gate MOSFET with N⁺ poly gate length $L = L_2$, and for $L_2 = 0$, it again becomes a conventional device with P⁺ poly gate length $L = L_1$. Therefore, the best advantage of the dual material gate is expected to be in between these two extremes.

Because of the increase in peak channel electric field with the increasing $L_1$ (as shown in Fig. 4), the carrier transport efficiency from the source to the channel is improved. However, beyond a certain value of $L_1$, this improvement reduces due to the lowering of the second peak of the electric field at the body-drift junction. As a result, compared to the conventional single-gate case (having only N⁺ poly gate), the drive current

Fig. 3. (a) Surface potential profile along the channel for different work function differences between $G_1$ and $G_2$. (b) Electric field profile along the channel for different work function differences between $G_1$ and $G_2$. (c) Electric field profile for the conventional and DMGT devices with gate length $L_1 = 0.3$ $\mu$m and $0.5$ $\mu$m while keeping the total channel length $L_1 + L_2$ constant at 1.1 $\mu$m. (d) The corresponding electron velocity in the channel for the conventional and the DMGT devices for different values of $L_1$. 

Authorized licensed use limited to: INDIAN INSTITUTE OF TECHNOLOGY DELHI. Downloaded on July 5, 2009 at 07:50 from IEEE Xplore. Restrictions apply.
Fig. 4. Peak value of the channel electric field in DMGT device as function of gate1 length ($L_1$).

At higher drain voltages, the electric field peak near the end of the trench is responsible for the breakdown in both conventional and DMGT devices and may be considered as the main peak of the electric field. The additional electric field peak in the channel of the DMGT device results in the reduction of the main peak as compared to the conventional device, and therefore, we observe an improvement in the breakdown voltage. Furthermore, as $L_1$ increases, the peak channel electric field also increases (as shown in Fig. 4), giving a higher breakdown voltage until $L_1$ approaches the value of $L$ (when it reduces to a single-gate device), because at that situation, the additional peak merges with the main peak of the electric field to make it further high. The breakdown behavior of the DMGT device, for various values of $L_1$, along with the conventional device (having only one N$^+$ poly gate), is shown in Fig. 5(b), indicating not only a significant increase in the breakdown voltage in the DMGT device but also a monotonic increase in the breakdown voltage with increasing $L_1$ (of course, until $L_1 < L$), as expected.

The influence of the variation in $L_1$ is summarized in Fig. 6, where various performance parameters such as threshold voltage, transconductance, on-resistance, and breakdown voltage are plotted as functions of $L_1$. Fig. 6(a) shows the increase in the threshold voltage in the DMGT device that can be taken care of in the design by selecting appropriate body doping or gate oxide thickness. The on-resistance and the transconductance of the device, evaluated at $V_{DS} = 1.0$ V, are shown as functions of $L_1$ in Fig. 6(b) and (c), respectively, indicating that the best values are achieved at $L_1 = 0.3$ μm. The breakdown voltage variation with $L_1$ is shown in Fig. 6(d) that indicates a monotonic improvement in the breakdown voltage with increasing $L_1$, as anticipated earlier.

From the earlier discussion, it may be inferred that the best performance is achieved when $L_1$ is kept at about half of the total length of the p-region (≈0.3 μm), giving equal control of the inversion charge in the p-region to both the gates $G_1$ and $G_2$ as shown in Fig. 1. When we compare the performance of the optimized DMGT device ($L_1 = 0.3$ μm) with the conventional device, we find 44% improvement in peak transconductance, 20% improvement in breakdown voltage, 6% improvement in drive current, and 0.5% improvement in on-resistance. Usually, an improvement in breakdown voltage adversely affects the on-resistance [11]–[13]. However, in the proposed device, although there is a 20% improvement in the breakdown voltage, it does not affect the on-resistance.

IV. CONCLUSION

By using 2-D numerical simulations, we have demonstrated that in a trench-gate power MOSFET, the sectioning of the gate into two parts gives the flexibility of gate work-function engineering. By using P$^+$ poly in upper section and N$^+$ poly in deeper section of the gate, we have shown a significant improvement in the device performance. The optimized performance is achieved when both the gates have equal control of the inversion charge of the channel. We obtained 20% improvement in the breakdown voltage and 44% improvement in the peak transconductance in the optimized DMGT device over the
conventional device. An additional electric field peak obtained in the channel of the DMGT device also makes it better from hot-carrier suppression point of view.

REFERENCES


Fig. 6. Effect of gate1 length (L1) variation in DMGT device on (a) threshold voltage, (b) on-resistance, (c) transconductance, and (d) breakdown voltage with constant total channel length (L1 + L2 = 1.1 μm).
Raghvendra S. Saxena received the B.E. degree in electronics and communication engineering from G. B. Pant Engineering College, Pauri Garhwal, India, in 1997, and the M.Tech. degree in microelectronics from the Indian Institute of Technology, Bombay, India, in 2003. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, Indian Institute of Technology, New Delhi, India.

Since 1998, he has been a Scientist with the Solid State Physics Laboratory, Delhi, India, working on the design, modeling, and characterization of infrared detectors and their readout circuits. His current fields of interest are power electronic devices, nanoscale VLSI devices, and infrared detectors. He has published about ten papers in various journals and conference proceedings.

Mr. Saxena is a member of the Institution of Electronics and Telecommunication Engineers, India.

M. Jagadesh Kumar (M’95–SM’99) was born in Mamidala, Andhra Pradesh, India. He received the M.S. and Ph.D. degrees in electrical engineering from the Indian Institute of Technology, Madras, India.

From 1991 to 1994, he was with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada, where he performed postdoctoral research on the modeling and processing of high-speed bipolar transistors. While with the University of Waterloo, he also did a research on amorphous-silicon TFTs. From July 1994 to December 1995, he was initially with the Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, India, and then, he joined the Department of Electrical Engineering, Indian Institute of Technology, New Delhi, India, where he became an Associate Professor in July 1997 and a Full Professor in January 2005. His research interests include nanoelectronic devices, modeling and simulation for nanoscale applications, integrated-circuit technology, and power semiconductor devices. He has authored three book chapters and more than 125 publications in refereed journals and conference proceedings. His teaching has often been rated as outstanding by the Faculty Appraisal Committee of IIT Delhi.

Dr. Kumar is a fellow of the Indian National Academy of Engineering and the Institution of Electronics and Telecommunication Engineers (IETE), India. He is an IEEE Distinguished Lecturer of the IEEE Electron Devices Society (EDS). He is also a member of the EDS Publications Committee and EDS Educational Activities Committee. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES and Editor-in-Chief of IETE Technical Review. He is also on the Editorial Board of the Journal of Computational Electronics, Recent Patents on Nanotechnology, Recent Patents on Electrical Engineering, Journal of Low Power Electronics, and Journal of Nanoscience and Nanotechnology. He is the Lead Guest Editor of the joint special issue of IEEE TRANSACTIONS ON ELECTRON DEVICES and IEEE TRANSACTIONS ON NANOTECHNOLOGY on “Nanowire Transistors: Modeling, Device Design, and Technology” (November 2008 issue). He has extensively reviewed for different international journals. He was the recipient of the 29th IETE Ram LalWadhwa GoldMedal for his distinguished contribution in the field of semiconductor device design and modeling and the 2008 IBM Faculty Award. He was the first recipient of ISA-VSI TechnoMentor Award given by the India Semiconductor Association in recognition of a distinguished Indian academician or researcher for playing a significant role as a Mentor and Researcher.