The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs

M. Jagadesh Kumar, Senior Member, IEEE, and M. Siva

Abstract—The ground plane (GP) concept is one of the techniques used to reduce the drain-induced barrier lowering (DIBL) in nanoscale MOSFETs and is effective only when the distance between the GP and the drain is small as compared with the channel length. Therefore, if the GP is placed in the substrate (GPS), the buried oxide (BOX) thickness should be kept as small as possible which, however, results in an increased subthreshold slope. As a result, for sub-100-nm channel lengths, it is not possible to achieve both reduced DIBL and steep subthreshold slope using GPS. In this brief, a new device structure with the GP BOX is proposed to overcome the aforementioned shortcomings so that a reduced DIBL as well as an improved subthreshold slope can be obtained. Two-dimensional simulation is used to understand the efficacy of the proposed method.

Index Terms—Drain-induced barrier lowering (DIBL), ground plane (GP), short-channel effects (SCEs), silicon-on-insulator (SOI) MOSFET, subthreshold slope, 2-D simulation.

I. INTRODUCTION

SILICON-ON-INSULATOR (SOI) technology employs a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (hundreds of nanometers) layer of silicon oxide. In fully depleted SOI (FD SOI) MOSFETs, the silicon film thickness is smaller than the maximum depletion width and exhibits the most attractive properties such as low electric fields, high transconductance, excellent short-channel behavior, and quasi-ideal subthreshold slope characteristics. However, as the device dimensions are scaled down into sub-100-nm regime, the performance of the FD SOI MOSFET also deteriorates due to short-channel effects. In order to realize the FD SOI MOSFETs under sub-100-nm regime, two device issues are important. One is to have a lower drain-induced barrier lowering (DIBL), and the other is to maintain a steep subthreshold slope. In the case of long channel SOI MOSFET, subthreshold slope can be improved by increasing the buried oxide (BOX) thickness [1]. In a shorter gate length SOI MOSFET, on the other hand, a thicker BOX causes a larger DIBL due to the electric field penetration through the BOX. As a result, the subthreshold slope deteriorates with an increase in the BOX thickness. The ground plane (GP) concept is one of the techniques used to reduce the DIBL effect [2]–[4], and it is effective only when the distance between the GP and the drain is small as compared with the channel length. Therefore, if we place the GP in the substrate (GPS), we should keep the BOX thickness as small as possible, but it results in an increased subthreshold slope. Therefore, for sub-100-nm channel lengths, it is not possible to achieve both reduced DIBL effect and steep subthreshold slope using GPS [5].

In this brief, we propose a new device structure in which the GP is introduced in the BOX (GPB) to overcome the aforementioned shortcomings. We show that the GPB can be created by using the SOI with Active Substrate (SOIAS) technology [6], [7]. In the proposed device structure, as the GP is placed in the BOX, it acts as a sink to the drain electric field, leading to a reduced DIBL effect. We also demonstrate that the BOX thickness can be increased in the proposed structure to decrease the BOX capacitance, resulting in a steeper subthreshold slope. Two-dimensional simulation is used to verify the efficacy of the proposed method.

II. DEVICE STRUCTURE AND PROCESSING

Steps to Create the GPB

The GPS can be created by implanting boron through the silicon film, but it is difficult to create a GPB itself due to the alignment problem between the gate and the GPs. Yang et al. [6], [7] have proposed a new device structure in which an amorphous silicon is introduced in the BOX. By using this structure, we can introduce the GPB using the same procedure as used to create the GPS.

We have compared three different structures: 1) conventional FD SOI MOSFET; 2) FD SOI MOSFET with GPS; and 3) FD SOI MOSFET with GPB, as shown in Fig. 1. The device parameters used in our simulation are given in Table I. In the conventional FD SOI MOSFET and GPB cases, BOX thickness is taken as 200 nm. For the case of the GPS, to effectively control the DIBL effect, the BOX thickness should be as small as possible, and therefore, it is taken to be 10 nm [3]. To have a similar control on DIBL, in the case of the GPB structure, the GP is located at 10 nm from the top of 200-nm-thick BOX.

The GPB structure can be created by using the SOIAS technology [6], [7]. The SOIAS substrate is a multilayered blanket film stack consisting of silicon wafer, insulating oxide, intrinsic polysilicon, back-gate oxide, and silicon film. Fig. 2 shows the fabrication process for the SOIAS preparation by the bonded-SIMOX approach. First step is the implantation of high-dose oxygen ions into the silicon wafer, which is followed by the high-temperature annealing step to form a BOX layer [Fig. 2(a) and (b)]. The oxide layer is thermally grown on top of the single crystalline silicon followed by the amorphous silicon deposition [Fig. 2(c) and (d)]. The device wafer is flipped and bonded to the oxidized handle wafer [Fig. 2(e) and (f)]. The bulk of the SIMOX wafer is removed by the chemical and mechanical polishing and the wet chemical etching. The

Manuscript received October 30, 2007; revised March 18, 2008. The review of this brief was arranged by Editor C. McAndrew.

The authors are with the Department of Electrical Engineering, Indian Institute of Technology, New Delhi 110 016, India (e-mail: mamidala@iitd.ac.in). Digital Object Identifier 10.1109/TED.2008.922859
Fig. 1. Cross section of different structures used in the simulation: (a) conventional FD SOI MOSFET, (b) FD SOI MOSFET with GPS, and (c) FD SOI MOSFET with GPB.

TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate oxide thickness</td>
<td>2 nm</td>
</tr>
<tr>
<td>SOI thickness</td>
<td>5 nm</td>
</tr>
<tr>
<td>Polysilicon thickness</td>
<td>5 nm</td>
</tr>
<tr>
<td>Source/drain doping</td>
<td>$10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Body doping</td>
<td>$10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Substrate doping</td>
<td>$10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Work function</td>
<td>4.6 eV</td>
</tr>
</tbody>
</table>

BOX of the SIMOX serves as a perfect etch stop [Fig. 2(g)]. Therefore, the silicon film thickness uniformity of the original SIMOX wafer is directly transferred to the SOIAS wafer. The BOX can be removed by conventional wet etching. The final silicon film thickness is achieved by thermal oxidation thinning. Fig. 2(h) shows the final bonded-SIMOX SOIAS wafer.

The device fabrication on SOIAS follows the conventional CMOS SOI process with two additional steps. The GPs can be created by ion implantation of boron through the silicon film in two masking steps, resulting in the formation of p$^+$ islands insulated by intrinsic polysilicon after thermal anneal [Fig. 2(i)]. As the GP can be formed after the gate-electrode etching, it is a self-aligned process. The GPs are placed under the source and drain regions in order to control the electric field around the junction regions.

III. TWO-DIMENSIONAL SIMULATION RESULTS

We have investigated the advantages of GPB over conventional and GPS structures using the physically based numerical device simulator ATLAS [8]. In our simulations, we used appropriate physical models, including the Selberherr’s impact ionization model [8]. Since midgap gate materials are suitable for high-performance FD SOI MOSFETs [9], [10], the gate work function is taken as 4.6 eV for all cases. Both the GPs and the substrate are kept at zero potential in our simulations.

The potential contours of the three structures at $V_{DS} = 1\, \text{V}$ are shown in Fig. 3. It can be observed that in the case of the conventional FD SOI MOSFET, the electric field lines from the drain side approach the source through the BOX, as shown in Fig. 3(a). However, in the case of the GPS [Fig. 3(b)] and the GPB [Fig. 3(c)], the electric field line coupling is minimized, indicating its impact on reducing the DIBL.

In the case of a FD SOI MOSFET, the subthreshold slope is given by

$$S = (1 + \alpha) \frac{kT}{q} \ell n(10) \tag{1}$$

where $kT/q$ is the thermal voltage, and $\alpha$ is the ratio of the capacitance between channel and substrate ground to the gate capacitance. From (1), it is clear that if we want a steeper subthreshold slope, we need a smaller BOX capacitance which can be obtained only by increasing the BOX thickness. However, an increase in BOX thickness will adversely affect the DIBL.

To estimate the DIBL, we have first calculated the threshold voltage as the gate voltage at which the drain current $I_D = 6(W/L) \, \text{nA}$, where the width $W$ of the device is taken as 1 $\mu\text{m}$. The DIBL effect is calculated as

$$\text{DIBL} = \frac{V_{th}|_{V_{DS}=0.05 \, \text{V}} - V_{th}|_{V_{DS}=1.0 \, \text{V}}}{V_{DS}(= 1.0 \, \text{V}) - V_{DS}(= 0.05 \, \text{V})}. \tag{2}$$

Fig. 4 shows the DIBL effect versus the channel length. It is clearly observed that the DIBL effect is less with the GP concept as compared with the conventional FD SOI MOSFET.
The DIBL of the GPS and GPB structures is identical because the BOX thickness is 10 nm for the GPS structure and the GP is kept 10 nm below from the top of the 200-nm BOX for the GPB structure.

Fig. 5 shows the subthreshold slope for all the three structures. From this figure, we can observe two things. First, the subthreshold slope is small for the conventional and GPB cases (BOX thickness = 200 nm) as compared with the GPS (BOX thickness = 10 nm) because of their larger BOX thickness. Therefore, the GPB structure can provide both reduced DIBL effect and better subthreshold slope for shorter channel lengths. This will have an impact on the OFF-state leakage current (calculated as the drain current at $V_{GS} = 0$ V and $V_{DS} = 1$ V), as shown in Fig. 6.

It is evident from Fig. 6 that for the same DIBL effect (GP is at a distance of 10 nm in both the GPS and GPB structures), both the GPS and GPB structures have lower OFF-state leakage current compared with the conventional FD SOI MOSFET. In Fig. 6, the slight difference in the OFF-state leakage current of the GPS and GPB structures is due to the higher threshold voltage.
the future scaling of MOSFETs in sub-100-nm applications. The FD SOI MOSFET with the GPB is a promising candidate for MOSFET and the FD SOI MOSFET with the GPS. Thus, the subthreshold slope compared with the conventional FD SOI structures, as shown in Fig. 8.

leakage current as compared with the conventional and GPS from the top of BOX), the GPB structure has lower standby and drain junctions only in the case of GPB structure (10 nm structure), it is observed that as the GP is nearer to the source GPS structure is made 200 nm (just as in the case of the GPB to the capacitive coupling. However, if the BOX thickness of the voltage of the GPS structure, as shown in Fig. 7, which is due to the capacitive coupling. However, if the BOX thickness of the GPS structure is made 200 nm (just as in the case of the GPB structure), it is observed that as the GP is nearer to the source and drain junctions only in the case of GPB structure (10 nm from the top of BOX), the GPB structure has lower standby leakage current as compared with the conventional and GPS structures, as shown in Fig. 8.

Fig. 7. Threshold voltage versus channel length for $V_{DS} = 1$ V.

Fig. 8. Variation of leakage current with channel length for the same BOX thickness of 200 nm.

IV. CONCLUSION

In this brief, we proposed a new device structure in which the GP is introduced in the BOX. By using a 2-D device simulation, it is shown that the proposed structure minimizes both the DIBL and the OFF-state leakage current while improving the subthreshold slope compared with the conventional FD SOI MOSFET and the FD SOI MOSFET with the GPS. Thus, the FD SOI MOSFET with the GPB is a promising candidate for the future scaling of MOSFETs in sub-100-nm applications.

REFERENCES


M. Jagadesh Kumar (M’95–SM’99) was born in Mamidala, Andhra Pradesh, India. He received the M.S. and Ph.D. degrees in electrical engineering from the Indian Institute of Technology (IIT), Madras, India. From 1991 to 1994, he performed a postdoctoral research on modeling and processing of high-speed bipolar transistors with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada.

While with the University of Waterloo, he also did research on amorphous–silicon thin-film transistors. From July 1994 to December 1995, he was initially with the Department of Electronics and Electrical Communication Engineering, IIT, Khargpur, India. He is currently with the Department of Electrical Engineering, IIT, New Delhi, India, where he became an Associate Professor in July 1997 and a Full Professor in January 2005. His teaching has often been rated outstanding by the Faculty Appraisal Committee, IIT Delhi. His research interests include nanoelectronic devices, modeling and simulation for nanoscale applications, integrated-circuit technology, and power semiconductor devices. He has published extensively in the aforementioned areas with three book chapters and more than 120 publications in refereed journals and conferences.

Dr. Kumar is a Fellow of the Indian National Academy of Engineering and the Institution of Electronics and Telecommunication Engineers (IETE), India. He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES. He is also on the editorial board of Journal of Computational Electronics, Recent Patents on Nanotechnology, Recent Patents on Electrical Engineering, Journal of Low Power Electronics, Journal of Nanoscience and Nanotechnology, and IETE Journal of Research as a subject area Honorary Editor for Electronic Devices and Components. He has extensively reviewed for different journals, including the IEEE TRANSACTIONS ON ELECTRON DEVICES, the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, and the Electronics Letters and Solid State Electronics. He was the recipient of the 29th IETE Ram Lal Wadhwa Gold Medal for a distinguished contribution in the field of semiconductor device design and modeling. He was also the first recipient of ISA-VSI TechnoMentor Award given by the India Semiconductor devices Association to recognize a distinguished Indian Academician or Researcher for playing a significant role as a Mentor and a Researcher.

M. Siva was born in Tiruchanur, Andhra Pradesh, India. He received the B.Tech. degree in electrical and electronics engineering from S.V. University College of Engineering, Tirupati, India, and the M.Tech. degree in integrated electronics and circuits from the Indian Institute of Technology, Delhi, India. He is currently with the Department of Electrical Engineering, Indian Institute of Technology, New Delhi. His research areas include the modeling and simulation of novel device structures for nanoscale applications and the design of analog and mixed signal circuits.