Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs

Tarun Vir Singh, M. Jagadesh Kumar*

Department of Electrical Engineering, Indian Institute of Technology, Delhi, Hauz Khas, New Delhi – 110 016, India

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Abstract

Using two-dimensional simulation, we have demonstrated the effect of the strain or Ge mole fraction \( x \) in a \( \text{Si}_{1-x}\text{Ge}_x \) pillar on the conduction path in cylindrical strained-silicon (s-Si) MOSFETs. We show that for low values of the Ge mole fraction \( x \) in a \( \text{Si}_{1-x}\text{Ge}_x \) pillar, the conduction path forms in the middle of the cylindrical SiGe pillar and not in the s-Si layer at the surface. Only for large values of the Ge mole fraction \( x \) in \( \text{Si}_{1-x}\text{Ge}_x \) pillar does the current conduction path form in the s-Si layer, enabling the advantage of the mobility enhancement of carriers in the device operation. On the basis of our simulation study, we provide the minimum amount of strain or Ge mole fraction \( x \) in a \( \text{Si}_{1-x}\text{Ge}_x \) pillar necessary in a device for the current to flow through the s-Si layer.

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1. Introduction

Scaling down of devices is one of the key methods of enhancing the transistor switching speed. But device length scaling beyond 100 nm has been seriously impeded by the increasing short channel effects (SCEs). Several structures have been proposed for overcoming SCEs, with double-gate (DG) and cylindrical surround gate MOSFETs being the most promising concepts [1–4]. For equivalent silicon and gate oxide thickness, cylindrical MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs for the same SCEs [5]. Cylindrical
MOSFETs offer additional advantages of improved subthreshold slope, higher packing densities, variable pillar doping (along the channel).

The second main factor controlling transistor switching speed is the carrier velocity (or mobility). Strained Si has been used in recent years to improve carrier transport properties, i.e. mobility and high field velocity, and a number of studies have shown the usefulness of strained silicon in extremely scaled down MOSFETs [6–10].

To incorporate the advantages of both the cylindrical surround gate and the strained silicon, strained-Si surround gate MOSFETs have recently been proposed [11]. This device consists of a SiGe pillar over which silicon is grown so that it becomes strained. The amount of strain created in the silicon layer depends on the Ge mole fraction in the SiGe pillar. In the conventional single-gate or double-gate s-Si MOSFETs, the inversion layer forms (and therefore current flows) near the s-Si/SiO$_2$ interface of the device. Due to the mobility enhancement in the s-Si layer, these transistors exhibit enhanced drain current. However, we show in this paper that in the case of cylindrical strained-Si-on-SiGe MOSFETs, the inversion layer forms in the center of the SiGe pillar if the Ge mole fraction $x$ in Si$_{1-x}$Ge$_x$ pillar is not chosen appropriately. To derive the mobility enhancement, the conduction path or the inversion layer must be formed in the strained-silicon layer. Using two-dimensional simulation, we estimate the minimum amount of strain or Ge mole fraction $x$ in a Si$_{1-x}$Ge$_x$ pillar necessary for the conduction path to be formed in the s-Si layer. We show that the minimum Ge mole fraction $x$ in a Si$_{1-x}$Ge$_x$ pillar required increases as the pillar diameter increases but is independent of the s-Si layer thickness. An increase in strain or Ge mole fraction $x$ in a Si$_{1-x}$Ge$_x$ pillar leads to a fall in the threshold voltage of the device [12]. Hence, strain can be introduced effectively in thick-pillar devices only if threshold voltage roll-off can be tolerated.

The simulation work presented in this work is primarily aimed at providing guidelines and motivation for the experimental implementation of cylindrical s-Si-on-SiGe MOSFETs. This study provides the preliminary possibilities and limitations of these devices in order to allow making an appropriate selection of Ge mole fraction $x$ in a Si$_{1-x}$Ge$_x$ pillar.

### 2. Strain related models used in 2D simulation

A silicon thin film grown pseudomorphically over a relaxed Si$_{1-x}$Ge$_x$ substrate experiences biaxial strain leading to changes in band structure [9,13]. Due to strain, the electron affinity of silicon increases and the bandgap decreases. The effect of strain on Si band structure can be modeled as [9,13,14]

$$
(\Delta E_c)_{s-Si} = 0.57x,
$$

$$
(\Delta E_g)_{s-Si} = 0.4x
$$

$$
\phi_t \ln \left( \frac{N_{V, Si}}{N_{V, s-Si}} \right) = \phi_t \ln \left( \frac{m_{h, Si}^*}{m_{h, s-Si}^*} \right)^{3/2} \approx 0.075x
$$

where $x$ is the Ge mole fraction in the Si$_{1-x}$Ge$_x$ substrate, $(\Delta E_c)_{s-Si}$ is the decrease in electron affinity of silicon due to strain, $(\Delta E_g)_{s-Si}$ is the decrease in bandgap of silicon due to strain, $\phi_t$ is the thermal voltage, $N_{V, Si}$ and $N_{V, s-Si}$ are the densities of states in the valence bands in normal and strained silicon respectively. The energy band parameters for Si$_{1-x}$Ge$_x$ substrate can also be estimated as [9,13,14]

$$
(\Delta E_g)_{SiGe} = 0.467x,
$$

$$
N_{V, SiGe} = (0.6x + 1.04(1 - x)) \times 10^{19} \text{ cm}^{-3},
$$

$$
\varepsilon_{SiGe} = 11.8 + 4.2x
$$

### References

[6–10] [11] [9,13,14]
where \( (\Delta E_g)_{\text{SiGe}} \) is the decrease in bandgap of \( \text{Si}_{1-x}\text{Ge}_x \) from that of Si, \( N_{V,\text{SiGe}} \) is the density of states in the valence band in relaxed \( \text{Si}_{1-x}\text{Ge}_x \), and \( \varepsilon_{\text{SiGe}} \) is the permittivity of \( \text{Si}_{1-x}\text{Ge}_x \).

A schematic view of a fully depleted cylindrical surround gate strained MOSFET simulated using 2D device simulator ATLAS [15] is shown in Fig. 1, in which the above strain related models are implemented. The parameters used in our simulation are given in Table 1. In this study we have considered a channel length of 100 nm. However, when the channel length is far less than 100 nm, to incorporate the quantum-mechanical effects, one can use the self-consistent coupled Schrödinger–Poisson model in ATLAS in which the Schrödinger and Poisson’s equations are solved alternately.

The associated energy band diagram from the center of the pillar to its surface is shown in Fig. 2 for different values of the Ge mole fraction \( x \) in the \( \text{Si}_{1-x}\text{Ge}_x \) substrate. With increasing strain (due to increased Ge mole fraction \( x \)), the larger electron affinity leads to electron injection from the SiGe pillar into the s-Si layer and the lower bandgap leads to larger pumping of electrons from the valence band to the conduction band. Hence, the inversion layer electron concentration will be more in the s-Si layer as strain is increased.

Fig. 3 depicts the electron concentration across the device from the center of the pillar to its surface for different values of strain (i.e. different values of the Ge mole fraction \( x \) in the
Fig. 2. Energy band diagram of the structure in Fig. 1 (in the radial direction, from the center of the pillar to the surface) for different values of strain \( x \) (Ge content in the SiGe film).

Fig. 3. Electron concentration profile in the radial direction (from the center of the pillar to the surface).

\( \text{Si}_{1-x}\text{Ge}_x \) pillar). For low values of strain (i.e. lower Ge mole fraction \( x \) in the \( \text{Si}_{1-x}\text{Ge}_x \) pillar), the inversion layer electron concentration is negligible in the s-Si layer compared to its value in the center of the SiGe pillar. Therefore, the majority of the current flow is expected to flow through the SiGe pillar; whereas for high values of strain (i.e. greater Ge mole fraction \( x \) in the \( \text{Si}_{1-x}\text{Ge}_x \) pillar), the current flow should shift to the s-Si layer due to its significantly large inversion layer concentration. This is the preferred mode of current conduction due to the mobility enhancement in the strained-silicon layer.
3. Minimum required Ge mole fraction for threshold condition

Using a 2D device simulator, we have estimated the minimum amount of Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar required to make the inversion layer charge concentration larger in the s-Si layer than in the SiGe pillar so that a significant inversion layer forms in the s-Si layer and not in the SiGe pillar. We have defined the minimum required Ge mole fraction $x$ in the $\text{Si}_{1-x}\text{Ge}_x$ pillar as the condition where the electron concentration in the center of the SiGe pillar is 10 times smaller than the background doping when the peak electron concentration in the s-Si layer equals the background doping. In other words, the gate voltage at which the peak electron concentration in the SiGe pillar is 10 times smaller than the peak electron concentration in the s-Si layer is taken as the threshold condition. This is depicted in Fig. 4.

4. Results and discussion

Fig. 5 shows the variation of the minimum required strain Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar with the SiGe pillar radius. It is observed that the amount of strain and hence the Ge mole fraction $x$ in the $\text{Si}_{1-x}\text{Ge}_x$ pillar necessary to form the conduction path in the s-Si layer increases as the pillar radius increases. This happens because for larger radii, many more electrons must be transferred from the thick pillar to the s-Si layer. Thus, thick cylindrical s-Si MOSFETs must employ a large amount of Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar. Fig. 5 also shows the variation of the threshold voltage of the device with the SiGe pillar radius. The threshold voltage has been obtained for the amount of Ge mole fraction $x$ in the $\text{Si}_{1-x}\text{Ge}_x$ pillar equal to the minimum required strain in the device. We observe that in order to effectively introduce strain in thick-pillar devices, threshold voltage roll-off must be tolerated. This is because thick-pillar devices need a large amount of strain and an increase in Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar leads to a fall in the threshold voltage.

Fig. 6 shows the variation of the minimum required Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar with s-Si film thickness, $t_{\text{s-Si}}$, for different values of SiGe pillar radius. It is observed that minimum required strain or Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar is essentially independent of $t_{\text{s-Si}}$ for the range from 5 nm to 20 nm.
Fig. 5. Variation of minimum required strain or Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar with the SiGe pillar radius.

Fig. 6. Variation of minimum required strain or Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar with strained-Si film thickness $t_{\text{s-Si}}$.

5. Conclusions

In this paper, we have examined the effect of the Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar on the formation of the conduction path in cylindrical strained-silicon MOSFETs using 2D simulation. We have shown that in order for the conduction path to be formed in the s-Si layer, the amount of strain or the Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar in cylindrical s-Si MOSFETs must be
above a certain minimum value. Only then will the current conduction path form in the s-Si layer, enabling the mobility enhancement to be used for enhanced drain current. Further, for thick-pillar devices, the minimum required strain or Ge mole fraction $x$ in a $\text{Si}_{1-x}\text{Ge}_x$ pillar is quite high, which leads to threshold voltage roll-off.

References


