A new symmetrical double gate nanoscale MOSFET with asymmetrical side gates for electrically induced source/drain

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Abstract

In this paper, we present the unique features exhibited by a novel double gate MOSFET in which the front gate consists of two side gates as an extension of the source/drain. The asymmetrical side gates are used to induce extremely shallow source/drain regions on either side of the main gate. Using two-dimensional and two-carrier device simulation, we have investigated the improvement in device performance focusing on the threshold voltage roll-off, the drain induced barrier lowering, the subthreshold swing and the hot carrier effect. Based on our simulation results, we demonstrate that the proposed symmetrical double gate SOI MOSFET with asymmetrical side gates for the induced source/drain is far superior in terms of controlling the short-channel effects when compared to the conventional symmetrical double gate SOI MOSFET. We show that when the side gate length is equal to the main gate length, the device can be operated in an optimal condition in terms of threshold voltage roll-off and hot carrier effect. We further show that in the proposed structure the threshold voltage of the device is nearly independent of the side gate bias variation.

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1. Introduction

The CMOS transistor gate length scaling is projected to continue through 2016 down to the incredible 9 nm [1]. Even if these dimensions can be realized using technological innovations, CMOS devices will suffer from a number of short channel effects, such as the threshold voltage roll-off, the drain induced barrier lowering (DIBL) and the subthreshold swing all of which degrade the MOSFET performance. A number of solutions have been proposed to overcome these problems [2]. Employing a double gate field effect transistor (DG MOSFET) structure instead of using bulk-Si transistors is one of these solutions. In addition to the inherent suppression of SCEs, DG MOSFETs offer high drive current and transconductance [3]. More importantly, the electrical coupling between the two gates results in high $I_{on}/I_{off}$ ratios when the threshold voltage is properly controlled [4,5].

An ultra shallow extended source/drain is another effective method to suppress SCEs. But, it is very difficult to form shallow junctions by conventional fabrication techniques. However, it has been reported that SCEs can be suppressed by using an inversion layer as an ultra shallow extended S/D [6–12]. These devices are known as electrically variable shallow junction MOSFETs (EJ MOSFETs). In spite of the area penalty associated with these devices due to the additional side gates required for the inversion layer formation, EJ MOSFETs are expected to play a major role in the reduction of SCEs and hot carrier effects as discussed in our paper. To combine the advantages of both DG and EJ structures, in this paper we propose a novel symmetrical double gate nanoscale MOSFET with asymmetrical side gates for electrically induced source/drain regions. This structure is similar to that of a symmetrical DG MOSFET with the exception that the front gate...
consists of two asymmetrical side gates on both sides of the main gate. The aim of this paper is, therefore, to present the design and performance considerations of the proposed structure using two-dimensional simulation [13]. First, we have compared the performance of the EJ-DG structure with the symmetrical double gate (S-DG) structure in terms of threshold voltage, subthreshold swing, and electric field. Second, we have investigated the side gate design considerations in terms of threshold voltage, electric field, and hot carriers effects. Based on our simulation results, we demonstrate that the proposed EJ-DG structure is superior to the symmetrical double gate (S-DG) structure in controlling the SCEs.

2. EJ-DG structure

A schematic cross-sectional view of EJ-DG MOSFET implemented using the 2-D device simulator MEDICI is shown in Fig. 1. The front gate consists of two side gates using n+-poly and a main gate using p+-poly while the back gate is a p+-poly gate. The doping in the silicon thin film is kept at $10^{15}$ cm$^{-3}$ (i.e., lightly doped with $N_A < 10^{16}$ cm$^{-3}$ [14]) to avoid adverse effects associated with heavy doping, such as the mobility degradation [15] and the random microscopic fluctuations of dopant atoms [16]. The doping in the n+ source/drain regions is kept at $5 \cdot 10^{19}$ cm$^{-3}$. The typical values of the main-gate and the side gate lengths are identical and equal to 50 nm. The thicknesses of main gate oxide and side gate oxide are identical and equal to 3 nm. The thickness of diffusion barrier between the main and the side gate is 4 nm. The work functions of p+-poly and n+-poly are chosen as 5.25 and 4.17 eV, respectively. The silicon thin film thickness is chosen as 10 nm. All the device parameters of EJ-DG are equivalent to those of the symmetrical DG (S-DG) unless otherwise stated.

Conventional 2-D simulation of semiconductor devices is based on the thermal equilibrium approximation (TEA), which implies that carrier temperatures are equal to the (constant) lattice temperature. For EJ-DG structure, this assumption is invalid since the electric fields in the direction of current flow can be very large. Therefore, we must consider the velocity saturation effects and the local carrier heating in the channel region for accurately predicting the device behavior. Due to local carrier heating, carrier temperatures significantly differ from the lattice temperature resulting in inhomogeneous carrier temperature distributions in the channel region of the device. As a result, the carrier temperature gradients can make the thermal diffusion currents to be significant and together with the local carrier heating may influence the spatial carrier distributions and hence the thermal currents [17–19].

To account for the above, we have selected the full energy balance model for mobility model in our simulations in which the electron temperature is fed back into the continuity equation. Impact ionization is again computed as a post processing step. However, if we choose other mobility models such as the approximate energy balance model, the carrier temperature is never fed back to the drift-diffusion equation [13] and this can result in substantial errors in the prediction of carrier transport.

3. Results and discussion

Fig. 2 shows a typical MEDICI simulated 2-D electron density distribution from source to drain of the EJ-DG structure for the main gate voltage $V_{MGS} = 0$ V, the side

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![Fig. 1. Cross-sectional view of the EJ-DG SOI MOSFET structure.](image1)

![Fig. 2. Electron distribution in the silicon thin film of the EJ-DG structure for $V_{MGS} = 0$ V, $V_{SGS} = 1.5$ V and $V_{DS} = 0$ V.](image2)
gate voltage $V_{SGS} = 1.5$ V and the drain to source voltage $V_{DS} = 0$ V. As can be seen from the figure, the electron distribution in the channel region under the side gates decreases exponentially (linearly in the log scale) from the top of the silicon film to its bottom. Due to the difference between the work functions of the side gates and the back gate, the inversion layer is formed at the top surface of the silicon film under the side gate [20]. But, the electron distribution in the channel region under the main gate is almost fixed and the change is very limited [21]. In other words, the proposed EJ-DG structure is an asymmetrical double gate (A-DG) in the side gate regions, and symmetrical double gate (S-DG) in the main gate region. Therefore, the good features of both the S-DG and the A-DG are combined in the proposed EJ-DG structure.

3.1. Performance comparison with S-DG

In Fig. 3, the surface potential is plotted against the horizontal distance in the channel for the EJ-DG structure. It can be seen from the figure that due to the presence of the electrically induced source/drain, there is no significant change in the potential under the main gate as the drain bias is increased even up to 1.5 V. Hence, in the EJ-DG structure, the channel region under the main gate is "screened" from the changes in the drain potential. As a consequence, $V_{DS}$ has only a very small effect on the drain current after saturation. Therefore, the side gates (i.e. virtual source/drain) are expected to effectively suppress the short channel effects.

The output characteristics of the EJ-DG MOSFET are compared with that of the S-DG MOSFET in Fig. 4. The drive capability of the EJ-DG MOSFET is lower than that of the S-DG MOSFET. This is expected because of the increased source/drain resistance in the EJ-DG MOSFET due to the extremely shallow depth of the inversion layers under the side gates. However, the output characteristics of the EJ-DG MOSFET are nearly ideal with significantly improved output conductance and improved breakdown voltage. These two advantages clearly overweight a small reduction in the drive capability. It is worth noting that adopting the inversion layer as an extended source/drain is very effective in not only controlling SCEs but also reducing source/drain parasitic resistance when a sub-15 nm source/drain is needed for future scaled CMOS [6].

In Figs. 5 and 6, the threshold voltage and the sub-threshold swing of the EJ-DG and the S-DG MOSFET are compared as a function of the main channel length. The threshold voltage values in our simulation are obtained from the commonly used maximum transconductance method. It can be observed clearly that the EJ-DG structure exhibits a lower threshold voltage roll-off. In the case of EJ-DG, when the main channel length is up to 20 nm with the side gate length fixed at 50 nm.
reduced from 60 to 20 nm, the variation in threshold voltage is only approximately 7%. In addition, even for a main channel length of $L_M = 20$ nm the subthreshold swing of the EJ-DG structure is near ideal while it is significantly larger for the S-DG structure.

The threshold voltage as a function of silicon thin-film thickness of the EJ-DG MOSFET is compared with the S-DG MOSFETs in Fig. 7. As can be seen from the figure, when the silicon thin film thickness is reduced from 40 to 8 nm, the threshold voltage roll up of the EJ-DG structure is 51 mV while for the S-DG structure, the roll up is 112 mV. Therefore, in the EJ-DG MOSFETs, the dependence of threshold voltage on the silicon thin-film thickness can be more effectively controlled as compared to the S-DG MOSFETs. This is due to the existence of a workfunction difference in the front gates in the case of EJ-DG MOSFETs.

In Fig. 8, the electric field distribution along the channel near the drain is shown for S-DG and EJ-DG MOSFETs with a channel length $L = 50$ nm. It is evident from the figure that the presence of the induced drain under the side gate reduces the peak electric field considerably.

Fig. 7. Subthreshold swing versus main channel length for channel lengths up to 20 nm with the side gate length fixed at 50 nm.

Fig. 8. Longitudinal electric field along the channel toward the drain end for the S-DG and the EJ-DG MOSFETs.

Fig. 9. Surface potential profiles in the channel of the EJ-DG MOSFET for different side gate biases.
into the channel as the side gate bias increases above 0 V. In other words, the threshold voltage of the device is only marginally dependent on the side gate bias as shown in Fig. 10. Hence, we can consider that the threshold voltage practically remains invariant with the applied side gate bias as well as the main channel length \( L_M \). This is an additional advantage of the EJ-DG structure over that of the conventional EJ MOSFET in which for a main channel length of \( L_M = 80 \) nm, the threshold voltage decreases by approximately 300% when the side gate voltage is varied from 6 to 10 V [7].

3.2. Side gate design considerations

In this section, the main gate length is fixed at 50 nm while the side gate length is varied for investigating the design optimization in terms of threshold voltage roll-off and hot carrier effect.

Fig. 11 shows the dependence of the threshold voltage roll-off on the variation of side gate conditions (length and bias). It can be observed clearly that the EJ-DG structure exhibits a reverse short channel effect (RSCE), i.e. the threshold voltage “rolls-up” when the side gate length is decreased for a fixed main gate length \( L_M \). The threshold voltage roll-up occurs because as the side gate length decreases, the influence of asymmetrical double gate region (side gate region) on the symmetrical double gate region (main gate region) reduces leading to an increase in the threshold voltage. This unique feature of the EJ-DG structure is an added advantage when the device dimensions are continuously shrinking. It is worth noting that the side gate bias affects the threshold voltage only marginally as already shown in Fig. 10.

For investigating the hot carrier effects in the EJ-DG structure, a comparison in terms of the vertical electric field and the electron temperature is performed. Fig. 12 shows the vertical field in the side gate region along A–A’ cut line located at 5 nm from the edge of the side gate on the drain side of the EJ-DG MOSFET. It can be seen that the peak electric field at the front gate side is larger as compared to the back gate and the electric field at the back gate side increases with decreasing the side gate length. Fig. 13 shows the electron temperature at the silicon thin film surface for the S-DG and EJ-DG structures. Due to the high electric field under the side gate region near the drain end, the electron temperature is different from the lattice temperature and this effect increases with decreasing side gate length. Thus, the choice of side gate length determines the extent of hot carrier effects in the device. However, it can be seen from Fig. 13 that the electron temperature for the S-DG structure is greater than that of EJ-DG structure. Since the hot electron effect is dependent on the electron temperature, it is expected that the EJ-DG structure will be less prone to the hot electron effect.
4. Conclusions

In this paper, we have proposed a novel configuration for the symmetrical double gate SOI MOSFET using two side gates in order to investigate the influence of extremely shallow source and drain junctions on the short-channel effects. A constant voltage, independent of the main gate voltage, is applied to the side gates to form inversion layers acting as the extremely shallow virtual source and drain. Based on our simulation results we demonstrate that the combination of extremely shallow junctions and double gate structure effectively reduce the SCEs due to the suppression of the charge sharing by the inversion layer under the side gates. Our results suggest that the optimized side gate length condition, in terms of SCEs and the hot carrier effect, is achieved when the side gate length is equal to the main gate length.

Fig. 13. Electron temperature near the front oxide and silicon interface of the S-DG and EJ-DG MOSFETs.

References