A new Hetero-material Stepped Gate (HSG) SOI LDMOS for RF Power Amplifier Applications

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Abstract

In this paper, we propose a new hetero-material stepped gate (HSG) SOI LDMOS in which the gate is divided into three sections - an n+ gate sandwiched between two p+ gates and the gate oxide thickness increases from source to drain. This new device structure improves the inversion layer charge density in the channel, results in uniform electric field distribution in the drift region and reduces the gate to drain capacitance. Using two-dimensional simulation, the HSG LDMOS is designed and compared with the conventional LDMOS. We demonstrate that the proposed device exhibits 28% improvement in breakdown voltage, 32% reduction in on-resistance, 13% improvement in transconductance, 9% reduction in gate to drain charge and 38% reduction in switching delay. HSG LDMOS may be effectively deployed in RF power amplifier applications.

1. Introduction

Laterally double diffused metal oxide semiconductor (LDMOS) technology is one of the most attractive technologies deployed in RF power amplifier applications because of its ease in integration to standard CMOS technology, high input impedance at high drive current and thermal stability [1]. Especially, silicon on insulator (SOI) LDMOS is more attractive due to its inherent dielectric isolation, high frequency performance and reduced parasitics [2]. However, achieving enhancement in all performance parameters like breakdown voltage, on-resistance, transconductance, drive current, gate to drain charge and switching characteristics is still an active area of research due to its tradeoffs [3]. For example, when we increase the breakdown voltage of the LDMOS, on-resistance also increases [4]. Similarly, when gate oxide thickness is scaled down for improving transconductance, gate to drain charge increases and reliability of gate oxide becomes questionable [5]. Therefore, the motivation of this work is to explore structural changes in SOI LDMOS to improve the device parameters.

In this paper, therefore, we propose a new hetero-material stepped gate (HSG) LDMOS to improve the breakdown voltage and transconductance, and reduce the on-resistance, gate-charge and switching delays. We demonstrate using two dimensional device simulations [6] that the hetero-material stepped gate results in significant improvement in all the above device parameters when compared with the conventional LDMOS.

In section 2, the proposed device structure and its fabrication procedure are explained. In section 3, we explain the expected enhancements with the TCAD simulation results.

2. Device Structure and Proposed Fabrication Procedure

The HSG LDMOS and the conventional LDMOS used for simulation are shown in Fig. 1. As shown in the figure, in the case of HSG LDMOS, there are three steps of gate oxide with thickness, 25 nm, 50 nm and 150 nm from source end to drift region end respectively. The first and third gates are made of p+ poly while middle gate uses n+ poly. The physical dimensions and doping profiles are same for the conventional and the proposed device except that in the case of the conventional device, we have used a single n+ poly gate and the gate oxide is chosen to be 50 nm. The gate oxide thickness and gate work function (n+ and p+ poly) combination of the proposed device is chosen such that the threshold voltage is approximately same as the reference device. The physical and doping parameters are shown in Table 1.
Table 1. Device parameters used in simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length, ((L_{G1}, L_{G2} \text{ and } L_{G3}))</td>
<td>0.3 (\mu)m, 0.7 (\mu)m and 0.4 (\mu)m</td>
</tr>
<tr>
<td>Gate oxide thickness, ((t_{ox1}, t_{ox2} \text{ and } t_{ox3}))</td>
<td>25 nm, 50 nm and 150 nm</td>
</tr>
<tr>
<td>Channel length, (L)</td>
<td>0.5 (\mu)m</td>
</tr>
<tr>
<td>Buried oxide thickness</td>
<td>400 nm</td>
</tr>
<tr>
<td>Silicon thickness</td>
<td>1 (\mu)m</td>
</tr>
<tr>
<td>Drift region length</td>
<td>2.3 (\mu)m</td>
</tr>
<tr>
<td>Source/Drain doping</td>
<td>(1 \times 10^{19}) (\text{cm}^{-3})</td>
</tr>
<tr>
<td>Drift region doping</td>
<td>(2 \times 10^{16}) (\text{cm}^{-3})</td>
</tr>
<tr>
<td>Channel doping</td>
<td>(1 \times 10^{17}) (\text{cm}^{-3})</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>(\approx 1.85) V</td>
</tr>
</tbody>
</table>

Fig. 1. Cross-sectional view of (a) conventional LDMOS (b) HSG LDMOS.

Fig. 2. Process steps to fabricate HSG LDMOS.

Fig. 2 shows the proposed fabrication procedure of HSG gate LDMOS. This process is similar to the method proposed by Xing et al [7]. The fabrication process begins with an SOI wafer with an n-silicon layer with a doping of \(2 \times 10^{16}\) \(\text{cm}^{-3}\). The first 0.3 \(\mu\)m long p⁺ poly gate is formed on a 25 nm thermally grown gate oxide using standard photolithography as shown in Fig. 2 (a). Subsequently, a 50 nm low temperature oxide (LTO) and over that n⁺ poly is deposited. Using blanket reactive ion etching (RIE), the polysilicon layer is etched leaving a sidewall polysilicon layer as shown in Fig. 2(b) which will now act as the second gate of 0.7 \(\mu\)m length. Now, we deposit 100 nm LTO and over that p⁺ poly is deposited and etched back to form 0.4 \(\mu\)m long third gate as shown in Fig. 2 (c). A chemical-mechanical polishing (CMP) process will planarize the gate as shown in Fig. 2(d). Once the gate is defined, rest of the fabrication process is similar to the conventional LDMOS fabrication. After metallization process, source, drain and gate contacts are formed and all the three gates shorted resulting in the final HSG LDMOS structure shown in Fig. 1(b).

3. Simulation results and discussion

We have created the conventional and proposed device structure in ATLAS, a two dimensional device simulator. The design of the LDMOS is done according to RESURF principle [8]. The effect of hetero-material stepped gate on breakdown voltage, DC characteristics, gate charge transients and switching characteristics are discussed below.
3.1. Breakdown Voltage

Breakdown voltage of LDMOS is the drain voltage at which the off state current rises abruptly with the increase in drain voltage (we have taken this drain current as 1 pA/µm). The breakdown voltage characteristics of the HSG LDMOS and the conventional device are shown in Fig. 3. It can be seen that the proposed device exhibits an enhanced breakdown voltage by about 29% compared to the conventional LDMOS.

The stepped gate in the drift region enhances RESURF and introduces additional electric field peaks as shown in Fig. 4. These additional peaks reduce the main electric field peak from $7.1 \times 10^5$ V/cm to $4 \times 10^5$ V/cm and also smear the electric field uniformly resulting in improved breakdown voltage.

3.2. DC Characteristics

The output characteristics of the HSG LDMOS and the conventional LDMOS are shown in Fig. 5. It can be observed that the proposed device has higher drain current than the conventional device. The reduced gate oxide at the source end improves the channel charge density thereby increasing the drain current. The improvement in drain current is approximately 60% at $V_{GS} = 4$ V and $V_{DS} = 20$ V. Due to the improved drain current, specific on-resistance also decreases as shown in Fig. 6. The improvement in on-resistance is 32% at $V_{GS} = 6$ V. Here, the specific on-resistance is calculated as the ratio of drain current by drain voltage per unit area at the gate potential of 6 V. Furthermore, the HSG LDMOS shows 13% enhancement in peak transconductance than the conventional device as shown in Fig. 7. This improvement is again due to the improved channel charge density.
3.3. Gate-Charging Transient

Gate charging transient analysis is important in understanding the switching speed of LDMOS as it reveals the behavior of input capacitance $C_{iss}$ (parallel combination of $C_{GS}$ and $C_{GD}$) [3]. It is desired to have high $C_{GS}$ for higher gate control and lower $C_{GD}$ for higher switching speed. Both of these requirements are expected to be met in the HSG LDMOS since the proposed device has thin gate oxide at the source end and thicker gate oxide at the drift region. Therefore, gate charging experiment is conducted through mixed mode simulations in ATLAS device simulator. The circuit configuration used in the simulation is shown in the inlet of Fig. 8, which has a constant current source charging the gate. The width of the device is chosen to be 10,000 µm.

Fig. 8 shows the gate charge analysis, the initial part of the curve till the slope changes determines the $C_{GS}$, and the next part of the curve with lesser slope determines $C_{GD}$ (miller capacitance). The charging time multiplied by the constant current gives the charge per unit area. It can be seen from Fig. 8, that the gate charge ($Q_{GS}$) of the HSG LDMOS and the conventional LDMOS are 283 pC/mm² and 204 pC/mm² respectively. This is approximately 39% improvement in the gate charge of the HSG LDMOS compared to the conventional device. Similarly, the gate to drain charge ($Q_{GD}$) of the proposed device is 158 pC/mm² and for the conventional device, it is 172 pC/mm². This is a 9% reduction in the gate to drain charge.

3.4. Switching Delay

Switching speed of the LDMOS is calculated by the inverter configuration shown in the Fig. 9. The circuit is implemented using ATLAS mixed mode simulator. The device width is chosen to be 10 µm. The delay is calculated as the difference between input and output pulse at 2.5 V (which is 0.5×$V_{DD}$). From Fig. 9, it can be seen that the switching delay of the HSG LDMOS is reduced by 38% compared to the conventional device.

4. Conclusion

In this paper, we have proposed a new LDMOS with hetero-material stepped gate (HSG) for improved performance. Using two dimensional numerical simulations, the proposed device is demonstrated to exhibit improved breakdown voltage, drive current, transconductance, on-resistance, gate charge and switching speed compared to the conventional device. These improvements have been realized without
unduly increasing the fabrication complexity. The proposed device can be advantageously deployed for RF power applications.

5. References


