Compact Modeling of Partially Depleted Silicon-on-Insulator Drain-Extended MOSFET (DEMOS) including High-voltage and Floating Body Effects

Tarun Kumar Agarwal, Amit R. Trivedi, Vaidyanathan Subramanian, and M. Jagadesh Kumar, Senior Member, IEEE.

Abstract—In this paper, a scalable compact model for partially depleted SOI drain extended MOSFETs (DEMOS) is developed using a sub-circuit approach. The proposed compact model captures the special dc behavior of a partially depleted SOI DEMOS transistor. Our model accounts for high voltage effects such as quasi saturation, impact ionization in the drift region along with a floating body effect such as the kink effect in the output characteristics of the floating body PD SOI DEMOS transistor. In the sub-circuit approach used, the channel region is modeled using the BSIM4SOI model and the drift region is modeled using a bias-dependent resistance model along with a current-controlled current source. The model is validated for a set of channel and drift lengths to demonstrate the scalability of the model. The accuracy of the proposed compact model is verified using 2-D numerical simulations.

Index Terms—SOI DEMOS, High voltage devices, quasi saturation, impact ionization, Sub circuit approach, floating body effects, kink effect, Compact model, Scalability.

I. INTRODUCTION

Currently, the drain extended MOSFETs (DEMOS) have become quite preferable as a high voltage (HV) device for smart power IC’s and interest in the accurate modeling of HV MOS transistors has increased in recent years due to the compatibility of these devices with standard CMOS technology [1]. HV MOS transistors can be designed for a wide range of voltage supplies, ranging from 5 V to 1000 V, leading to numerous applications, ranging from a power amplifier (PA) in mobile handsets and base stations to automotive systems [2]. Over the years, as Si-RF technologies are maturing, silicon-on-insulator (SOI) HV MOSFETs have become a preferred choice over bulk HV MOSFETs providing enhanced power added efficiency (PAE) and reduced crosstalk [3]. Optimal design of power circuits requires an accurate compact model of partially depleted SOI DEMOSFETs, which captures the high voltage behavior along with the floating body effects.

To model the bulk HV MOSFETs and the SOI HV MOSFETs with a body contact, various modeling approaches are reported in literature [4]–[9]. A frequently followed approach is to use a sub circuit along with the conventional low-voltage MOS transistor models. Some compact models are examples of this approach such as HV-EKV [4], [5], MM20 models [6], [7]. These models account only for the quasi saturation effect and show good results in terms of accuracy and speed for both dc and ac domains. But, sufficient emphasis on accurate modeling of other high voltage effects such as impact ionization in the drift region is not present in these models and also channel length scaling is not reported for all dc characteristics of HV MOSFETs. On the other hand, Wang et al. [10] report only the impact ionization in the drift region at higher gate biases and a physical model based on the BSIM3 substrate current model to model the impact ionization in the drift region. To the best of our knowledge, there is no compact model in literature for the floating body partially depleted SOI DEMOSFETs taking into account the quasi saturation effect, the impact ionization in the drift region and the kink effect in the output characteristics.

The aim of this paper is, therefore, to develop a scalable compact model for partially depleted SOI DEMOSFETs simultaneously considering all the above special dc effects. To model these effects accurately, a sub-circuit consisting of a bias-dependent resistor and a current-controlled current source are used along with the BSIM4SOI compact model [11], [12]. The BSIM4SOI compact model can predict the kink for the gate biases where the channel region current is dominating. But, as the drift region starts dominating at higher gate biases, a sub-circuit is needed to model the kink effect along with the other high voltage effects. The other effects dominant in SOI transistors such as self-heating effect (SHE) can be easily modeled using the BSIM4SOI model and the developed model can be extended to capture ac behavior of a PD SOI DEMOS transistor. It may be noted that our compact model in its present form does not model the breakdown characteristics accurately. The accuracy of the proposed compact model is verified by 2-D device simulations [13].

II. DEVICE STRUCTURE AND SIMULATION RESULTS

Fig. 1 shows the cross sectional schematic of a conventional floating body PD SOI MOS and a floating body PD SOI DEMOS transistor respectively. It is shown that a floating
body DEMOS device shown in Fig. 1(b) is derived from a PD SOI NMOS device shown in Fig. 1(a) by simply extending the drain of the device with a lightly doped drift region. Similarly, a body contacted DEMOS device can be derived from a floating body DEMOS device shown in Fig. 1(b) by simply having a p-type doped region beneath the source. The device parameters for simulation are given in Table I. Based on a fabricated high voltage PD SOI MOS device in [14]. The device simulations are done using a 2-D numerical simulator, ATLAS from SILVACO [13]. To maintain sanity and self-consistency in the simulated data, calibration of the impact ionization model in ATLAS is performed with the measured data of a PD SOI DEMOS device fabricated with SOI CMOS process [14]. In calibration, impact ionization coefficients are optimized to best fit the experimental results (AN1 = 2x10^6 cm^{-1}, AN2 = 2x10^6 cm^{-1}, BN1 = 1.7x10^9 V/cm and BN2 = 1.7x10^6 V/cm). Further details are provided in Appendix A. The drift region doping for the reference device is chosen to have a breakdown voltage higher than 15 V for the floating body device and 20 V for the body contacted device. Some aspects such as graded channel doping density and gate overlap are not considered in the design of DEMOS device shown in Fig. 1(b). This is due to the availability of sub micrometer photolithography to define the channel length in the same way as CMOS devices and a self aligned drift-region implantation to the gate, rather than relying on the double-diffusion process [15].

The concept of intrinsic drain potential ($V_K$) has been a powerful tool to understand and model the high voltage effects observed in HV MOS transistors [16]. As Fig. 1(b) shows, $V_K$ denotes the surface potential at the junction of the intrinsic MOS region and the drift region. Fig. 2 shows the variation of $V_K$ with gate and drain biases for the body contacted PD SOI DEMOS device obtained using ATLAS. An interesting observation from Fig. 2 is that $V_K$ decreases with $V_G$ after reaching a maximum ($V_{K,MAX}$) at a fixed drain voltage $V_D$. The reasons for this reduction in $V_K$ are clearly explained in [16]. Our analysis also shows that for lower values of $V_G$, when the pinch-off of the depletion region in the drift region occurs, $V_K$ reaches its maximum value ($V_{K,MAX}$) and current will be forced through the depletion zone of the drift region. However, as $V_G$ increases, pinch-off is delayed resulting in a local accumulation or corner injection of carriers in the substrate near the drift region leading to the $V_K$ reduction with $V_G$ after reaching the maximum [16].

Further, it can be physically explained using Kirk Effect. Kirk effect states that when the injected electron density from channel to the drift region exceeds the doping concentration of the drift region ($N_{dr}$), the peak electric field shifts from the channel-drift ($p^{-}n^{-}$) junction to the drift-drain ($n^{-}n^{+}$) junction at higher gate biases [17]. It further explains that $V_K$ increases with the gate voltage due to the existence of peak electric field at the channel-drift ($p^{-}n^{-}$) junction. This leads to an increase in the surface potential at $p^{-}n^{-}$ junction with an increase in the gate voltage. And, with further increase in the gate voltage, $V_K$ decreases due to the existence of the peak electric field at the drift-drain ($n^{-}n^{+}$) junction. As a result, the surface potential decreases at the $p^{-}n^{-}$ junction while it increases at the $n^{-}n^{+}$ junction. Based on the variation of $V_K$ with the gate voltage, we define two modes of operation for HV MOSFETs. First being, a low voltage FET (or intrinsic MOS) dominant mode of operation in which $V_K$ increases with the gate voltage and reaches to a maximum ($V_{K,MAX}$). Second mode of operation is when the drift region starts dominating and $V_K$ starts decreasing from $V_{K,MAX}$ with an increase in the gate voltage. Based on the variation of $V_K$, quasi saturation and the impact ionization in the drift region are physically explained using Kirk effect which further explains the second hump in the impact ionization current as shown in Fig. 3. To understand the kink behavior in the floating body PD SOI DEMOSFETs, a conventional PD SOI MOS transistor is chosen as a starting point. And it is observed that a floating body PD SOI DEMOS device behaves as a conventional floating body PD SOI MOS device in the first mode of operation based on the $V_K$ variation. And, in the drift dominant second mode of operation, due to the impact ionization in the drift region or electron-hole pair generation at $n^{-}n^{+}$ junction, the floating body potential shows different behavior than a conventional floating body PD SOI MOS transistor as shown in Fig. 4. It is clear from Fig. 4(b) that in the drift dominant mode of operation, the body potential starts rising at lower drain voltages, resulting in a kink in the output characteristics of the floating body PD SOI DEMOSFETs at lower drain voltages. And, with further increase in the gate voltage, the transistor enters the deep triode region of operation and the kink in the output characteristics disappears as shown in Fig. 5(b). In conclusion, to accurately model the kink behavior in the drift dominant mode of operation, the impact ionization in the drift region is to be accurately modeled.

### III. Modeling Strategy

Based on the physical insights gained from the device simulations, a compact model for partially depleted SOI DEMOSFETs is derived from the BSIM4SOCI model and the sub-circuit. Here, the BSIM4SOCI model is used to model the intrinsic MOS dominant mode of operation and the sub circuit, containing a bias-dependent resistance and a current-controlled current source, is used to model the drift region dominant mode of operation of the transistor. Fig. 6 shows the SPICE sub-circuit implementation, containing an intrinsic MOSFET, a bias-dependent resistor and a current-controlled current source (CCCS). The drain terminal of the intrinsic MOSFET is named as “K”, $V_K$ is calculated using the BSIM4SOCI model and the bias-dependent resistor within the simulator. In this way, the drain to source current ($I_{DS}$), body current ($I_B$) and $V_K$ are expressed explicitly in terms of the external node voltages (D, G, S, B, X) where X (substrate node) is always grounded.

#### A. Channel region or intrinsic MOS modeling

The intrinsic MOSFET of the PD SOI DEMOS device is modeled using the BSIM4SOCI compact model. The BSIM4SOCI model shows good capability in modeling floating body effects, observed in partially depleted SOI MOSFETs, along with self heating effects (SHE) by using an improved impact ionization current and parasitic BJT current model [18].
In floating body configuration, only three external nodes are present for the intrinsic MOS which are gate (G), source (S) and substrate (X) while drain (K) and body (B) node voltages of the intrinsic MOS ($V_D$ and $V_K$) are calculated iteratively in circuit simulation. The potential of body node $V_B$ is calculated by the balance of all body current components and $V_K$ is calculated by the intrinsic MOS and the drift region currents. The body resistance, which is the part of the BSIM4SOI model, is neglected in the developed model i.e. the body resistance model parameters present in the BSIM4SOI model are set to their default values. The channel current, calculated using the BSIM4SOI model, is a function of $V_K$, $V_G$, $V_S$, $V_B$ and $V_X$. The impact ionization current due to the channel region ($I_{ii1}$) is also calculated using the BSIM4SOI model. $I_{ii1}$ is a function of $I_{KS}$, $V_{KS}$, $V_{GS}$ and $V_X$.

### B. Drift region modeling

In the drift region dominant mode of operation, the HV-MOSFETs shows two important effects: (i) quasi saturation (as the drain current compression in the output characteristics) and (ii) the impact ionization in the drift region (as a second hump in the body current variation with gate voltage).

#### a) Quasi saturation: Attempt to model quasi saturation accurately with JFET and a bias-dependent resistance are reported in literature [19]–[21]. However, to have a scalable model, bias-dependent resistance is more popular. In our work, a scalable bias-dependent drift region resistance ($R_{DRIFT}$) model is based on the equations used in the industry standard compact model HiSiM HV [22]. The modified equations for $R_{DRIFT}$ model are given as:

$$R_{DRIFT} = (R_D \cdot L_{DR} + f(V_{DS})) \cdot f(V_{GS}) \cdot f(V_{BS})$$

where,

$$f(V_{DS}) = \frac{V_{asat} \cdot R_{DV}}{R_{DV}}$$

$$f(V_{GS}) = \left(1 + R_{DV}G1 - \frac{R_{DV}G1}{R_{DV}G2}\right) V_{GS}$$

$$f(V_{BS}) = 1 - R_{DV}B \cdot V_{BS}$$

$$R_{DV} = R_{DV}G \cdot \left(1 + \frac{R_{DV}D}{L_{GATE} \cdot 10^2 R_{DV}DSP} \cdot SC\right)$$

$$SC = \frac{L_{DR} \cdot RDSC1 + RDSC2}{L_{DR}}$$

#### b) Impact ionization in the drift region: The impact ionization current, in DEMOS devices, has contributions from both the channel-drift and the drift-drain junctions as shown in Fig. 3. As the BSIM4SOI’s improved impact ionization model is only capable of modeling the impact ionization at the channel-drift junction using $I_{ii1}$, an extra current-controlled current source ($I_{ii2}$) is added between external drain and body nodes to model the impact ionization at the drift-drain junction. Here, the derived equations for extra body current are physical as they involve $V_K$, solved by the simulator. A general body current equation due to the impact ionization in the drift region can be written as:

$$I_{ii2} = \int_0^{L_{DR}} \alpha \cdot I_{DS} \cdot \exp(-\frac{B}{E_g})dy$$

Eq. 7 can be approximated into a well known equation as given below [23]:

$$I_{ii2} = \alpha \cdot (V_D - V_K) \cdot I_{DS} \cdot \exp\left(-\frac{B \cdot L_{DR}}{(V_D - V_K)}\right)$$

Here, $V_K$ is the potential at $y=0$ (at body-drift junction) and $V_D$ is the potential at $y=L_{DR}$. As shown in Fig. 3, $I_B$ increases with gate voltage continuously until the device breaks down after the transistor enters the triode region. To model this behavior, Eq. 8 is modified as:

$$I_{ii2} = \alpha \cdot (V_D - V_K) \cdot I_{DS} \cdot \exp\left(-\frac{B}{E_{eff}}\right)$$

where,

$$E_{eff} = \frac{(V_D - V_K) \cdot (V_{GS} - V_{OFF})^{coeff1}}{L_{DR}}$$

Model parameters in the current-controlled current source model (Eq. 9) are $\alpha$, $B$, $V_{OFF}$ and $$.
Fig. 10 shows that the calculated output characteristics of the body contacted transistor are in excellent agreement with the 2-D numerically simulated data for different channel and drift lengths. It is clear that the quasi saturation effect is well modeled using a scalable bias-dependent drift resistance model. The drift resistance model captures the increase in the drift resistance with increase in the drift length shown in Fig. 10(a) and Fig. 10(b). It also predicts a higher drain resistance at lower channel lengths to model the quasi saturation effect at lower gate biases for short channel devices as shown in Fig. 10(a) and Fig. 10(c). To accurately calculate the inferred body potential in the floating body PD SOI DEMOS, all the body current components such as impact ionization current, diode current and parasitic BJT currents need to be accurately modeled. Fig. 8 shows that the impact ionization current due to both channel and drift region is well modeled for different channel lengths. The impact ionization in the channel region is modeled using BSIM4SOI model parameters while impact ionization in the drift region is modeled using a current-controlled current source described in section III. Fig. 11(a) shows that the kink behavior in the quasi saturation regime is well captured by accurately modeling the impact ionization in the drift region. The output characteristics of a floating body PD SOI DEMOS transistor is accurately modeled across various channel and drift lengths, as shown in Fig. 11. This paper mainly focuses in modeling high voltage and floating body effects observed in PD SOI DEMOSFETs. Other second order effects such as self heating are not taken into account, but can easily be included by extracting the BSIM4SOI self heating model parameters.

V. CONCLUSION

A scalable compact model for high voltage PD SOI devices is developed using a proposed sub-circuit approach. The developed compact model includes the high voltage and the floating body effects observed in PD SOI DEMOS devices. The relationship between the proposed sub-circuit modeling approaches and the physical mechanism of high voltage PD SOI MOS devices has also been discussed based on the device simulation results. Using the 2-D numerical simulator, ATLAS, a physical description of the specific dc behavior of partially depleted SOI DEMOSFETs is presented. The famous kink effect is studied for high-voltage floating body PD SOI devices. And, it is demonstrated that the kink effect disappears when the high voltage transistor enters deep quasi saturation regime. In the proposed modeling approach, the sub-circuit comprises of a intrinsic MOSFET and the drift region which are modeled using the BSIM4SOI model and a bias-dependent resistor respectively. Additionally, to model the impact ionization in the drift region, a current-controlled current source is added to the sub-circuit. The model performance is demonstrated for the 20-V DEMOS device by implementing the SPICE sub-circuit in Spectre (Cadence). Generally, the proposed compact model can be run on any SPICE simulator, since the model equations of the standard BSIM4SOI compact model are not changed. Therefore, the developed compact model in this paper will enable the accurate design of complex circuits using PD SOI DEMOS devices based on SPICE simulation.

ACKNOWLEDGMENT

The authors would like to thank Y. S. Chauhan, A. Bandopadhyay and folks at SRDC, Bangalore for their interesting comments. This work was sponsored by Semiconductor Research and Development Center, IBM, Bangalore, India. We are grateful to the reviewers for their careful and critical comments which have significantly improved the readability and usefulness of the paper.

REFERENCES

APPENDIX A

CALIBRATION PROCEDURE

To achieve sanity and self consistency in the data obtained using ATLAS for modeling purpose, the coefficients of the impact ionization model, in ATLAS, are found out using the calibration procedure described below. While, the other physical models, used in simulation by ATLAS, use the default value of coefficients.

In our calibration, a device structure similar to the one used in [14] is created and simulated using ATLAS. Then, the output characteristics of SOI DEMOS transistor with and without the body contact are compared. Fig. 12(a) and 12(b) depict the measured output characteristics and those obtained using TCAD simulations primarily to show the off state breakdown voltage and the kink in the output characteristics. The calibrated device used for the TCAD simulation is not the exact replica of the experimental device. The main intention of showing the experimental data from [14] in Fig. 12 was merely as a guideline in order to come up with self consistent and meaningful data from device simulations which could then be used for the modeling part. However, the simulated data used in this paper is self-consistent which is shown by the presence of the kink in the output characteristics of the floating body device, the lower breakdown voltage of floating body device in comparison to the body contacted device and the scaling behavior with the channel and the drift length. In the end, the impact ionization model coefficients are optimized to best fit the TCAD generated results such as the off-state breakdown voltage of SOI DEMOS device, with and without the body contact.

APPENDIX B

DRIFT RESISTANCE EXTRACTION PROCEDURE

The drift resistance equation is, based on the equations used in the industry standard compact model HiSiM HV, given by Eq. 1. The equation shows the drift resistance dependence on gate, drain and body bias along with the gate length. The extraction procedure for the model parameters used in these equations can be summarized in the following steps:

1) Firstly, a wide gate length device is chosen for extracting the model parameters used in $R_{\text{DRIFT}}$ equations such as $R_{D}$, $asat$, $RDV_{G1}$, $RDV_{G2}$, $RDV_{B}$ and $RDV_{D}$.
   - At low drain biases, all the BSIM4SOI model parameters pertaining to the mobility, subthreshold slope, $V_{T,LIN}$ and body effects are extracted.
   - Using the $I_{DLIN}$ at higher gate biases, the $R_{\text{DRIFT}}$ at low drain bias is modeled using the parameter $R_{D}$. This is followed by the medium and high drain bias modeling i.e. the output characteristics fitting.
   - The drain bias dependence of $R_{\text{DRIFT}}$ i.e. $RDV_{D}$ is extracted by fitting the output characteristics slope and the quasi saturation regime.
   - Similarly, the gate bias dependence of $R_{\text{DRIFT}}$ i.e. $RDV_{G1}$ and $RDV_{G2}$ and the body bias dependence i.e. $RDV_{B}$ are extracted.

2) Then, the deviations associated with the small geometries are taken into account by extracting the parameters $RDV_{DS}$, $RDV_{DSP}$, $RD_{SC1}$ and $RD_{SC2}$, following the step 1.
TABLE I
DEVICE PARAMETERS USED IN THE SIMULATION, DERIVED FROM A REFERENCE DEVICE IN [14].

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>$t_{OX}$</td>
<td>Gate oxide thickness</td>
<td>30 nm</td>
</tr>
<tr>
<td>$t_{SI}$</td>
<td>Silicon film thickness</td>
<td>180 nm</td>
</tr>
<tr>
<td>$t_{BOX}$</td>
<td>Buried oxide thickness</td>
<td>1 μm</td>
</tr>
<tr>
<td>$N_{ch}$</td>
<td>Channel doping (p-type)</td>
<td>$1.5 \times 10^{17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>$N_{dr}$</td>
<td>Drift region doping (n-type)</td>
<td>$4 \times 10^{16}$ cm$^{-3}$</td>
</tr>
<tr>
<td>—</td>
<td>S/D doping concentration</td>
<td>$10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>$L_{CH}$</td>
<td>Channel length</td>
<td>0.64 μm</td>
</tr>
<tr>
<td>$L_{DR}$</td>
<td>Drift region length</td>
<td>1 μm</td>
</tr>
</tbody>
</table>

![Fig. 1. Cross sectional schematics of the n-channel devices. (a) A conventional floating body partially depleted SOI MOSFET. (b) A floating body partially depleted drain extended MOSFET (DEMOS).](image)

![Fig. 2. Variation of $V_K$ with gate bias for different drain biases obtained using ATLAS for a body contacted PD SOI DEMOS device.](image)

![Fig. 3. Variation of the body current with gate bias for a body contacted PD SOI DEMOS device showing impact ionization in the drift region at higher gate biases, obtained using ATLAS.](image)
**Fig. 4.** Body potential variation with drain bias obtained using ATLAS. (a) A conventional floating body partially depleted SOI MOSFET. (b) A floating body partially depleted drain extended MOSFET (DEMOS).

**Fig. 5.** Output characteristics of the n-channel devices obtained using ATLAS. (a) A conventional floating body partially depleted SOI MOSFET. (b) A floating body partially depleted drain extended MOSFET (DEMOS).

**Fig. 6.** SPICE sub-circuit implementation with the BSIM4SOI compact model.
Fig. 7. (symbols) 2-D numerically simulated and (solid lines) calculated $V_K$ and $V_B$ characteristics of (a) Body contacted PD SOI DEMOS and (b) Floating body PD SOI DEMOS using BSIM4SOI approach for $L_{CH}=0.64 \mu m$ and $L_{DR}=1 \mu m$.

Fig. 8. (symbols) 2-D numerically simulated and (solid lines) calculated body current characteristics of PD SOI DEMOS using BSIM4SOI approach for (a) $L_{CH}=0.64 \mu m$ and $L_{DR}=1 \mu m$. (b) $L_{CH}=3 \mu m$ and $L_{DR}=1 \mu m$. 
Fig. 9. (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a body contacted PD SOI DEMOS using BSIM4SOI approach at $V_B = 0.7$ V for (a) $L_{CH}=0.64 \, \mu m$ and $L_{DR}=1 \, \mu m$. (b) $L_{CH}=0.64 \, \mu m$ and $L_{DR}=3 \, \mu m$. (c) $L_{CH}=3 \, \mu m$ and $L_{DR}=1 \, \mu m$.

Fig. 10. (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a body contacted PD SOI DEMOS using BSIM4SOI approach for (a) $L_{CH}=0.64 \, \mu m$ and $L_{DR}=1 \, \mu m$. (b) $L_{CH}=0.64 \, \mu m$ and $L_{DR}=3 \, \mu m$. (c) $L_{CH}=3 \, \mu m$ and $L_{DR}=1 \, \mu m$. 
Fig. 11. (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a floating body PD SOI DEMOS using BSIM4SOI approach for (a) $L_{CH}=0.64$ $\mu$m and $L_{DR}=1$ $\mu$m, (b) $L_{CH}=0.64$ $\mu$m and $L_{DR}=3$ $\mu$m, (c) $L_{CH}=3$ $\mu$m and $L_{DR}=1$ $\mu$m.

Fig. 12. Measured and TCAD generated output characteristics of a SOI DEMOS device with and without body contact. (a) Measured output characteristics [14] and (b) Output characteristics obtained using ATLAS at $V_{GS}=3.5, 3.0, 2.5, 2.0, 1.5, 0$ V.
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