Design of High Performance Lateral Schottky Structures using Technology CAD

A dissertation submitted in partial fulfillment of
the requirement for the degree of
Master of Science (Research)

by
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May 5, 2003

Certificate

This is to certify that the thesis entitled **"Design of High Performance Lateral Schottky Structures using Technology CAD"** being submitted by **Linga Reddy C (2000EEM010),** for the award of degree of **Master of Science (Research)** in **Electrical Engineering** to the **Indian Institute of Technology, Delhi,** is a record of bonafide work done by him under my guidance and supervision.

It is further certified that this work has not been submitted anywhere else for the award of degree or diploma.

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Abstract

Schottky junctions are well known for their low forward drop and insignificant storage effects. Their application in both the two-terminal and three-terminal devices to enhance the high-speed performance has gained importance due to the technological ability to prepare extremely clean semiconductor surfaces. In the recent past, several novel rectifier as well as transistor structures have been reported using Schottky junctions. SiC Schottky rectifiers have several advantages in high temperature, high speed and high voltage applications. Although a number of vertical SiC Schottky rectifiers have been reported in literature, lateral Schottky rectifiers are increasingly becoming important because of their utility in power ICs.

Due to it's excellent material properties of SiC, device designers have started using it as emitter in high-performance HBTs where as SiGe is an excellent semiconductor for RF applications. Replacing the collector-base p-n junction by a Schottky junction in BJTs has been proposed to reduce the collector resistance, base widening and to improve the transient response of the transistor. But all these proposed devices are vertical in nature and not compatible with standard CMOS processes, so they could not gain wider acceptability in VLSI BiCMOS applications.

In the present work, to enhance the performance limits of Schottky rectifiers and HBTs, we have proposed four high performance BiCMOS compatible lateral Schottky devices in Silicon-On-insulator (SOI) technology namely, 1) A Novel high voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) rectifier, 2) Lateral Dual Sidewall Schottky (LDSS) concept for improved rectifier performance on SOI, 3) A Novel lateral N-SiC emitter P-SiGe base Schottky Metal-collector (NPM) HBT on SOI and 4) A New lateral dual – bandgap P-emitter N-SiGe base Schottky Metal-collector (PNM) HBT on SOI with reduced collector – emitter offset voltage.

We have used carefully calibrated two-dimensional simulations to study the characteristics of the proposed devices in this work. Based on the simulated results, we have analyzed the reasons for the improved performance of the proposed structures over the conventional devices. We have also presented a BiCMOS compatible fabrication procedure for all our proposed devices. The results presented in our work are expected to be an incentive for further experimental exploration by other researchers.

Contents

Chapter 1

Introduction

1.1 Applications and necessity of lateral devices on SOI

Schottky junctions are well known for their low forward drop and insignificant storage effects. Though several vertical Schottky rectifiers with improved performance are reported [1-3] in the literature, lateral Schottky rectifiers are becoming more popular due to easy integration of these devices into CMOS and BiCMOS process technologies. For RF and mixed signal circuits, high performance (High current gain, high cut-off frequency and high transconductance) transistors are necessary. The RF performance of high-frequency transistors is limited by the parasitic RC time constants arising from the series resistances and shunting capacitances of the transistors. Control of these parasites is a key issue in the development of advanced transistors. In this context, the SOI technology has emerged as a best technology to alleviate the above problem and support the needs of VLSI applications. Recently, lateral bipolar transistors [4-10] have been implemented on SOI technology by taking the full advantages of SOI technology. Although the conventional vertical HBTs on bulk substrate will meet most of the performance requirements for RF applications, complicated fabrication processes of these devices is the major drawback and this leads to uneasy integration of these device into BiCMOS technology subsequently which leads to the high cost of technological development and manufacturing. On the other hand, the present SOI lateral HBT is

easily integrable with SOI BiCMOS technology. In the most simplified process, SOI BiCMOS integration will be possible with few extra masks and ion implants with minor modification of standard CMOS process. SOI BiCMOS technology for mixed signal applications has been a very attractive alternative to its bulk counterpart as it offers the advantages such as (i) Reduced analog-to-digital crosstalk noise, (ii) Decrease of sensitivity to alpha particles, (iii) Reduction of substrate capacitance and (iv) Better device isolation. Therefore, the use of lateral HBTs in SOI BiCMOS should lead to realization of the above advantages with no added process complexity.

1.2 Previous work

SiC Schottky rectifiers have several advantages in high temperature, high speed and high voltage applications [11]. Although a number of vertical SiC Schottky rectifiers have been reported in literature [12], lateral Schottky rectifiers are increasingly becoming important because of their utility in power ICs [13-15]. Recently, Kumar and Singh [15] have reported that Schottky rectifiers with sharp reverse breakdown can be achieved using the sidewall Schottky contact of a trench filled with a metal. Selecting a metal for this Lateral Trench Sidewall Schottky (LTSS) rectifier with a suitable work-function plays a vital role in deciding its forward and reverse characteristics. If a low-barrier metal is used for the Schottky contact in the LTSS rectifier, it will result in a low forward voltage drop but the reverse leakage current will be large and vice-versa for a high-barrier Schottky contact. Achieving both the low forward voltage drop and less reverse leakage current in LTSS rectifier is impossible without making a trade off between forward voltage drop and reverse

leakage current. In this work we propose a novel concept called Lateral Dual Sidewall Schottky (LDSS) for both SiC and Si to overcome the above problem.

Replacing the collector-base p-n junction by a Schottky junction in BJTs has been proposed [16] to reduce the collector resistance, base widening and to improve the transient response of the transistor. But these Schottky structures are vertical in nature and not compatible with standard CMOS processes, so they could not gain wider acceptability in VLSI BICMOS applications. Recently, it has been shown that lateral Schottky BJTs which are compatible with BiCMOS technology can also be made [17]. Further, to improve the performance of BJTs, device designers have started recognizing the utility of wide bandgap emitter (e.g. SiC emitter [18]) and narrow bandgap base (e.g. SiGe base) in BJTs for high speed circuit applications. To combine the advantages of SiC-emitter and SiGe-base together with the combination of SOI technology and lateral Schottky collector, in this work we propose a novel SiC emitter SiGe base lateral NPM Schottky collector HBT on SOI. Wide bandgap HBTs are, however, prone to an increased collector-emitter offset voltage and this problem is more severe in PNP HBTs. As a result, making PNP HBTs which are compatible with NPN HBTs is very difficult. To overcome this problem, we propose a novel technique in which a dual bandgap emitter is used.

1.3 Objectives of the thesis

The main objective of this thesis is to propose novel lateral Schottky structures for high speed applications. The structures we have studied are: i) A Novel high voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) rectifier, ii) Application of Lateral Dual Sidewall Schottky (LDSS) concept for improved rectifier performance on SOI,

iii) A Novel lateral N-SiC emitter P-SiGe base Schottky Metal-collector (NPM) HBT on SOI and iv) A New lateral dual – bandgap P-emitter N-SiGe base Schottky Metal-collector (PNM) HBT on SOI with reduced collector–emitter offset voltage. From our simulation study, we demonstrated that LDSS rectifier exhibits low forward drop as well less reverse leakage current and proposed HBTs exhibit excellent performance over its counterparts. We have also presented a BiCMOS compatible fabrication procedure for all our proposed devices. We have shown from our simulation results that the proposed LDSS rectifiers attractive for use in high-speed and low-loss power IC applications and proposed HBTs are attractive for high frequency and low power BiCMOS VLSI applications.

1.4 Thesis organization

The dissertation is divided into six chapters and its outline is described as given below.

- **Chapter One: Introduction.**

  Fundamental concepts related to Lateral devices and SOI, previous work, objectives and organization of the thesis.

- **Chapter Two: A Novel high voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) rectifier with ideal forward and reverse characteristics.**

  This chapter introduces a new concept called Lateral Dual Sidewall Schottky (LDSS) to attain the low forward voltage drop which is close to that of a Schottky rectifier with low barrier metal as well as less reverse leakage current which is close to that of a Schottky rectifier with high barrier metal.

- **Chapter Three: Application of Lateral Dual Sidewall Schottky (LDSS) concept for improved rectifier performance on SOI.**

  This chapter demonstrates the application of Lateral Dual Sidewall Schottky (LDSS) concept on SOI to get the improved performance over its equivalent devices namely Lateral Conventional Schottky (LCS) and Lateral Trench Sidewall Schottky (LTSS) rectifiers.

- **Chapter Four: 2D-Simulation and analysis of a novel SiC N-emitter SiGe P-base lateral Schottky Metal-collector (NPM) HBT on SOI.**

  This chapter describes the design and analysis of SiC wide bandgap N-emitter and P-SiGe base lateral Schottky Metal-collector (NPM) HBT on SOI.

- **Chapter Five: A New dual – bandgap P-emitter SiGe N-base lateral Schottky Metal-collector (PNM) HBT on SOI with reduced collector – emitter offset voltage.**

  This chapter presents a novel solution to deal with the offset voltage problem in wide bandgap emitter PNP/PNM HBTs.

- **Chapter Six: Conclusions.**

Chapter 2

A Novel High Voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) Rectifier with Ideal Forward and Reverse Characteristics

2.1 INTRODUCTION

SiC Schottky rectifiers are now well known for their advantages in high temperature, high speed and high voltage applications [11]. Although several vertical SiC Schottky rectifiers have been reported in literature [12], lateral Schottky rectifiers are increasingly becoming important because of their utility in power ICs [13-15]. Recently, Kumar and Singh [15] have demonstrated that Schottky rectifiers with high breakdown voltage and PiN diode like sharp reverse breakdown can be achieved using the sidewall Schottky contact of a trench filled with a metal. Selecting a metal for this Lateral Trench Sidewall Schottky (LTSS) rectifier with a suitable work-function plays a vital role in deciding its forward and reverse characteristics. If a low-barrier metal is used for the sidewall Schottky contact in the LTSS rectifier, it will result in a low forward voltage drop but the reverse leakage current will be large and vice-versa for a high-barrier Schottky contact. However, it would be ideal if the Schottky rectifier has both low forward voltage drop as well as low reverse leakage current. This is impossible to obtain in a LTSS rectifier without making a trade-off between forward voltage drop and the reverse leakage current. In order to overcome this, for the first time, we propose a Lateral Dual Sidewall Schottky (LDSS) rectifier in which the low-barrier sidewall Schottky conducts during forward bias and the high-

barrier sidewall Schottky conducts during the reverse bias. Based on simulation results, we demonstrate that the forward characteristics of the proposed LDSS structure are close to that of the low-barrier LTSS rectifier and the reverse characteristics are close to that of the high-barrier LTSS rectifier resulting in a near ideal Schottky rectifier. The reverse breakdown of the LDSS structure is also very sharp and is similar to that of a PiN diode. In the following sections, we report the results on this unique and highly desired I-V characteristics of the proposed 4H-SiC LDSS rectifier and analyze the reasons for the improved performance.

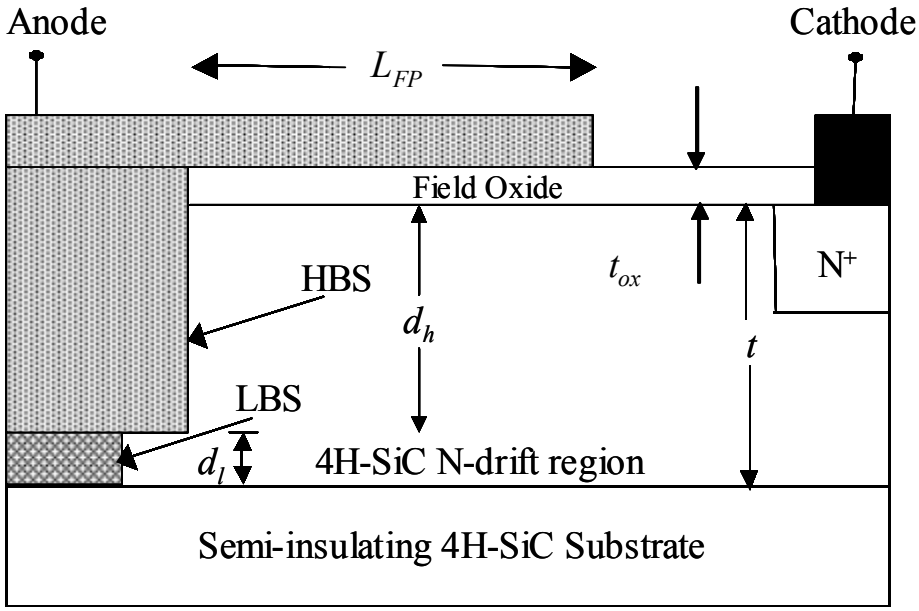


Fig. 2.1 Cross-sectional view of the 4H-SiC Lateral Dual Sidewall Schottky (LDSS).

2.2 LDSS STRUCTURE AND PARAMETERS

Schematic cross-sectional view of the 4H-SiC LDSS rectifier implemented in the 2-dimensional device simulator MEDICI [19] is shown in Fig. 2.1.

The anode of the LDSS rectifier consists of a high barrier Schottky (HBS) metal (Nickel with ϕ_{BH} = 1.50 eV) on top of the low barrier Schottky (LBS) metal (Titanium with ϕ_{BL} = 0.85 eV). These two metals are commonly used in SiC Schottky rectifiers [11]. Electric field crowding at the trench edges is reduced by using a simple field plate termination. The ohmic cathode contact is taken from the N^+ region. To optimize the device parameters, we first fixed the thickness (t), doping (N_D) and drift region length (L) then varied the low-barrier Schottky trench depth (d_l) and high-barrier Schottky trench depth (d_h). The performance of the proposed device (LDSS) in terms of forward voltage drop (@100 A/cm^2) and Reverse Current density (@500 A/cm^2) are tabulated in Table-2.1 for various d_l and d_h. From this Table-2.1, we extracted the optimum value of the low-barrier Schottky trench depth (d_l) as 0.25 μm and the high-barrier Schottky trench depth (d_h) as 1.75 μm.

Table 2.1: Forward voltage drop (@100 A/cm^2) and Reverse current density (@500 A/cm^2) for various d_l and d_h.

d_l (μm)	d_h (μm)	Forward voltage drop @100 A/cm^2	Reverse current density @500 V
0.00	2.00	1.21	6.00E-05
0.25	1.75	0.55	7.15E-05
0.50	1.50	0.55	2.52E-04
0.75	1.25	0.55	5.91E-03
1.00	1.00	0.55	4.25E-02
1.25	0.75	0.55	1.39E-01
1.50	0.50	0.55	2.99E-01
1.75	0.25	0.55	5.05E-01
2.00	0.00	0.55	9.33E-01

t = 2 μm
$N_D = 1\times10^{17}$ /cm^{-3}
L = 5.5 μm
t_{ox} = 0.4 μm
L_{FP} = 4.5 μm
$d_1 + d_h$ = 2 μm = t_{sic}

To extract the optimum value of the field oxide thickness (t_{ox}), breakdown voltage and the reverse current density (@500 A/cm^2) of the proposed device (LDSS) are extracted from the simulation for various values of field oxide thickness and tabulated as shown in Table-2.2. From this Table-2.2, we extracted the optimum value of the field oxide thickness (t_{ox}), which is of 0.4 μm for the highest breakdown voltage.

Table 2.2: Breakdown voltage and Reverse current density (@500 A/cm^2) for various t_{ox}.

Field oxide thickness, t_{ox} (μm)	Breakdown voltage (V)	Reverse Current density @500 A/cm^2
0.1	921	3.83E-05
0.2	933	5.07E-05
0.3	951	6.16E-05
0.4	982	7.15E-05
0.5	960	7.98E-05
0.6	948	8.72E-05
0.7	933	9.42E-05

t = 2 μm
$N_D = 1\times10^{17}$ /cm^{-3}
L = 5.5 μm
L_{FP} = 4.5 μm
d_1 = 0.25 μm
d_h = 1.75 μm

Field plate length (L_{FP}), has been chosen to be of 4.50 μm such that the breakdown voltage of the proposed device is maximum.

The optimized device parameters used in the simulation for the 4H-SiC LDSS rectifier are given in Table-2.3.

Table 2.3: Optimized MEDICI input parameters for the 4H-SiC LDSS rectifier.

Parameter	Value
N^+ doping for ohmic contact	10^{20} cm^{-3}
Drift region doping, N_D	1×10^{17} cm^{-3}
Drift region length, L	5.50 μm
Drift region thickness, t	2.00 μm
Field oxide thickness, t_{ox}	0.40 μm
Field plate length, L_{FP}	4.50 μm
Trench depth, d_h	1.75 μm
Trench depth, d_l	0.25 μm
Low Schottky barrier height (Ti), ϕ_{BL}	0.85 eV
High Schottky barrier height (Ni), ϕ_{BH}	1.50 eV
Richardson constant	140 A/cm^2K^{-2}

2.3 FABRICATION STEPS FOR LDSS RECTIFIER

The dual sidewall Schottky contact can be created in the 4H-SiC LDSS structure as shown in Fig. 2.2. We start with a semi-insulating 4H-SiC substrate with a 2.0 μm n-type 4H-SiC epitaxial layer doped at $N_D = 1\times10^{17}$ cm^{-3}.

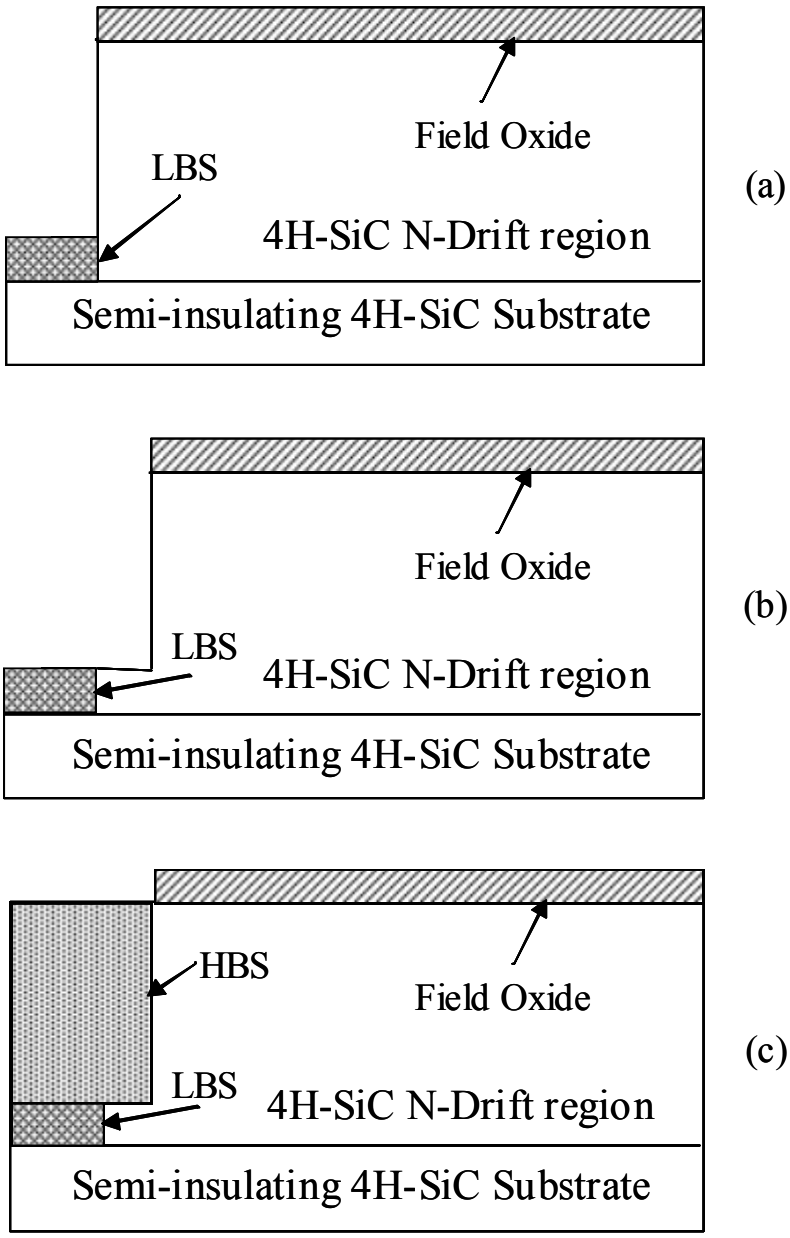


Fig. 2.2 Steps for creating dual metal sidewall Schottky contacts in 4H-SiC LDSS rectifier.

The low-barrier Titanium metal of desired thickness can be first deposited in the trench as shown in Fig. 2.2(a). Using another mask and selective etch process, a second trench is made resulting in the low-barrier Schottky contact as shown in Fig. 2.2(b). Following this step, Nickel can be deposited to form the high-barrier Schottky

contact as illustrated in Fig. 2.2(c). The final structure will be as shown in Fig. 2.1. The proposed 4H-SiC LDSS rectifier is compared with the compatible 4H-SiC Lateral Conventional Schottky (LCS) and the Lateral Trench Sidewall Schottky (LTSS) rectifiers whose structures are similar to those reported in [15].

2.4 SIMULATION RESULTS AND DISCUSSION

2.4 (A) Barrier height lowering model

Simulation of SiC Schottky rectifiers is not easy because the measured reverse current density for 4H-SiC Schottky diodes has been reported to be much higher than predicted by thermionic emission theory and depends strongly on the applied voltage [20]. This discrepancy between measured and estimated reverse leakage current is due to the complex dependence of barrier height on image forces, surface inhomogeneities [21], depletion region generation [12], carrier tunneling [22] and also the barrier height fluctuations. Incorporating all these current flow mechanisms in the thermionic emission model is very difficult primarily because the fundamental physics taking place at the Schottky interface is not well understood. To overcome this problem, Singh and Kumar [11] have proposed a simple empirical model for the barrier height lowering ($\Delta\phi_B$) based on experimental results and have shown its application in two-dimensional simulation of 4H-SiC Schottky rectifiers to accurately predict both the forward and reverse characteristics.

The Singh-Kumar barrier height lowering model [11] for 4H-SiC Schottky structures can be expressed as

$$\Delta\phi_B = a[E_{av}]^{1/2} + b \qquad \text{.....Eq (2.3)}$$

where E_{av} is the average electric field (V/cm) at the Schottky contact and a and b are constants. These constants have been reported to be a = 3.63×10^{-4} $V^{1/2}cm^{1/2}$ and b = -0.034 V for Ti and a = 1.54×10^{-4} $V^{1/2}cm^{1/2}$ and b = 0.638 V for Ni, the metals used in our study. We have implemented the above Singh-Kumar barrier lowering model for 4H-SiC in our 2-D numerical simulation and evaluated the performance of the proposed structure as discussed below.

2.4 (B) Forward and Reverse Characteristics

Fig. 2.3 shows the simulated forward and reverse characteristics of the 4H-SiC low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and the proposed

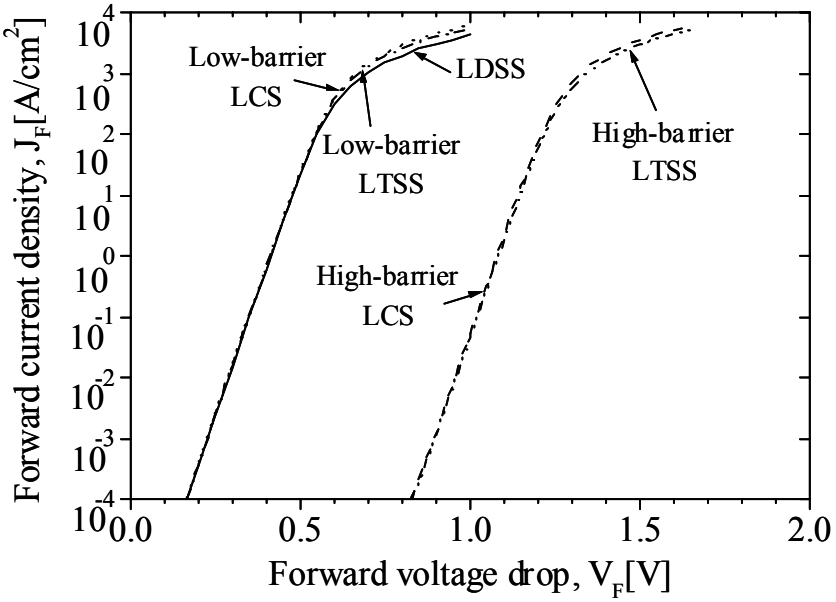


Fig. 2.3 Forward conduction characteristics of the low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and LDSS rectifiers.

LDSS rectifiers. From Fig. 2.3, we observe that the forward characteristic of the LDSS rectifier is close to that of low-barrier LCS or LTSS rectifier as most of the current flows through low-barrier Schottky contact during forward bias as shown by

the current vectors in Fig. 2.4. The forward voltage drop of the proposed LDSS structure is approximately 0.55 V at a current density of 100 A/cm^2.

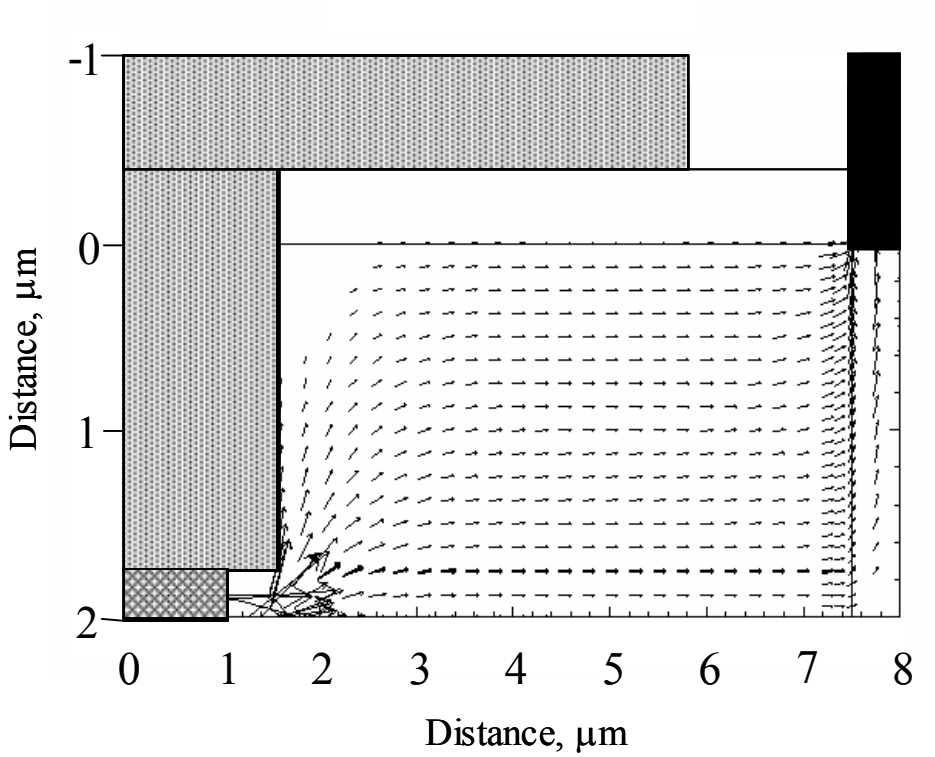


Fig. 2.4 Current flow vectors in the LDSS rectifier at a forward current density of 100A/cm^2.

As it is clear from Fig. 2.4 that low-barrier Schottky metal in the proposed device (LDSS) plays a key role under forward bias.

From Fig. 2.5, we note that the reverse leakage current of the LDSS rectifier is very low and is close to that of the high-barrier LCS and LTSS rectifiers. This is because during the reverse bias the low-barrier Schottky is shielded by the depletion region and most of the reverse current flows through the high-barrier Schottky contact.

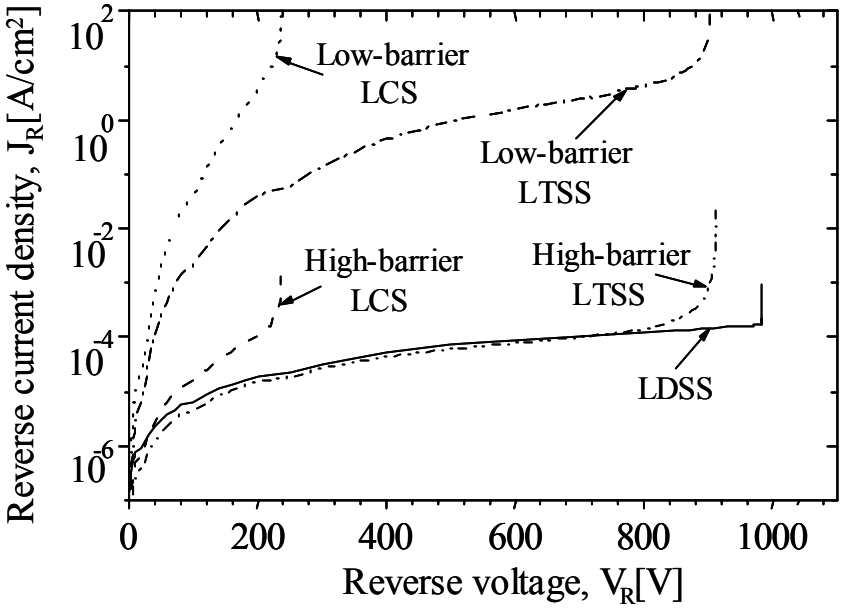


Fig. 2.5 Reverse blocking characteristics of the low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and LDSS rectifiers.

This is because during the reverse bias the low-barrier Schottky is shielded by the depletion region and most of the reverse current flows through the high-barrier Schottky contact. This can be seen from the reverse current vectors of the LDSS rectifier shown in Fig. 2.6. We also note that the reverse current of both the low-barrier and high-barrier LCS rectifiers increases very rapidly with increasing reverse voltage resulting in an extremely soft breakdown at 230 V. However, the breakdown voltage of the LDSS rectifier is very large at ~ 1000 V (more than four times the breakdown voltage of LCS rectifiers.). This is because the breakdown of the LDSS

structure takes place below the right edge of the field plate (away from the Schottky contact) [15].

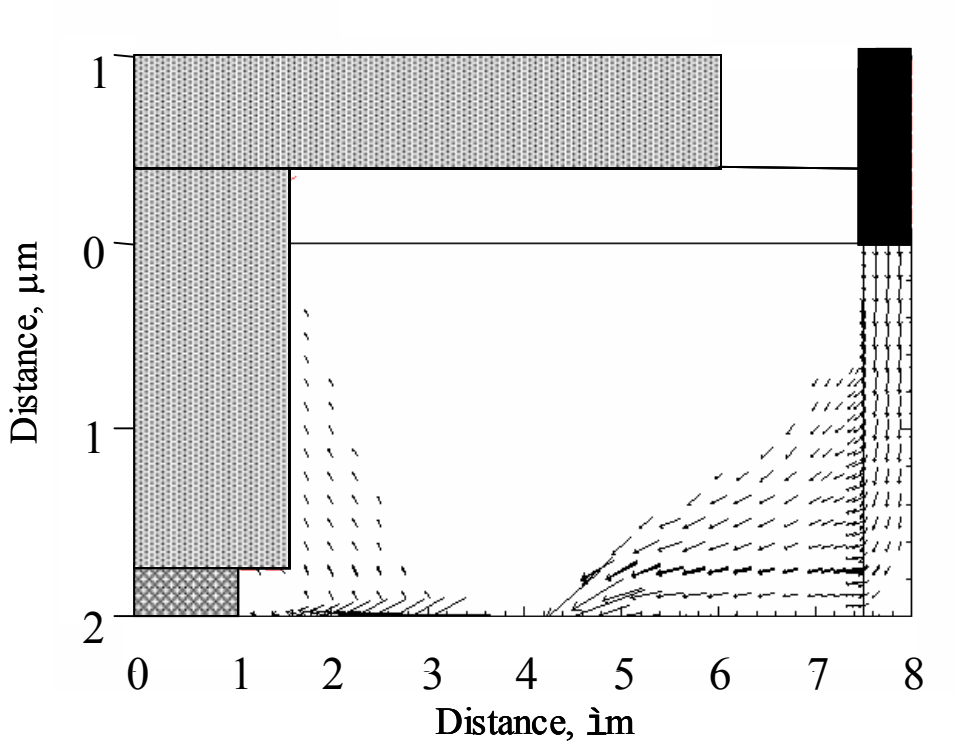


Fig. 2.6 Current flow vectors in the LDSS rectifier
At a reverse bias of 500 V.

To understand this behavior, the electric field is plotted in Fig. 2.7 along the horizontal line at the field-oxide / 4H-SiC interface of low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and LDSS rectifiers near the breakdown voltage of the LCS rectifier (230 V). We note from Fig. 2.7 that in the case of low-barrier and high-barrier LCS rectifiers, the peak electric field occurs at the Schottky junction resulting in a large barrier lowering as shown in Fig. 2.8. This leads to a soft and low breakdown in the case of low-barrier and high-barrier LCS rectifiers.

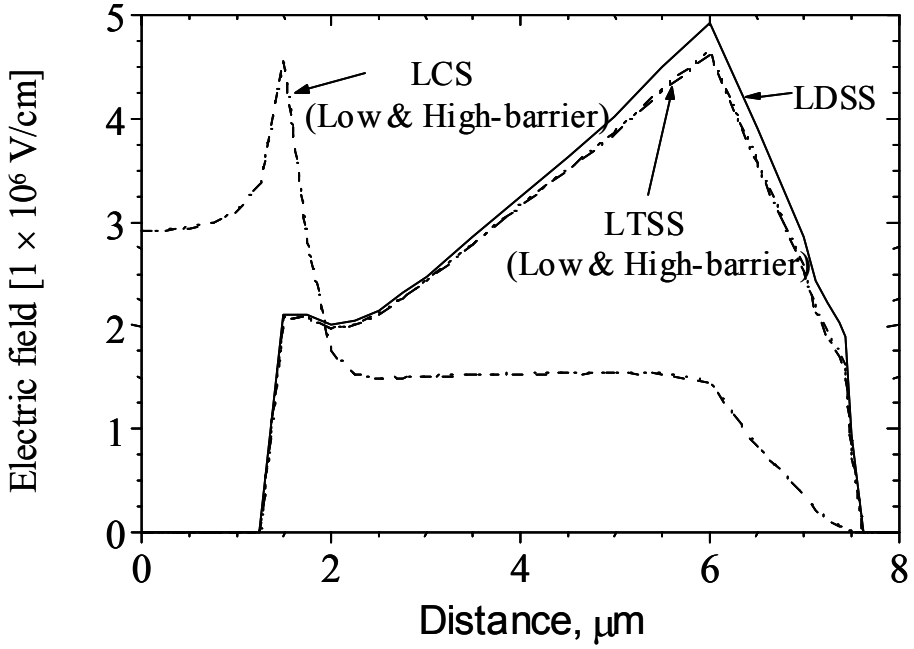


Fig. 2.7 Electric field variation along the horizontal line at the field-oxide / 4H-SiC interface of low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and LDSS rectifiers near its breakdown voltage.

But, the proposed LDSS structure exhibits a very sharp breakdown similar to that of a PiN diode in spite of using only Schottky junctions in the structure.

This is due to the reduced electric field at the Schottky contact which in turn results in a significantly diminished barrier lowering ($\Delta\phi_B$) for the LDSS structure as shown in Fig.2.8.

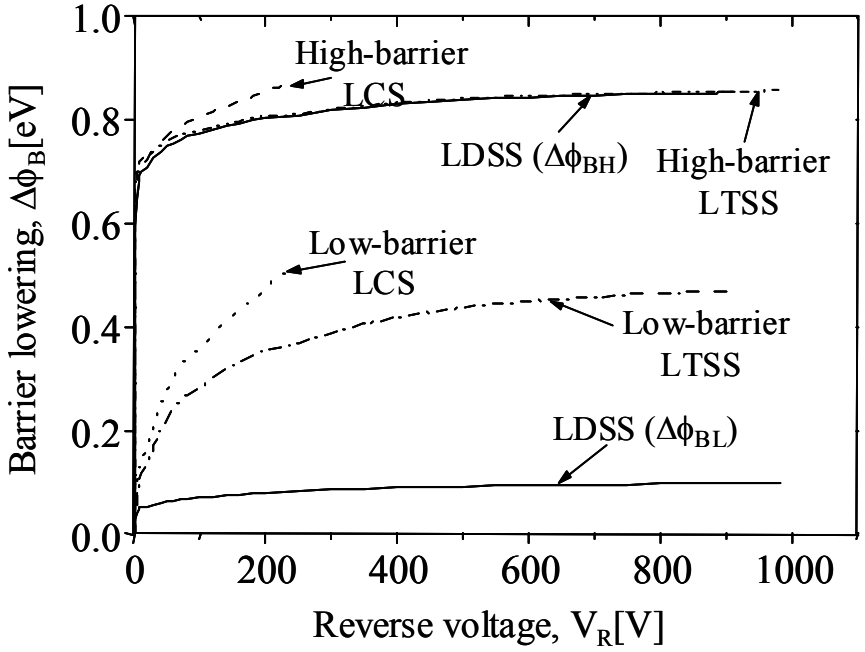


Fig. 2.8 Barrier height lowering as a function of reverse bias voltage for the low-barrier and high-barrier LCS, low-barrier and high-barrier LTSS and LDSS rectifiers.

A useful figure of merit for rectifiers which combines the current carrying capability under forward bias and blocking capability under reverse bias, is the on/off current ratio [20] defined at fixed forward (1 V) and reverse biases (–500 V). Taking the *J-V* characteristics into consideration, the calculated on/off current ratio for the LDSS rectifier is of about 5.5×10^7 at 1 V/-500 V for an epitaxial layer doping of $1\times10^{17}/cm^3$, which is same as the on/off current ratio obtained by considering the forward characteristic of the low-barrier LTSS and reverse characteristic of the high-barrier LTSS. In other words, the LDSS structure combines the benefits of the low-barrier LTSS and high barrier LTSS rectifiers resulting in an ideal Schottky rectifier.

2.5 CONCLUSION

A novel high-voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) rectifier has been presented. Using 2-dimensional simulation, we have demonstrated that the forward characteristic of the proposed LDSS rectifier is close to that of a low-barrier LTSS rectifier and its reverse characteristic is close to that of a high-barrier LTSS rectifier, resulting in an on/off current ratio of 5.5×10^{7}. An interesting feature of the proposed LDSS rectifier is that it exhibits a sharp breakdown similar to that of a PiN diode in spite of using only Schottky junctions in the LDSS structure. The combined low forward voltage drop, low reverse leakage current and excellent reverse blocking capability make the proposed LDSS rectifier attractive for use in low-loss, high-voltage and high-speed power IC applications.

Chapter 3

Application of Lateral Dual Sidewall Schottky (LDSS) Concept for Improved Rectifier Performance on SOI

3.1 INTRODUCTION

SiC is a special material and still has problems with regard to the quality of the epitaxial films. However, silicon is a well understood material and it is not very difficult to get high quality silicon films on SOI. Therefore, to generalize the Lateral Dual Sidewall Schottky (LDSS) concept and to examine how a silicon based LDSS structure performs, we have studied the implementation of the LDSS rectifier on SOI. Based on simulation results, we demonstrate that the forward characteristics of the proposed LDSS rectifier on SOI are close to that of the low-barrier Lateral Trench Sidewall Schottky (LTSS) rectifier and its reverse characteristics are close to that of the high-barrier Lateral Trench Sidewall Schottky (LTSS) rectifier. The detailed analysis and the reasons for the improved performance of the proposed LDSS rectifier on SOI are presented by comparing its performance with the compatible Lateral Conventional Schottky (LCS) and Lateral Trench Sidewall Schottky (LTSS) rectifiers [15] on SOI in the following sections.

3.2 DEVICE STRUCTURE AND PARAMETERS

Cross sectional view of the proposed Lateral Dual Sidewall Schottky (LDSS) rectifier on SOI implemented using two dimensional device simulator MEDICI [19] is shown in Fig. 3.1.

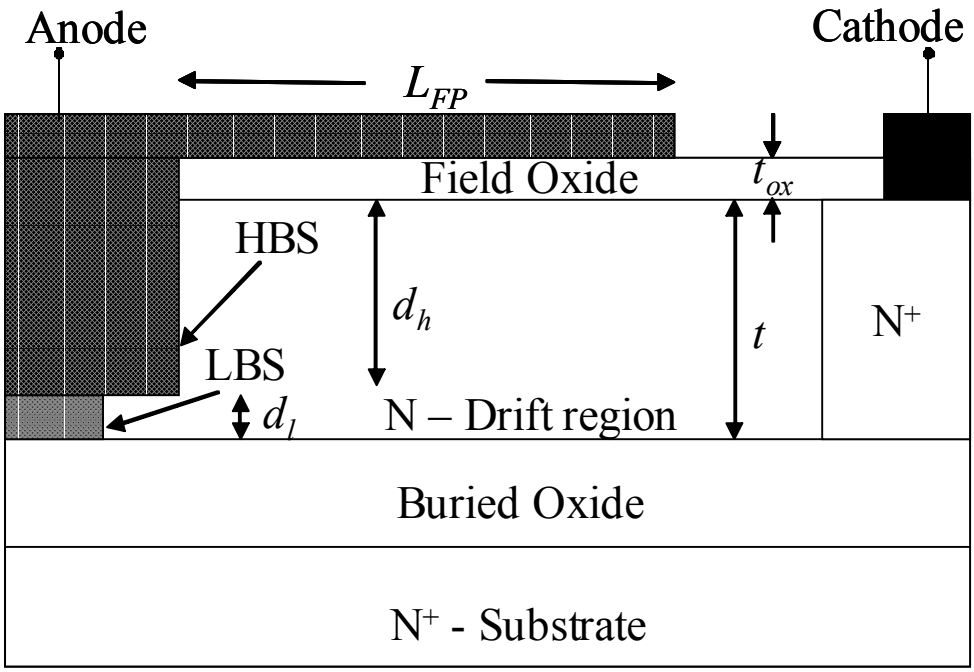


Fig. 3.1 Cross sectional view of the proposed Lateral-
-Dual Sidewall Schottky (LDSS) rectifier on SOI.

The anode consists of both the low-barrier Schottky contact as well as high-barrier Schottky contact. Nickel (ϕ_{BL} = 0.57 eV) is chosen for the low-barrier Schottky contact and Tungsten (ϕ_{BH} = 0.67 eV) is chosen for high-barrier Schottky contact as these two are the well studied and most commonly used metals for Schottky contacts. The cathode contact is taken from the N^+ region. Field plate with a length of 3.5 μm is used to avoid the electric field crowding at the Schottky contact. Drift region doping (N_D) is chosen to be 5×10^{16} cm^{-3} and its thickness is 0.5 μm. Field oxide thickness is 0.2 μm and buried oxide thickness is 2 μm. High-barrier Schottky trench depth is chosen to be 0.4 μm and low barrier Schottky trench depth is chosen to be 0.1 μm as this combination gives the low forward voltage drop as well as less reverse leakage current. Most of these parameters are chosen based on the works reported in the literature [15].

Fabrication procedure for making lateral dual sidewall Schottky contacts is same as that discussed in chapter 2.

3.3 SIMULATION RESULTS AND DISCUSSION

Fig. 3.2 shows the simulated forward IV characteristics of the proposed Lateral Dual Sidewall Schottky (LDSS) rectifier on SOI and is compared with the compatible Lateral Conventional Schottky (LCS) and Lateral Trench Sidewall Schottky (LTSS) rectifiers on SOI.

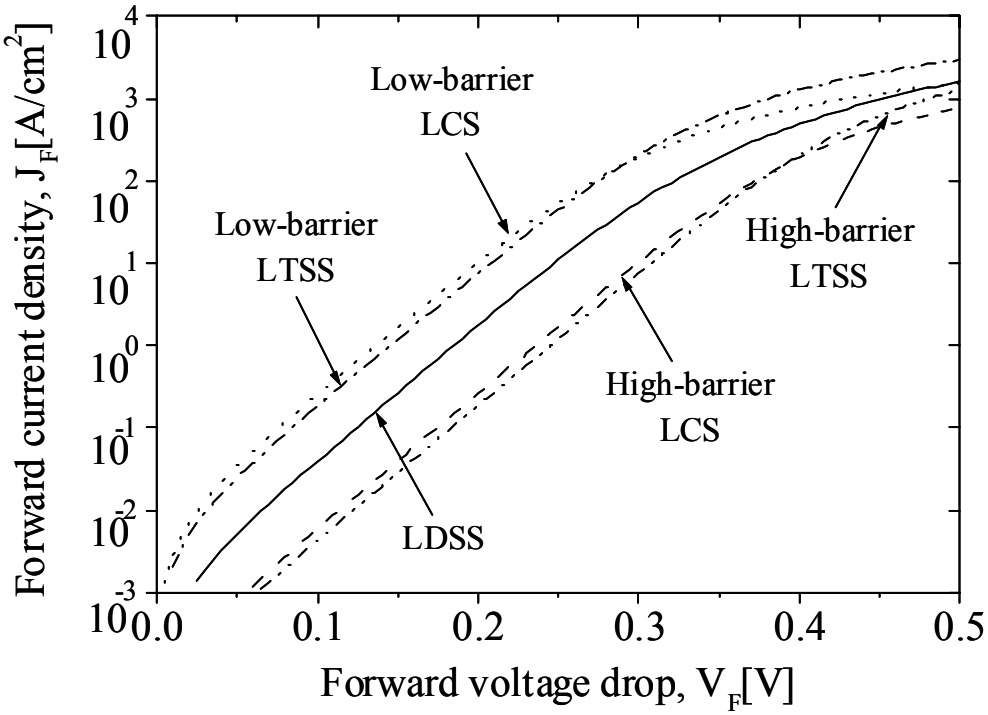


Fig. 3.2 Forward IV characteristics of the proposed LDSS rectifier and is compared with LCS and LTSS rectifiers.

It can be observed from the figure that the forward characteristic of the proposed LDSS rectifier is close to that of low-barrier LCS and LTSS rectifiers as low-barrier Schottky contact plays an essential role in providing most of its current.

Simulated reverse IV characteristics of the proposed LDSS rectifier on SOI and its compatible Lateral Conventional Schottky (LCS) and Lateral trench Sidewall Schottky (LTSS) rectifiers on SOI are shown in Fig. 3.3.

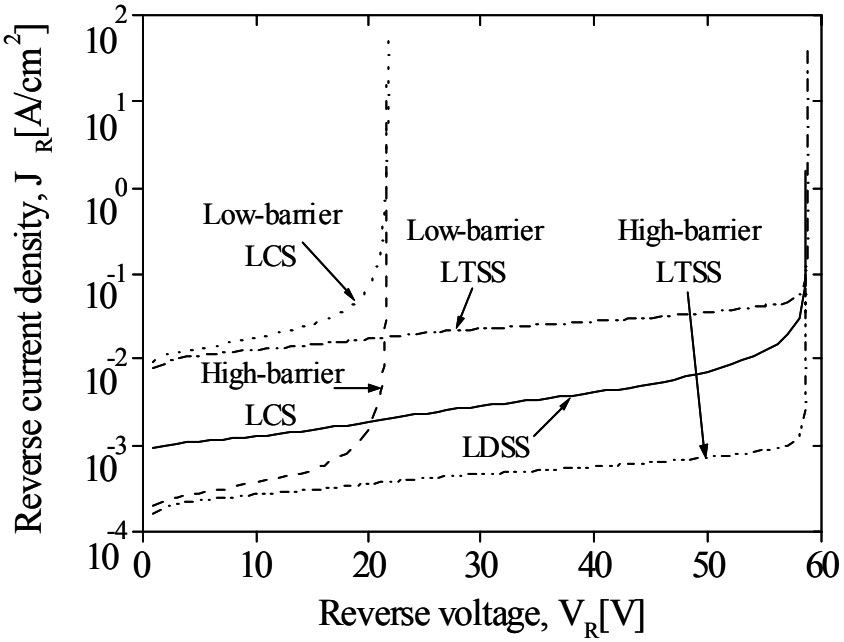


Fig. 3.3 Reverse IV characteristics of the proposed LDSS rectifier and is compared with LCS and LTSS rectifiers.

From the above figure, we can observe that low-barrier and high-barrier LCS rectifiers exhibit a lower breakdown voltage due to large peak electric field at the Schottky contact as shown in Fig. 3.4 where as low-barrier and high-barrier LTSS rectifiers exhibit higher breakdown voltage. This improvement is due to the shifting of peak electric field from Schottky contact to the field plate edge [15] as shown in the Fig. 3.4. Further, it can be observed that the reverse leakage current of both the low-barrier LCS and LTSS rectifiers is quite high as compared to high-barrier LCS and LTSS rectifiers.

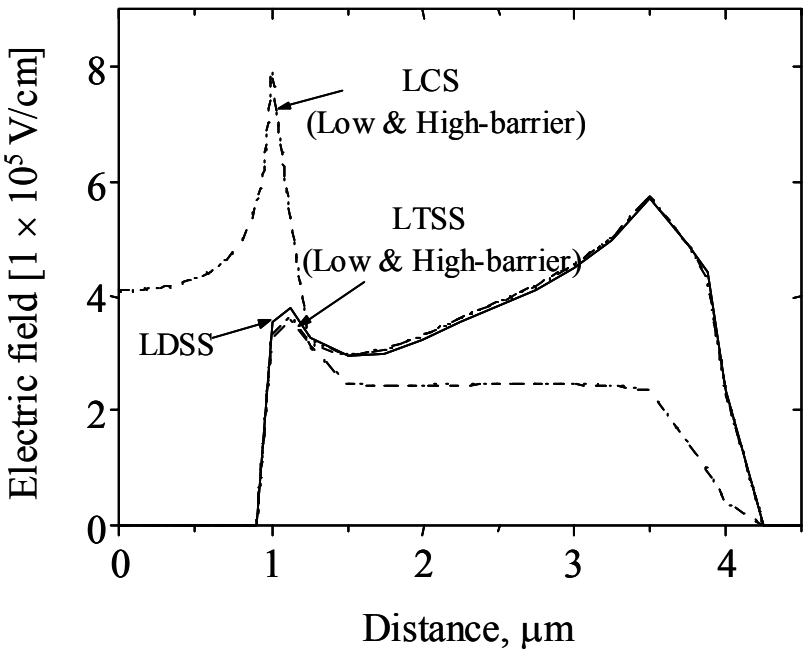


Fig. 3.4 Electric field variation along the horizontal line at the Si/SiO_2 interface of LCS, LTSS and LDSS rectifiers near the breakdown voltage.

The reverse leakage current of the proposed LDSS rectifier on SOI is close to that of high-barrier LCS and LTSS rectifiers as the low-barrier Schottky metal of the proposed LDSS rectifier is pinched off and high-barrier Schottky alone is responsible for the current conduction during the reverse bias.

3.4 CONCLUSION

From our simulation analysis we conclude that the proposed Lateral Dual Sidewall Schottky (LDSS) rectifier on SOI behaves as a low-barrier Lateral Trench Sidewall Schottky (LTSS) rectifier on SOI and it behaves as a high-barrier Lateral Trench Sidewall Schottky (LTSS) rectifier on SOI under reverse bias conditions which makes it to achieve both the low forward voltage drop as well as less reverse leakage current. The combined low forward voltage drop, less reverse leakage current and excellent reverse blocking capability make the proposed LDSS rectifier attractive for use in high-speed and low-loss power IC applications.

Chapter 4

2D-Simulation and Analysis of Lateral SiC N-emitter SiGe P-base Schottky Metal-collector (NPM) HBT on SOI

4.1 INTRODUCTION

Due to its excellent material properties such as wide bandgap, high thermal conductivity, high saturated electron drift velocity and ability to operate at high temperatures [23–25], silicon carbide (SiC) is an attractive choice in many applications such as military, satellite and intelligent control systems. Device designers have started recognizing the utility of SiC as an emitter in HBTs to take the full advantages of its excellent material properties together with its fabrication compatibility with silicon. In the past, several structures were reported in literature [18, 26] with SiC as emitter in HBTs. But all these were vertical in nature and not compatible with standard CMOS processes so they could not gain wider acceptability in VLSI BICMOS applications.

SiGe is a promising semiconductor for the applications involved in high speed circuits such as RF circuits (PAs, LNAs, modulators, mixers, VCOs …etc.), mixed signal circuits (Analog to digital converters, digital to analog converters, fractional N synthesizers …etc.) and in the precision analog circuits (Op Amps, bandgap references, temperature bias control and current mirrors). In the literature, several SiGe HBTs were reported with the above advantages.

While the SiC/Si and SiGe/Si based HBTs have several advantages, they also suffer from many non-ideal effects such as base widening at high collector currents and excessive base storage time. To overcome this problem, one can use a Schottky

collector either as a vertical structure [16] or as a lateral structure on SOI [17]. However, to combine the advantages of SiC and SiGe with the combination of SOI technology and lateral Schottky collector, for the first time, we propose a novel SiC emitter SiGe base lateral NPM Schottky collector HBT. To the best of our knowledge this is the first work to suggest the integration of SiC emitter SiGe base, lateral Schottky collector and SOI for BiCMOS applications providing an incentive for further experimental exploration.

We evaluated the performance of the proposed NPM HBT and its equivalent NPN HBT and NPM BJT structures using two-dimensional device simulator ATLAS [27]. From our simulation results, we observe that the proposed NPM HBT exhibits improved performance in terms of high current gain, high cut-off frequency, suppressed Kirk effect, ability to operate at high temperatures and excellent transient response (with almost zero base storage time) over its compatible NPN HBT and NPM BJT structures. The proposed device structure, a feasible fabrication process compatible with BiCMOS process, steady state and dynamic behavior analysis are presented in the subsequent sections.

4.2 PROPOSED DEVICE STRUCTURE AND ITS PARAMETERS

Top and cross-sectional view of the proposed NPM HBT (SiC emitter SiGe base lateral Schottky collector HBT), implemented in the two-dimensional device simulator ATLAS [27] is shown in Fig. 4.1. The emitter SiC region can be formed by well defined lateral growth processes [28-31]. The base region is converted into SiGe using Ge implantation. The Schottky metal collector is at the right edge of the base. A highly doped P^+-poly is deposited on the p-type SiGe base region to take the base contact.

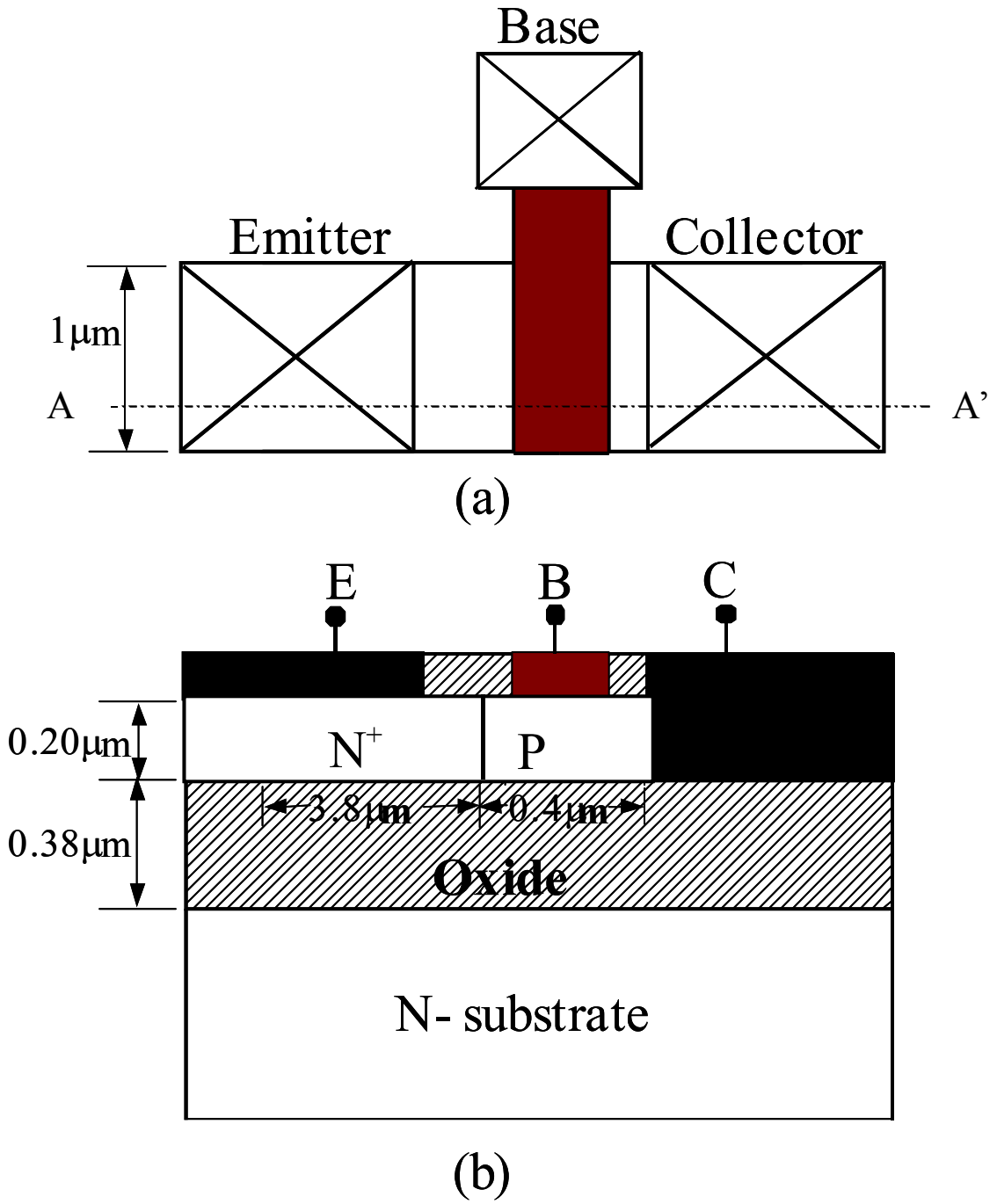


Fig. 4.1 (a) Top and (b) cross-sectional view of the proposed NPM HBT (SiC emitter SiGe base lateral Schottky collector HBT on SOI).

Palladium silicide is chosen for the Schottky collector as it gives the highest barrier height (0.7 eV) with p-type SiGe (20% Ge) as reported in the literature [32–33] based on experimental results. The proposed NPM HBT is compared with compatible NPN HBT and NPM BJT devices, which have exactly the same dimensions and impurity profiles of the proposed NPM HBT except that to make the comparison more effective we set the collector doping of the NPN HBT to be $2\times10^{17}cm^{-3}$ such that collector breakdown voltage BV_{CEO} matches approximately with that of NPM HBT for zero base current. The compared NPN HBT is same as that of the proposed NPM HBT except that its collector is of silicon material. The compared NPM BJT is same as that of proposed NPM HBT except that its emitter and base are of silicon material.

Table 1: ATLAS input parameters for the proposed NPM HBT, NPN HBT and NPM BJT.

Parameter	Value
SOI thickness t_{si} (Initially)	0.20 μm
Buried oxide thickness t_{box}	0.38 μm
Field oxide thickness t_{ox}	0.18 μm
Emitter length	3.80 μm
Base length	0.40 μm
Emitter region doping concentration	$5x10^{19}$ cm^{-3}
Base region doping concentration	$5x10^{17}$ cm^{-3}
Collector region doping concentration (Only for NPN HBT)	$2x10^{17}$ cm^{-3}
Barrier height lowering coefficient	$2.0x10^{-7}$ cm
SRH concentration parameter for electrons and holes NSRHN and NSRHP(Both for Si and SiGe)	$1x10^{22}$ cm^{-3}

The ATLAS [27] input parameters for the proposed NPM HBT and those of the compatible NPN HBT and NPM BJT are listed in table. 1. These parameters are chosen based on reported experimental results for lateral bipolar transistors on SOI [8].

4.3 FABRICATION STEPS FOR THE PROPOSED NPM HBT

We start with an SOI wafer having a p-type epitaxial layer of 0.2 μm thickness and a doping of 5 x 10^{17} cm^{-3}. We first deposit a thick CVD oxide and pattern as shown in Fig. 4.2(a). In the next step, we epitaxially grow the n^+ SiC on the vertical edge (at point A in Fig. 4.2(b)) of the silicon surface which acts as a seed for the lateral growth of SiC [28-31] as shown in Fig. 4.2(b). Subsequent to this step, CMP process is performed and then by depositing a thick CVD oxide, it is patterned as shown in Fig. 4.2(c). Following this step, a nitride film is deposited as shown in Fig. 4.2(d) and is etched using an unmasked RIE etch such that a nitride spacer is retained at the vertical edge of thick CVD oxide as shown in Fig. 4.2(e). Next, a thick CVD oxide is deposited as shown in Fig. 4.2(f) and by using CMP process, the surface is planarized. After this step, the nitride spacer is removed with selective etching to create a window in the oxide as shown in Fig. 4.2(g). To create the SiGe base region, we now need to implant Ge through this window. It has been shown in literature [34-37] that Ge implantation is a useful technique to create SiGe regions. Energies in the range of 130 KeV and fluences of the order of 3 x 10^{16} cm^{-2} can be used for this purpose. This needs to be followed by a rapid thermal annealing for at least 10 s to recrystallize the amorphous SiGe region [37]. In our simulations we have assumed a maximum Ge concentration of 20% which is the maximum limit for most practical applications [38-39].

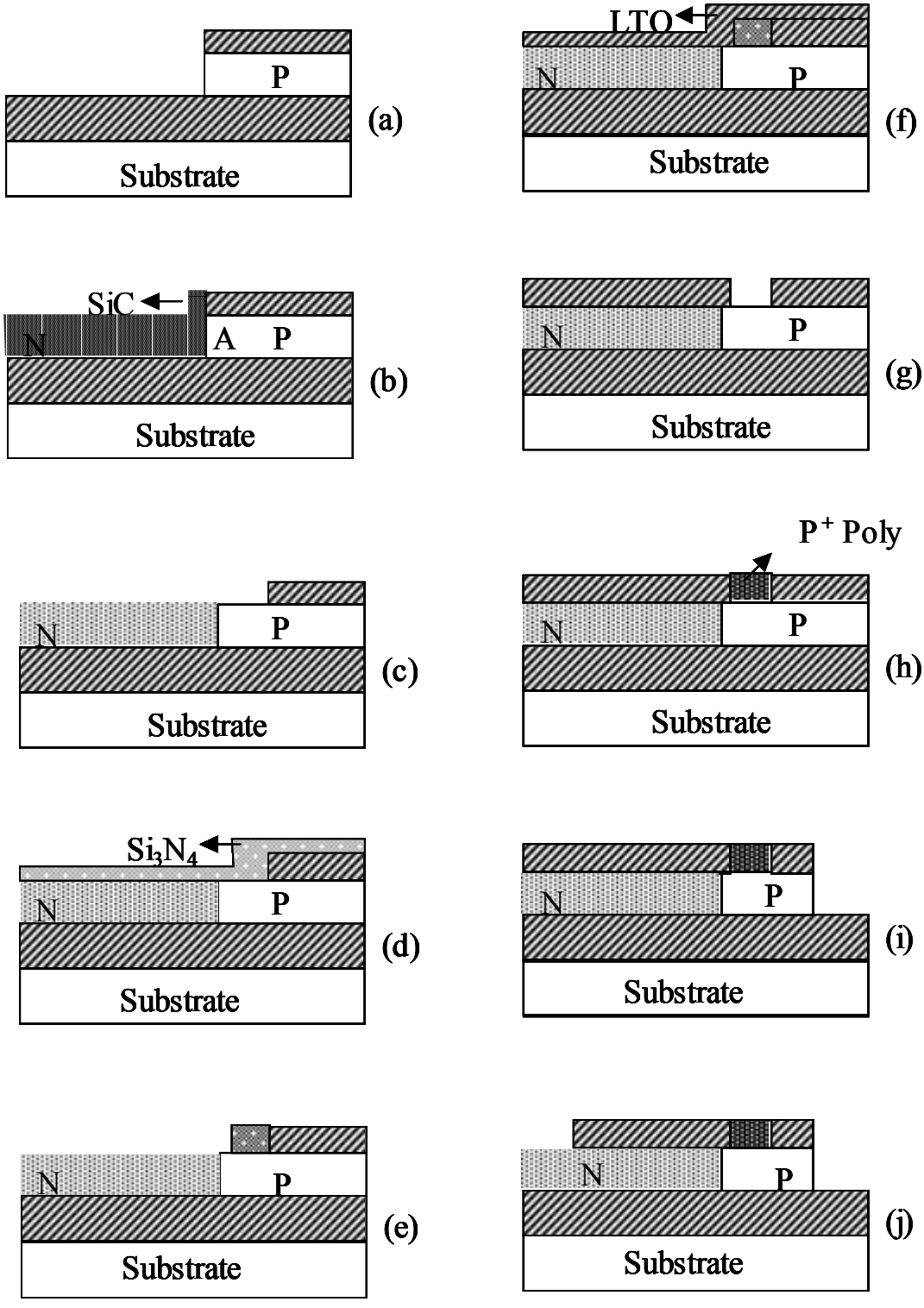


Fig. 4.2 Fabrication steps for the proposed NPM HBT.

After converting, silicon in the base region to SiGe, we then deposit p^+-poly. Next, by using CMP process, the wafer is once again planarized. At the end of this step, only p^+ - poly will be present in the window as shown in Fig. 4.2(h). Following this step, a contact window is opened for metal Schottky collector as shown in Fig. 4.2(i) and subsequent to this step, n^+ emitter contact window is opened as shown in Fig. 4.2(j). Finally, palladium silicide is deposited to form the Schottky collector contact and ohmic contacts on the emitter and p^+-poly base region. The final structure appears as shown in Fig. 4.1(b).

4.4 SIMULATION RESULTS AND DISCUSSION

To explore the performance of the proposed NPM HBT (SiC emitter SiGe base lateral Schottky collector HBT), we used the two-dimensional device simulator ATLAS [27]. We incorporated suitable physical models such as concentration dependent mobility, field dependent mobility, bandgap narrowing, Shockley-Read-Hall, Auger recombination models and Klassens mobility model in the simulator to evaluate the performance of the proposed device. For the carrier statistics purpose, we used the Fermi-Dirac distribution. To account for the deep donor (N_D) and deep acceptor (N_A) levels in SiC emitter, we used the incomplete ionisation model. Standard thermionic emission model is incorporated including image force barrier lowering phenomenon [27] for the Schottky collector junction. Electrical properties of SiC are taken from the reported works in the literature [40]. The performance of the proposed NPM HBT compared with NPN HBT and NPM BJT is presented below in detail.

4.4 (A) DC Performance:

Fig. 4.3 shows the simulated common-emitter output characteristics of the proposed NPM HBT (SiC emitter SiGe base lateral Schottky collector HBT) and its equivalent devices (NPN HBT and NPM BJT). As can be observed from the figure, the proposed NPM HBT shows high collector current for a given base current as compared to those of NPN HBT and NPM BJT which will result in a large transconductance. The proposed NPM HBT however shows a collector offset voltage which is more than that of the NPN HBT and NPM BJT structures. Collector offset voltage is commonly seen in the HBTs due to the bandgap offset [41] and in Schottky collector transistors due to the Schottky junction [42]. Since the proposed structure includes both the hetero junction on the emitter side and the Schottky junction on the collector side, its collector offset voltage is expected to be larger than that of NPN HBT and NPM BJT and this should be taken into account in the digital logic circuit design.

The Gummel plot of the proposed NPM HBT, NPN HBT and NPM BJT for a fixed collector emitter voltage (V_{CE} = 1 V) is plotted in Fig. 4.4. We can see from the figure that the NPM BJT shows high currents as compared to the proposed NPM HBT and NPN HBT because of low cut-in voltage which can be best observed from the band diagrams drawn at thermal equilibrium as shown in Fig. 4.6. An interesting point is that the base current of the proposed NPM HBT is less than that of the NPN HBT even at high–level injection of carriers which clearly shows the suppression of the Kirk effect [43] in the proposed NPM HBT.

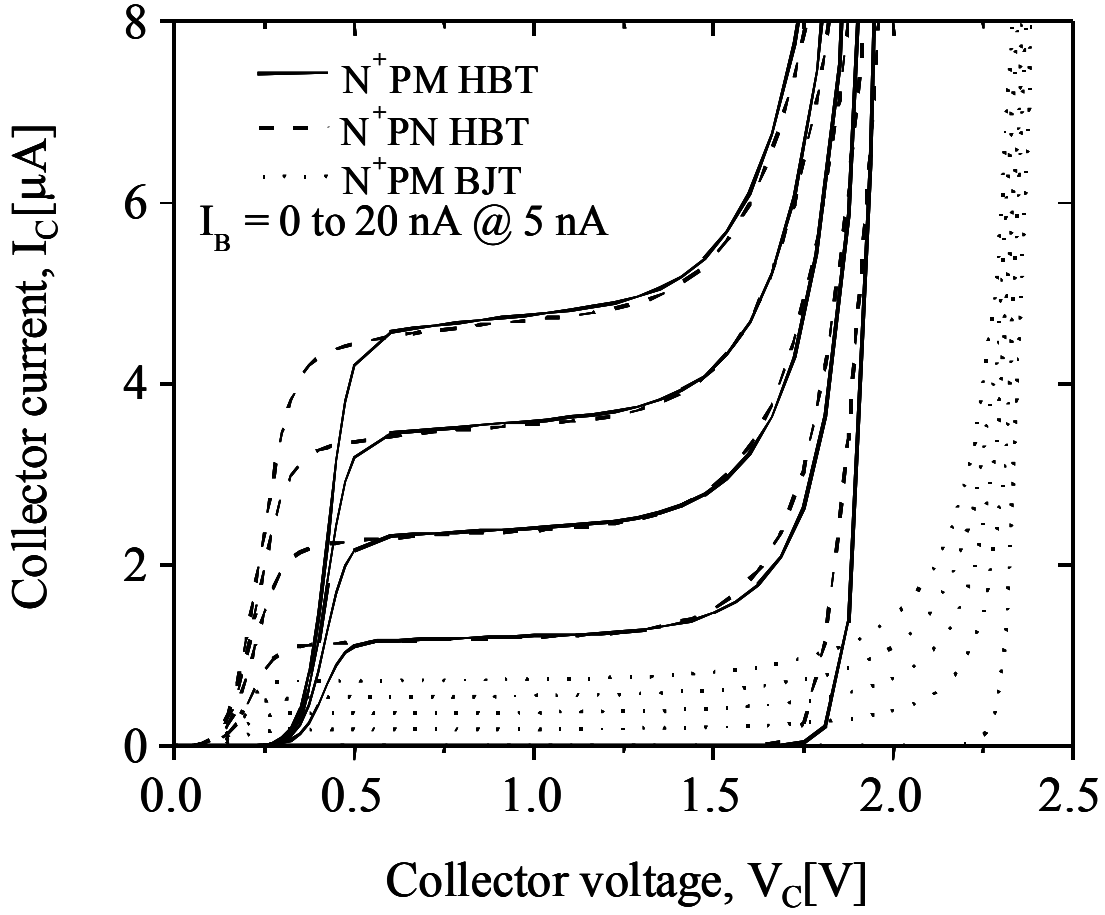


Fig. 4.3 Common-emitter IV – characteristics of the proposed NPM HBT compared with NPN HBT, NPM BJT.

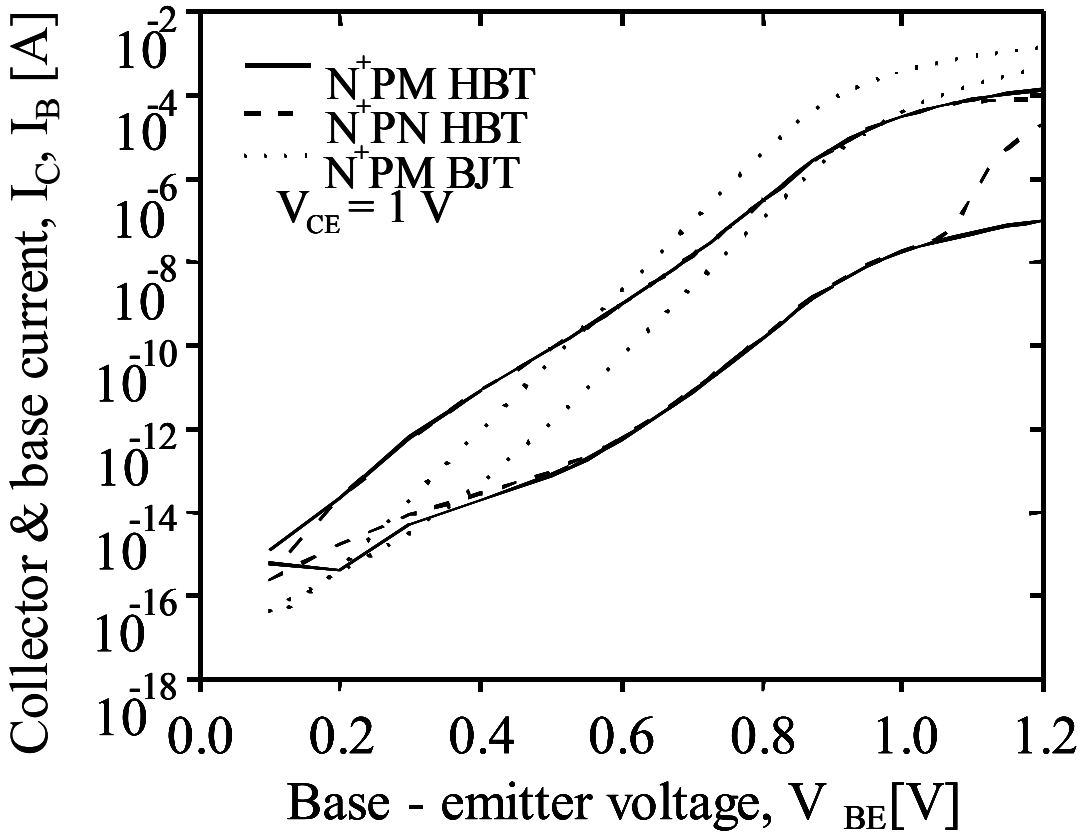


Fig. 4.4 Gummel plot of the proposed NPM HBT compared with NPN HBT, NPM BJT for a fixed collector emitter voltage (V_{CE} = 1 V).

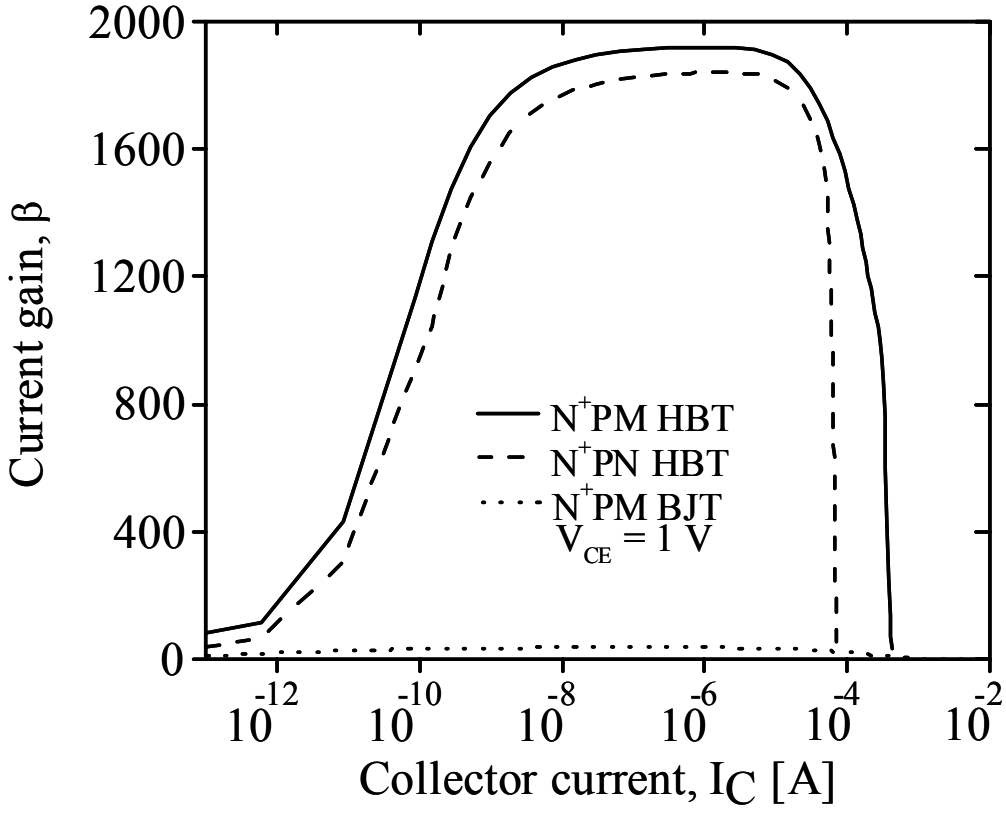


Fig. 4.5 Gain versus collector current characteristics of the proposed NPM HBT compared with those of NPN HBT, NPM BJT for a fixed collector emitter voltage (V_{CE} = 1 V).

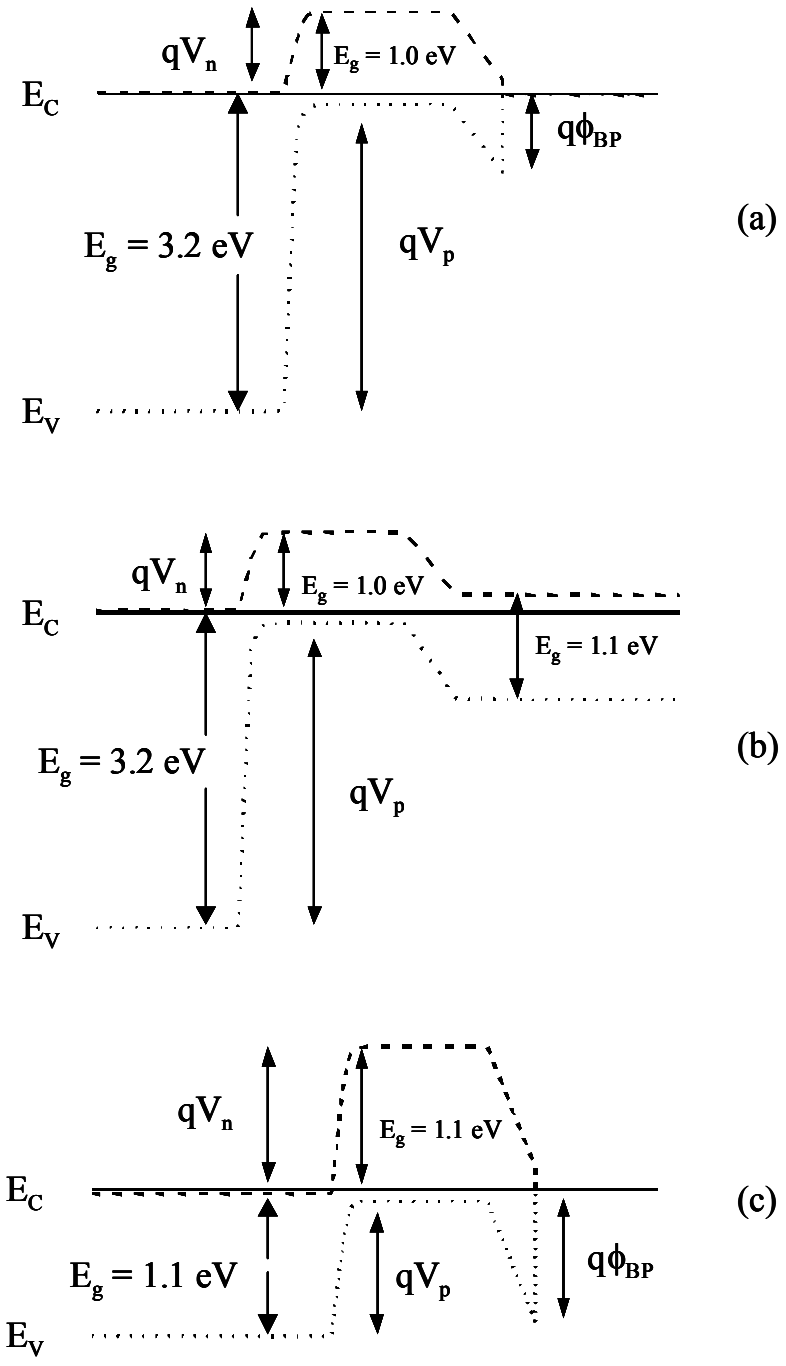


Fig. 4.6 Band diagrams drawn at thermal equilibrium
(a) Proposed NPM HBT, (b) NPN HBT and (c) NPM BJT.

Fig. 4.5 shows the gain versus collector current of the NPM HBT which is compared with that of NPN HBT and NPM BJT. As it is clear from the figure, the gain of the proposed NPM HBT and NPN HBT is very high compared to that of NPM BJT due to the high emitter injection efficiency because of differing barrier heights for electrons and holes as shown in Fig. 4.6. Further, the gain of the proposed NPM HBT is more than that of NPN HBT because of the proficient collection of minority carriers by the metal collector injected into the base. The NPM HBT can also operate at higher collector currents than the NPN HBT because of the metal collector.

We have also investigated the effect of base doping on peak gain and breakdown voltage BV_{CEO} (for zero base current) for various germanium concentrations in the base (SiGe) for the proposed NPM HBT. Fig. 4.7 shows the peak gain versus base doping for various germanium concentrations in the base (SiGe) of the proposed NPM HBT. It can be observed from this figure that the peak gain decreases as we decrease the germanium concentration in the base (SiGe) for a given base doping and the gain also decreases as we increase the base doping for a given Ge concentration because of low emitter injection efficiency. Fig. 4.8 shows the breakdown voltage BV_{CEO} (for zero base current) versus base doping for various germanium concentrations in the base (SiGe) of the proposed NPM HBT. We observe from this figure that for a given base doping, the breakdown voltage BV_{CEO} (for zero base current) increases as we decrease the germanium concentration and for a given Ge concentration, the breakdown voltage increases as we increase the base doping which can be easily understood from the current gain variation shown in Fig. 4.7.

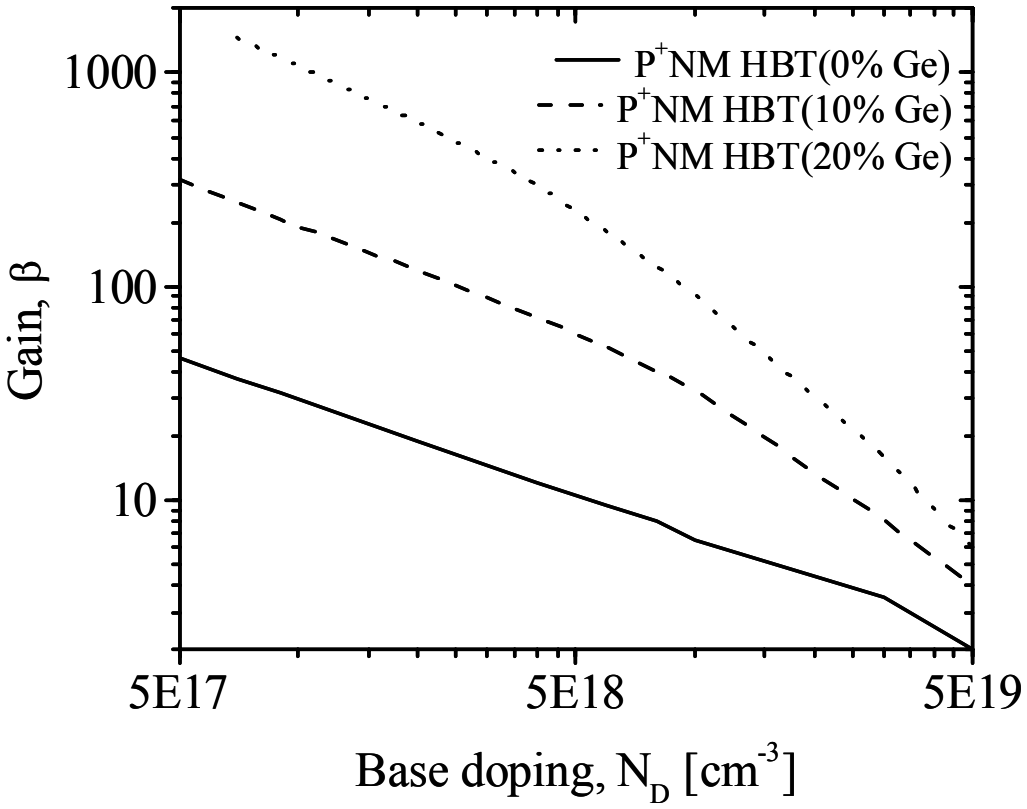


Fig. 4.7 Gain versus base doping for various germanium concentrations in the base (SiGe) of the proposed NPM HBT.

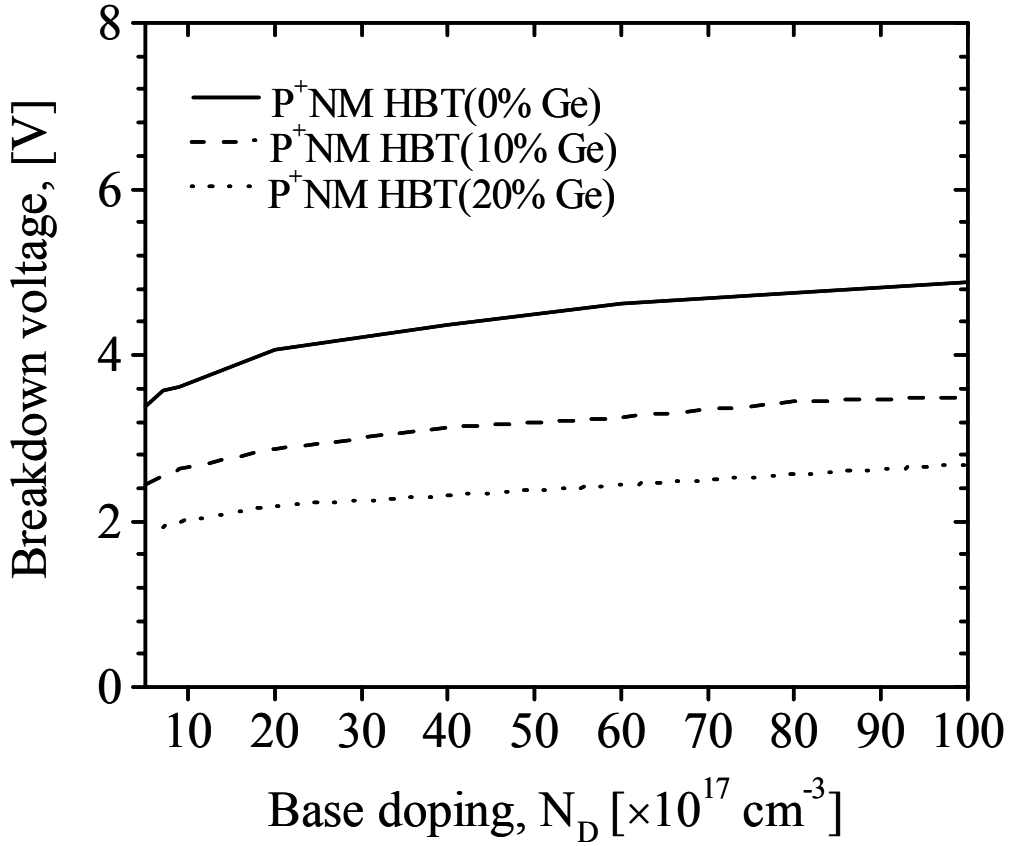


Fig. 4.8 Breakdown voltage BVCEO (for zero base current) Versus base doping for various germanium concentrations in the base (SiGe) of the proposed NPM HBT.

4.4 (B) Dynamic Behaviour Analysis:

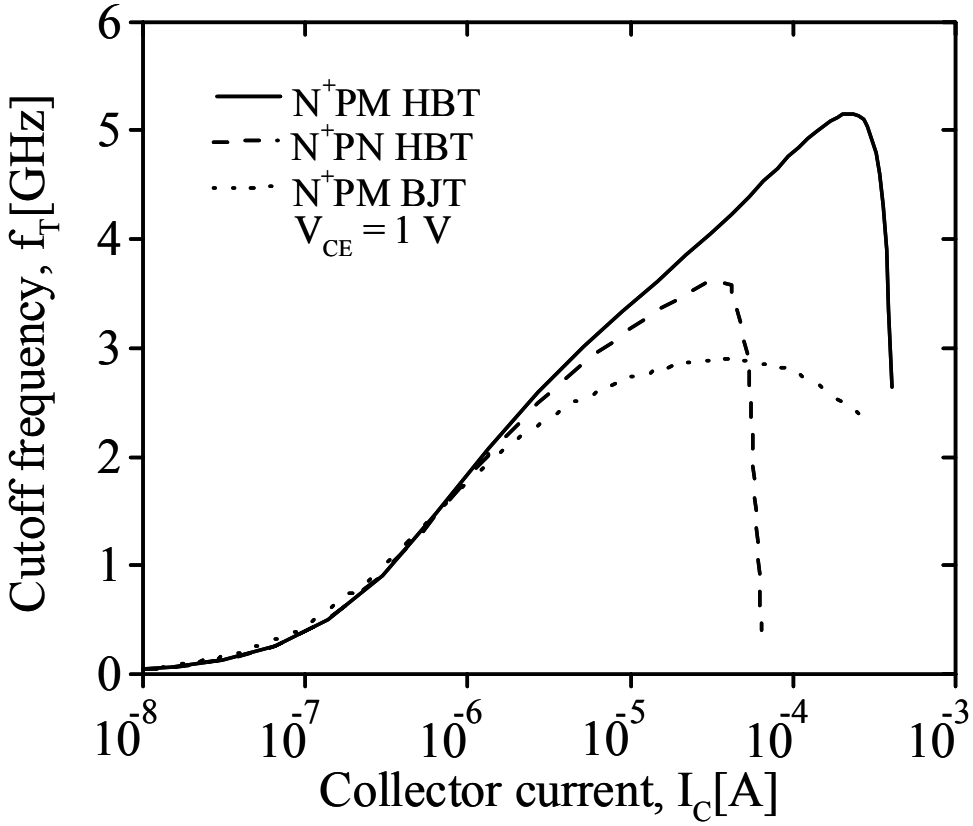


Fig. 4.9 Unity gain cut-off frequency versus collector current of the proposed NPM HBT and its counterparts (NPN HBT and NPM BJT).

Fig. 4.9 shows the unity gain cut-off frequency versus collector current of the proposed NPM HBT (SiC emitter SiGe base lateral Schottky collector HBT) and is compared with NPN HBT, NPM BJT. For the cut-off frequency calculation, we have used the model given in ATLAS [27]. As can be observed, the cut-off frequency of the proposed NPM HBT is higher than those of NPN HBT and NPM BJT due to its metal collector and higher transconductance $g_{m.}$ The proposed NPM HBT exhibits an f_T of 5.2 GHz at a collector current of 0.2 mA, whereas for the comparable NPN HBT and NPM BJT, f_T falls to a negligible value at the above current due to Kirk effect and decrease in transconductance.

Fig. 4.10 shows the transient behaviour of the proposed NPM HBT which is compared with NPN HBT and NPM BJT structures. It is clear that the proposed NPM HBT and NPM BJT show excellent transient response with nearly zero base charge storage time due to its metal collector and suppressed Kirk effect while NPN HBT shows a higher storage time due to the Kirk effect and also the electron pile-up at the collector-base hetero-junction.

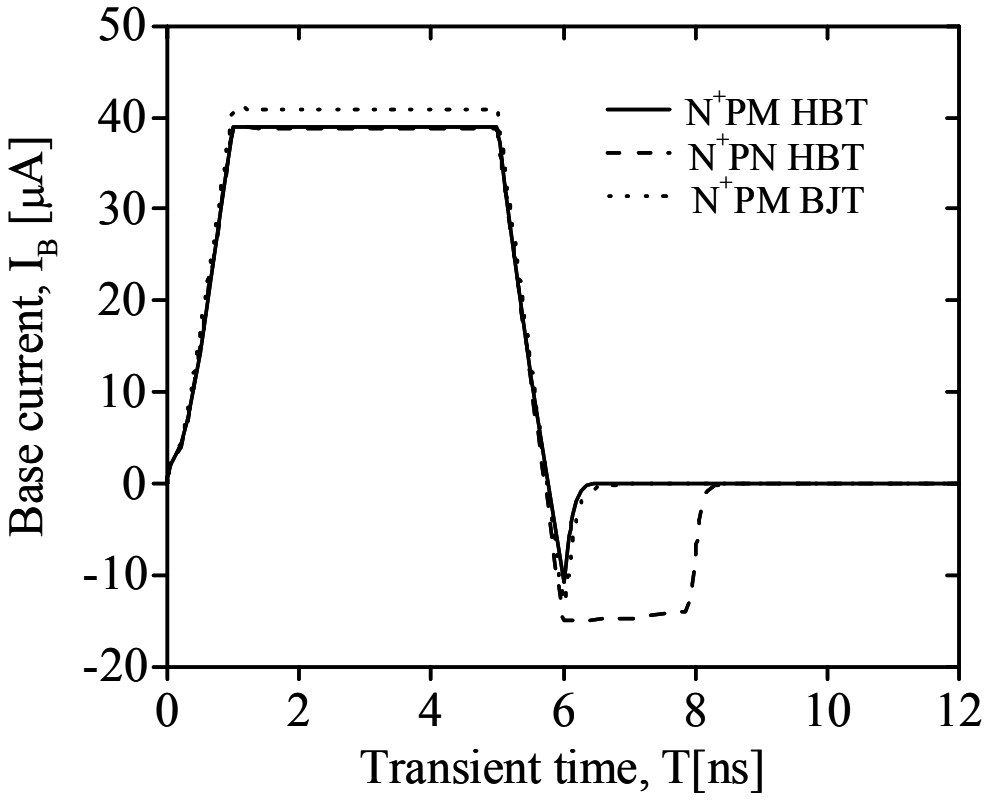


Fig. 4.10 Transient behaviour of the proposed NPM HBT which is compared with NPN HBT and NPM BJT.

4.4 (C) Performance at High Temperature:

Fig. 4.11 shows the gain versus collector current for various temperatures of the proposed NPM HBT which is compared with NPN HBT. As the temperature increases gain decreases which is in excellent agreement with the results reported experimentally for vertical SiC emitter HBT [40]. Further, it can be observed in spite of the Schottky collector, the NPM HBT exhibits a higher current gain (917) as compared to the NPN HBT (860) which is a clear indication of its ability to operate at high temperatures.

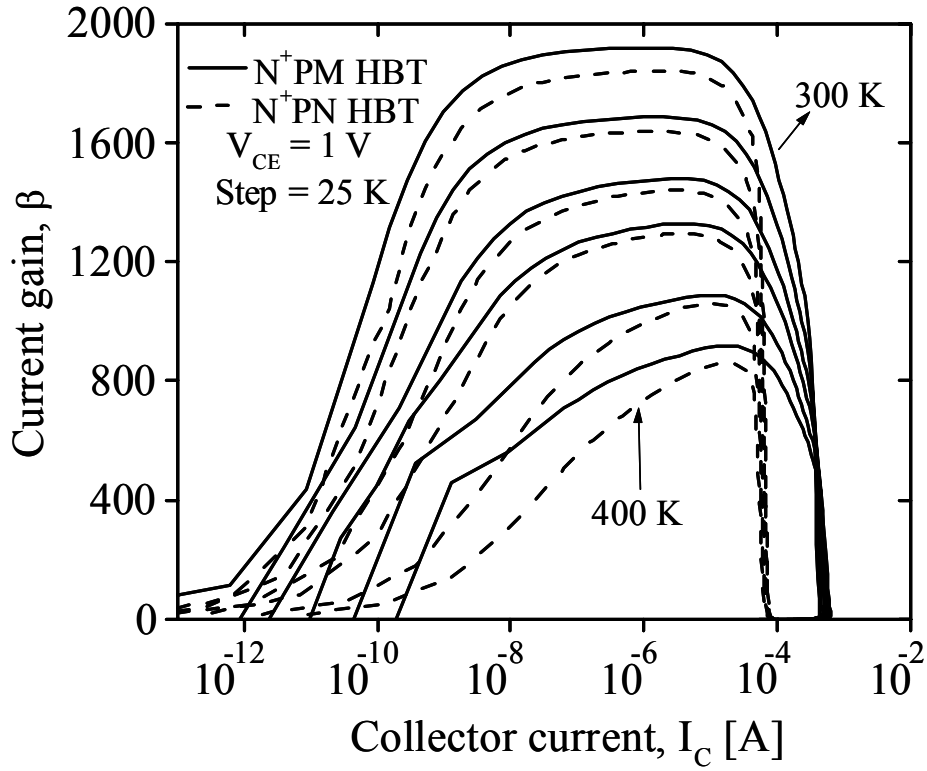


Fig. 4.11 Gain versus collector current for various temperatures of proposed NPM HBT and NPN HBT.

4.5 CONCLUSION

A thorough investigation of the proposed SiC emitter SiGe base lateral Schottky collector HBT has been presented. We conclude from our study that the proposed NPM HBT exhibits superior performance in terms of high current gain, high cut-off frequency, suppressed Kirk effect and excellent transient response (with almost zero base storage time) over its counterparts (NPN HBT and NPM BJT). Its excellent transient response is expected to result in a reduced power-delay product. The proposed NPM HBT finds applications in BiCMOS compatible high current-driving circuits and high speed circuits such as RF, mixed signal and in precision analog circuits.

In many analog applications, compatible wide-bandgap emitter PNP HBTs are also required. In the following chapter, we examine why it is difficult to realize wide-bandgap emitter PNP HBTs and also suggest a novel method to overcome the difficulties in realizing such a structure.

Chapter 5

A New Lateral Dual – bandgap P-Emitter N-SiGe base Schottky Metal-collector (PNM) HBT on SOI with Reduced Collector-Emitter Offset Voltage.

5.1 INTRODUCTION

Wide bandgap emitter bipolar transistors have several advantages over their homo-junction counterparts, such as (i) large current gain independent of emitter doping, (ii) increased base doping against current gain trade-off and (iii) high speed operation [23-25]. A wide bandgap emitter BJT can be realized either by reducing the base region bandgap with respect to the emitter or by increasing the emitter region bandgap with respect to the base. SiGe HBTs are an excellent example of wide bandgap emitter BJTs which have become very attractive in high speed applications due to their superior performance [38-39]. In the recent past, SiC as an emitter has also been shown to be a potential candidate for making wide bandgap emitter BJTs [18, 26 & 44]. While other wide bandgap HBT technologies based on compound semiconductors such as InGaP/GaAs or AlGaAs/GaAs are available, HBTs based on SiC/Si are attractive because of their compatibility with the silicon technology and the excellent properties of SiC. In spite of a large lattice mismatch, wide bandgap SiC emitter hetero-bipolar transistors with large current gains have been successfully reported [18, 26 & 44]. However, wide bandgap emitter HBTs exhibit a finite collector-emitter offset voltage, $V_{CE(offset)}$ [45-46] due to the large difference in the built-in potential of emitter-base and collector-base junctions. This is detrimental in many digital applications and should be minimized while retaining the advantages of the wide bandgap emitter.

A survey of literature reveals that only NPN wide bandgap SiC emitter transistors have been reported. Often, in many applications, compatible PNP transistors with wide bandgap SiC P-emitters are required. However, this is not possible because, as we shall demonstrate in the following section, SiC emitter PNP transistors are highly prone to the collector-emitter offset-voltage problems than the wide bandgap SiC emitter NPN transistors. If the $V_{CE(offset)}$ problem is eliminated in SiC wide bandgap emitter PNP transistors, they will find wide usage in many applications. To the best of our knowledge, no solution has yet been reported on how $V_{CE(offset)}$ can be minimized in wide bandgap emitter PNP transistors.

The aim of this chapter is therefore to propose for the first time a novel method of minimizing the $V_{CE(offset)}$ in SiC wide bandgap emitter PNP transistors. We suggest that by making use of a dual-bandgap material consisting of SiC over Si in the emitter region will reduce the $V_{CE(offset)}$ without significantly affecting the current gain. We used numerical simulation to verify the efficacy of our solution to minimize $V_{CE(offset)}$. In our simulations, we have chosen a lateral experimental BJT structure on SOI to implement our solution. We will also demonstrate that the use of SiGe base and a Schottky collector in the proposed structure will further enhance the transistor performance making it a suitable candidate for high speed BiCMOS applications involving compatible NPN and PNP transistors with wide bandgap SiC-emitters. We also have suggested in the end a possible fabrication procedure for the device using well established fabrication steps for lateral BJTs. It may be pointed out that the actual fabrication will not be without its problems. However, we believe that the proposed structure may provide significant incentive for experimental exploration considering the importance of wide bandgap emitter PNP transistors in many circuit applications.

5.2 COMPARISON OF $V_{CE(OFFSET)}$ PROBLEM IN WIDE BANDGAP EMITTER NPN/PNP HBTs

The collector-emitter offset voltage is defined as the difference between the turn-on voltage of the emitter-base (EB) and base-collector (BC) junctions [47]:

$$V_{CE(offset)} = V_{EB} - V_{BC} \text{ at } I_C = 0 \text{ mA}. \quad \text{(eq. 5.1)}$$

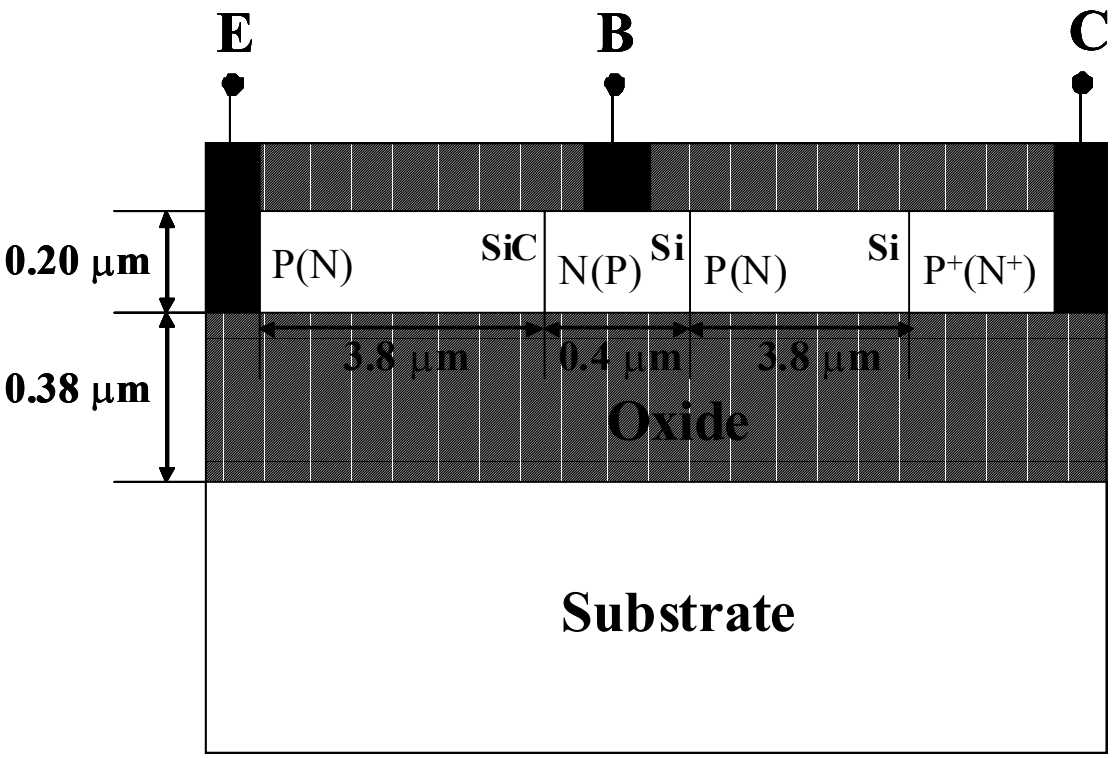


Fig. 5.1 Cross-sectional view of the wide bandgap SiC emitter lateral PNP/NPN HBT.

In order to compare the collector-emitter off-set problem in wide bandgap PNP/NPN HBTs, we have chosen a lateral HBT structure as shown in Fig. 5.1 in which the emitter region is SiC, base and collector regions are silicon. The epitaxial film thickness of the HBT is chosen to be 0.2 μm and the buried oxide thickness is 0.38 μm. Emitter is doped at 5×10^{19} cm^{-3}. Base width is 0.4 μm and its doping is chosen to be 5×10^{17} cm^{-3}. Collector is doped at 2×10^{17} cm^{-3}. All these parameters are chosen based on reported experimental results of lateral silicon NPN BJTs [8].

The collector-emitter offset problem of SiC emitter PNP HBTs can be best understood from Fig. 5.2 in which the emitter-base (EB) and base-collector (BC) junction diode characteristics are shown.

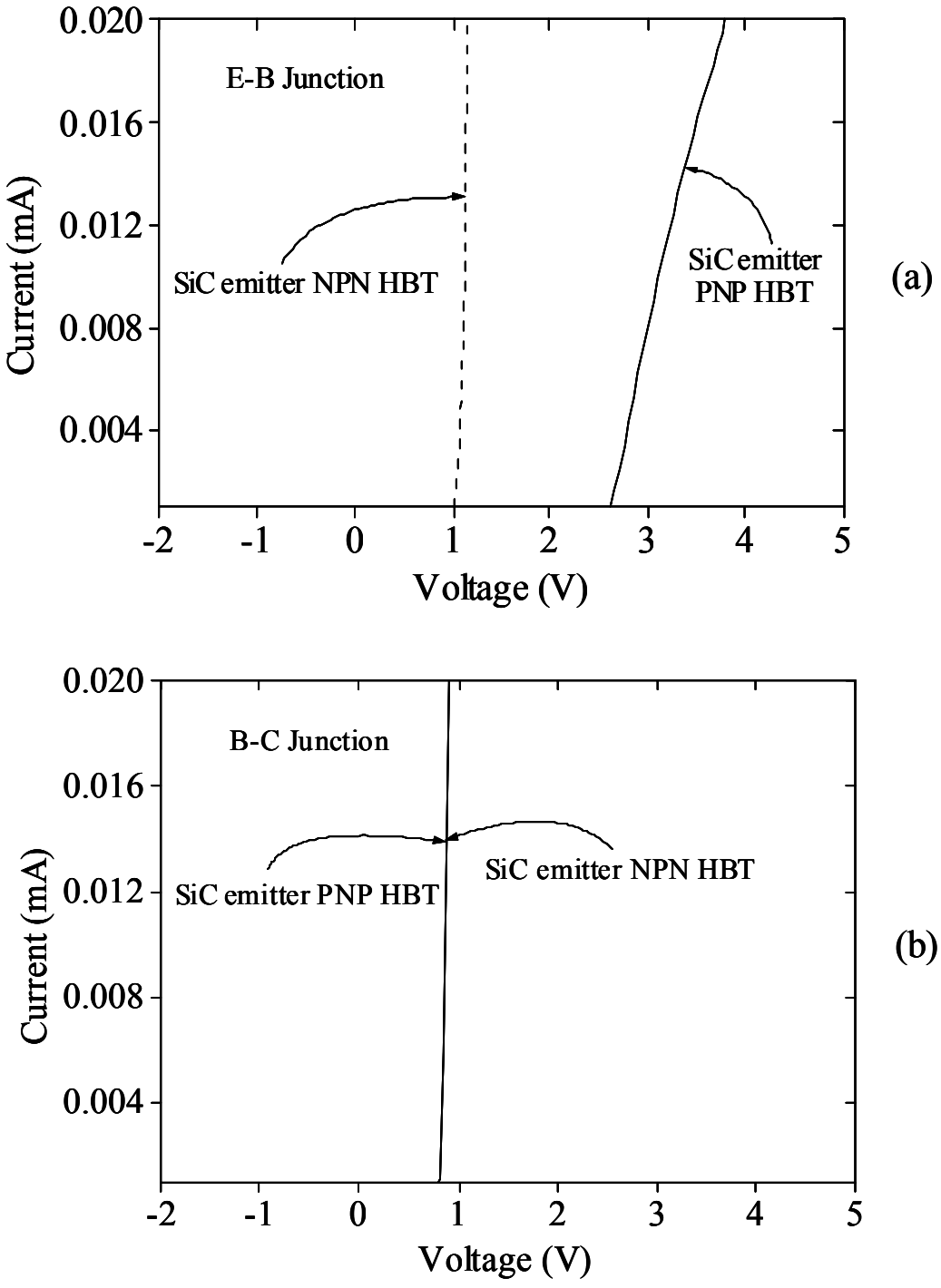
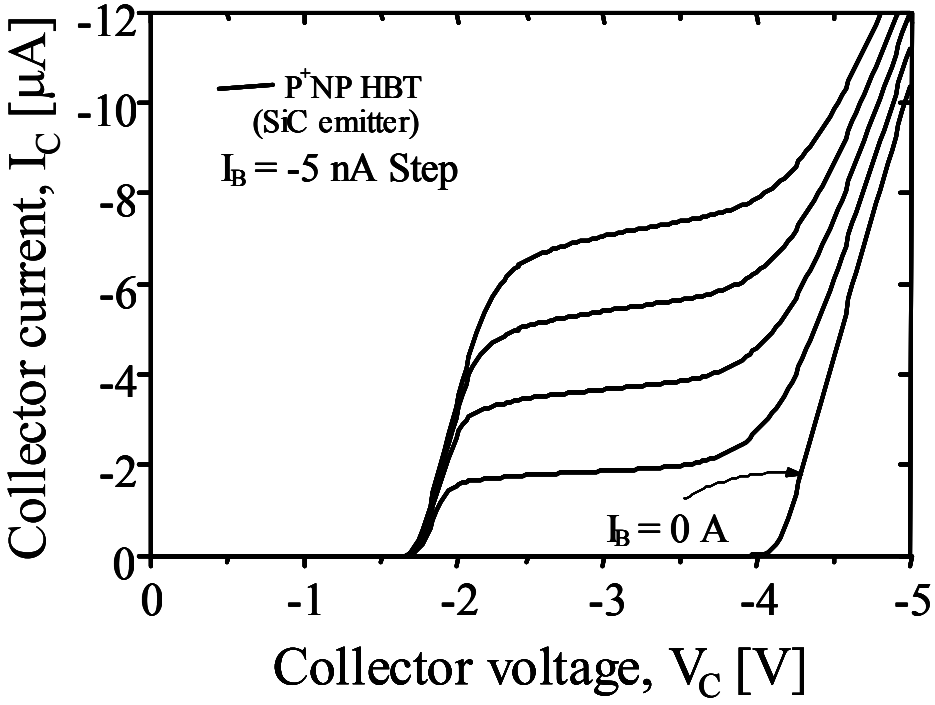
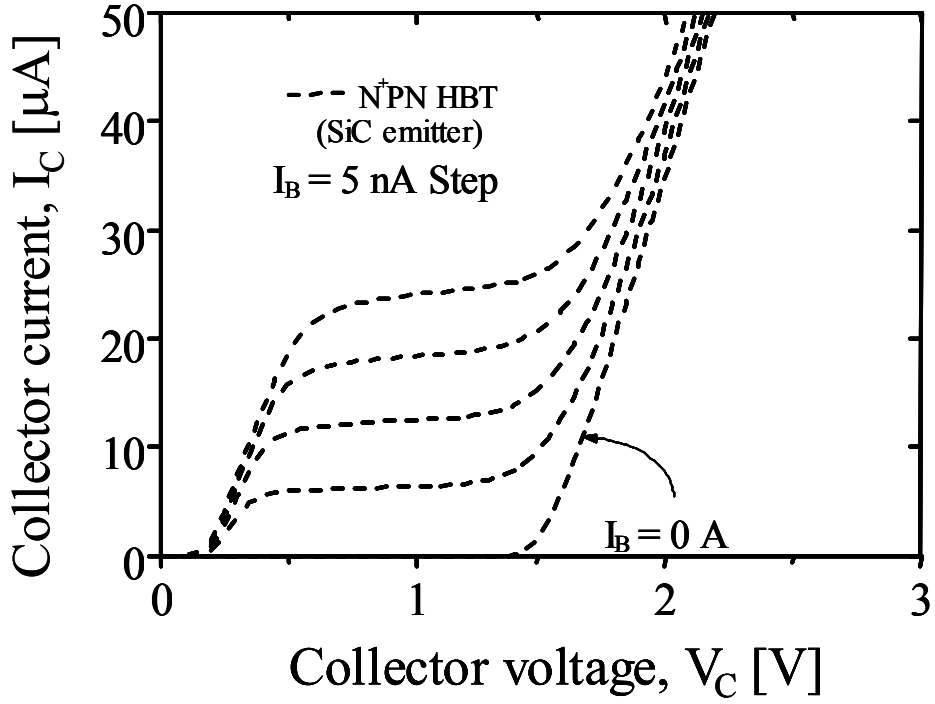


Fig. 5.2 (a). E-B and (b). B-C diode characteristics of the SiC emitter NPN HBT and SiC emitter PNP HBT.

Fig. 5.2(a) shows that the turn on voltage V_{EB} for emitter-base junction of the PNP SiC emitter HBT is 1.5 V larger than that of the emitter-base junction of the NPN SiC emitter HBT. On the other hand the turn on voltage V_{BC} of the collector-base junction for both the SiC emitter PNP/NPN HBTs is identical (~ 0.8 V) as shown in Fig. 5.2(b) since silicon is used for both the base and collector regions. The output characteristics of the PNP and NPN wide bandgap SiC emitter HBTs are shown in Fig. 5.3. It can be clearly observed from Fig. 5.3(a) that the SiC emitter PNP HBT exhibits a large collector-emitter offset voltage ~(1.75 V) compared to the SiC emitter NPN HBT due to the large built-in voltage difference between the emitter-base (EB) and base-collector (BC) junctions [44-45, 47] seen in Fig. 5.2. According to eq.(5.1), the collector-emitter offset voltage for SiC emitter NPN HBT is expected to be of ~(0.25 V) and matches well with the offset voltage shown in Fig. 5.3(b). The collector-emitter offset voltage of the SiC emitter PNP HBT calculated using eq.(5.1) comes out to be ~(1.75 V) and matches well with the offset voltage predicted from the IV characteristics shown in Fig. 5.3. Due to this large collector-emitter offset-voltage exhibited by the SiC emitter PNP HBTs, they cannot be used along with SiC emitter NPN HBTs. It can also be observed from Fig. 5.3 that the wide bandgap SiC emitter PNP HBT has a lesser current gain than that of the wide bandgap NPN HBT. But often, it is essential to have the performance of PNP HBTs nearly identical to that of NPN HBTs in BiCMOS applications such as push-pull amplifier design and also in ECL and complementary (npn/pnp) logic design.



(a)



(b)

Fig. 5.3 Common-emitter IV – characteristics of
(a). SiC emitter PNP HBT and (b). SiC emitter NPN HBT.

5.3 DUAL BANDGAP EMITTER APPROACH TO REDUCE V_{CE}(OFFSET) IN SIC EMITTER PNP HBTs

In this section, we show that the collector-emitter offset-voltage of wide bandgap SiC emitter PNP transistors can be significantly reduced by replacing the SiC emitter in the lateral PNP HBT by a dual bandgap emitter consisting of SiC on Si as shown in Fig. 5.4.

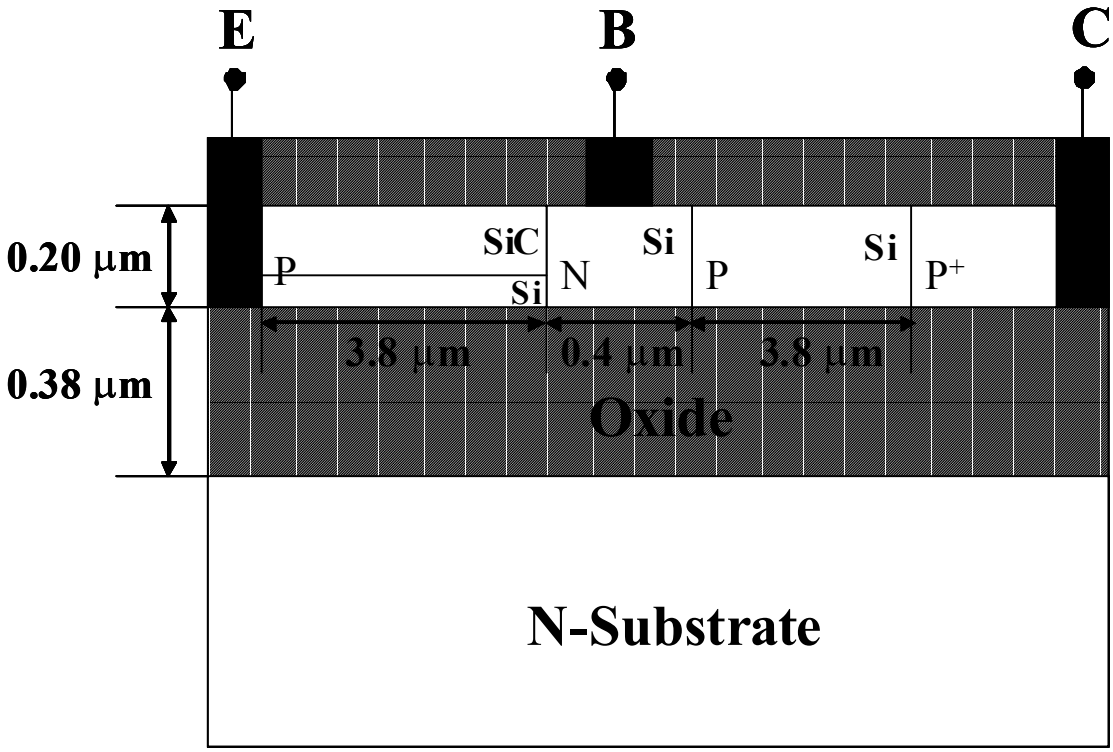


Fig. 5.4 Cross-sectional view of the dual bandgap emitter lateral PNP HBT.

The presence of a thin layer of P-silicon in the emitter reduces the collector-emitter offset-voltage drastically by eliminating built-in potential difference between emitter-base (EB) and base-collector (BC) junctions. The reduction of collector-emitter offset voltage in dual bandgap emitter PNP HBT can be best understood from Fig. 5.5.

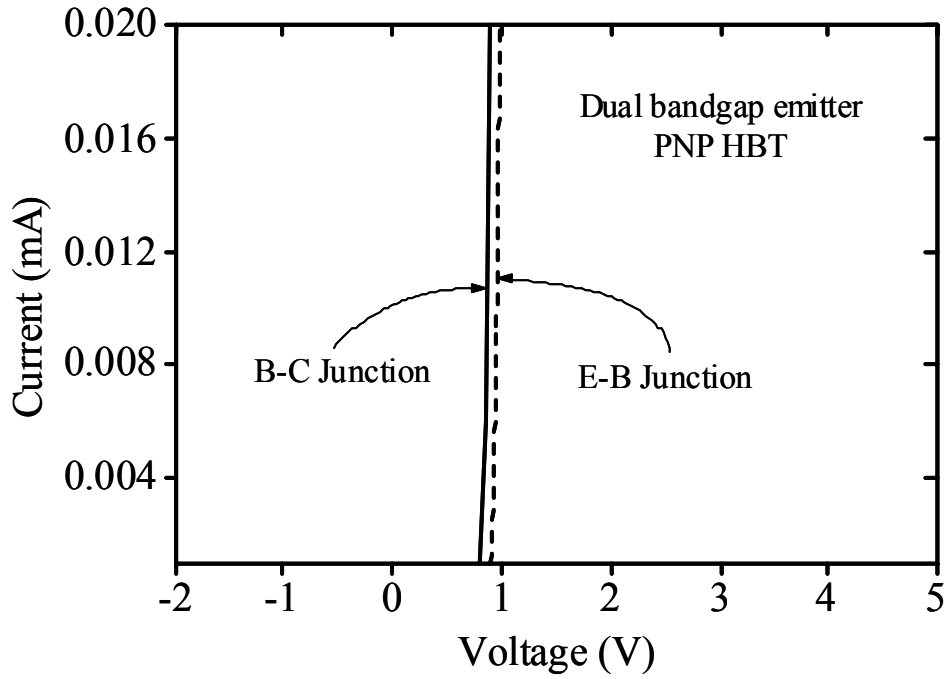


Fig. 5.5 E-B and B-C diode characteristics of the dual bandgap emitter PNP HBT.

As can be observed from Fig. 5.5, there is a large reduction in built-in potential of emitter-base (EB) junction after replacing SiC emitter by the dual bandgap emitter. Now the theoretically predicted offset voltage for the dual bandgap emitter PNP HBT should be approximately ~(0.05 V) according eq.(5.1). The output characteristics of the dual bandgap PNP HBT (emitter thickness: 0.15 μm SiC + 0.05 μm Si) are compared in Fig. 5.6 with that of SiC wide bandgap P-emitter PNP HBT. We observe that the $V_{CE(offset)}$ of the dual bandgap emitter PNP HBT matches with the value calculated from eq.(5.1) and is significantly smaller than the $V_{CE(offset)}$ of the SiC P-emitter HBT. However, while the introduction of a thin layer of silicon in the wide bandgap emitter reduces $V_{CE(offset)}$, it is also accompanied by a reduction in the current gain.

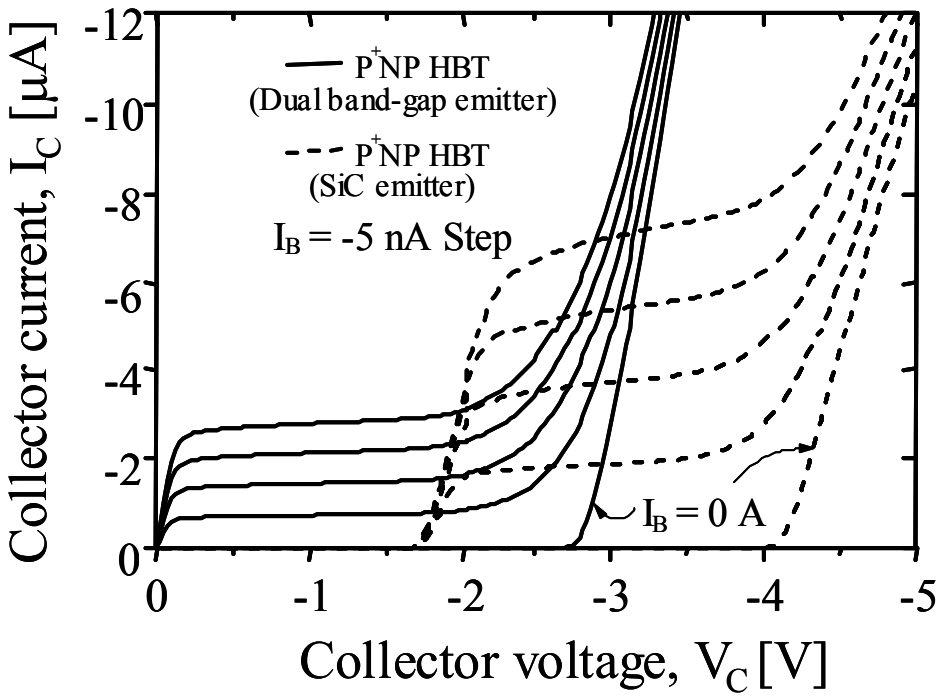


Fig. 5.6 Common-emitter IV – characteristics of the SiC emitter PNP HBT compared with that of the dual bandgap emitter PNP HBT.

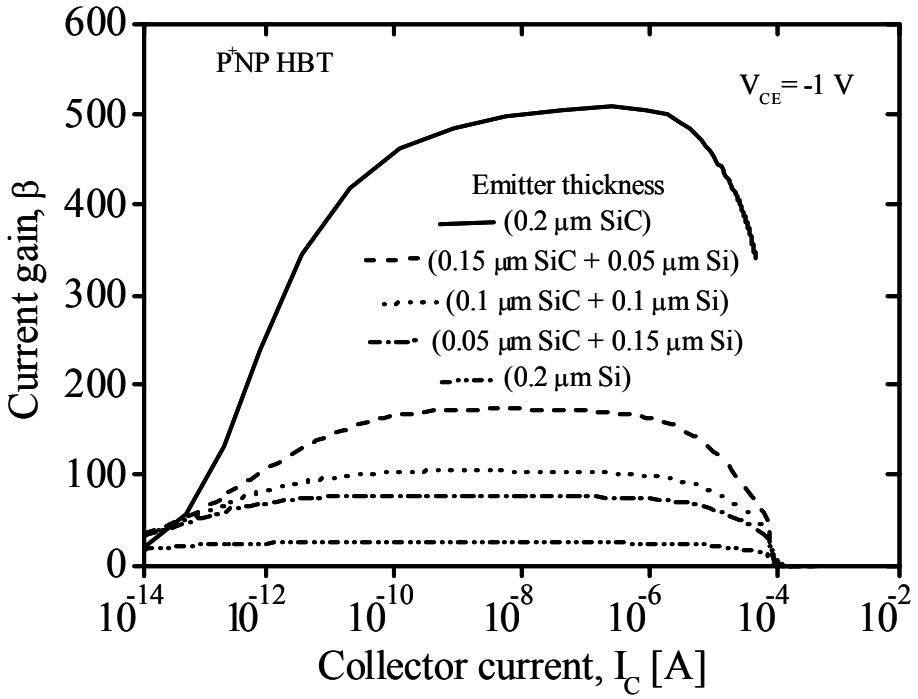


Fig. 5.7 Gain versus collector current characteristics of the dual bandgap emitter PNP HBT for various thicknesses of emitter (V_{CE} = -1 V).

In Fig. 5.7, the dependence of current gain is shown for different relative values of SiC and silicon in the emitter region. We notice that as the si film thickness increases, the current gain decreases. We demonstrate in the following section that the loss in current gain can be recovered by introducing the SiGe base in the proposed structure shown in Fig. 5.4.

5.4 APPLICATION OF SIGE BASE TO THE DUAL BANDGAP EMITTER PNP HBT

To improve the current gain of the dual bandgap emitter PNP HBT, in our simulations we have replaced the silicon base by the SiGe base(20% Ge content) in the proposed structure. The simulated current gain of the dual bandgap emitter with and without the SiGe base is shown in Fig. 5.8.

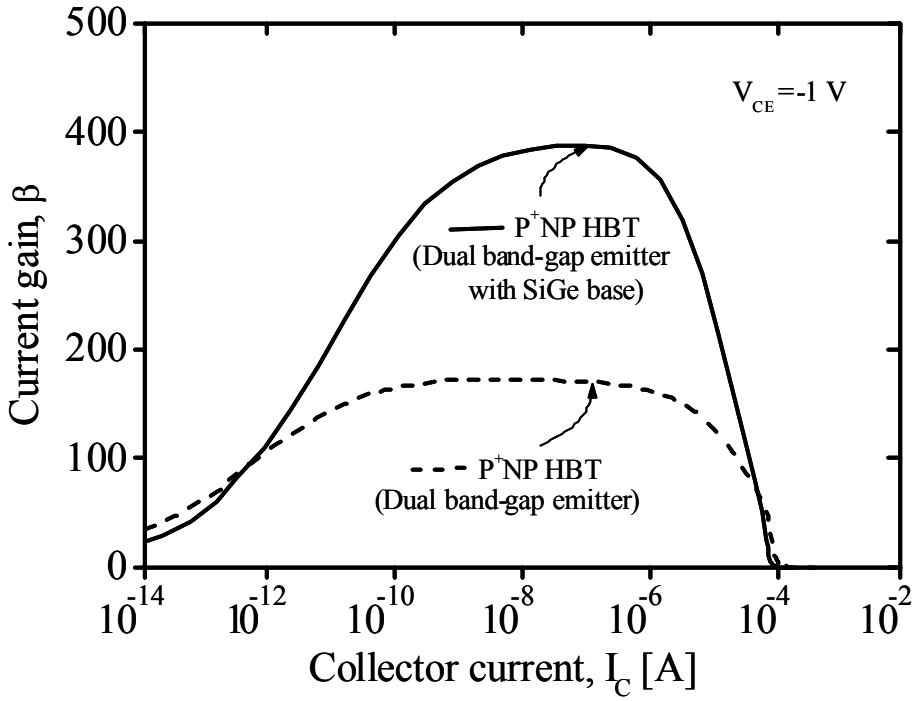


Fig. 5.8 Gain versus collector current characteristics of the dual bandgap emitter PNP HBT with and without SiGe base (V_{CE} = -1 V).

The presence of SiGe in the base region improves the emitter injection efficiency resulting in a higher current gain. Although the application of SiGe base restores the current gain, it is well known that PNP transistors suffer from large collector resistance due to low hole mobility. Further, SiGe base transistors suffer from the additional problem of excess stored base charge due to the accumulation of carriers at the collector-base junction [48]. The application of a Schottky collector has been shown to improve the performance of PNP bipolar transistors [16-17, 44]. Therefore, it would be of great interest to see how the usage of the Schottky collector to the dual bandgap emitter SiGe base PNP transistor will enhance its performance.

5.5 APPLICATION OF SCHOTTKY COLLECTOR TO THE DUAL BANDGAP EMITTER SIGE BASE PNP HBT AND ITS IMPACT ON DEVICE PERFORMANCE

In order to study the effect of the Schottky collector, we have replaced the P-collector of the proposed structure shown in Fig. 5.4 with a Schottky contact. Based on experimental results, it has been reported [49] that platinum silicide gives the highest barrier height (ϕ_{Bn} = 0.82 eV) with n-SiGe base. Therefore, making an appropriate Schottky contact to the n-SiGe base is not a difficult task.

The Gummel plots of this dual bandgap SiC-on-Si P-emitter SiGe base HBT with and without the Schottky collector transistor are compared in Fig. 5.9.

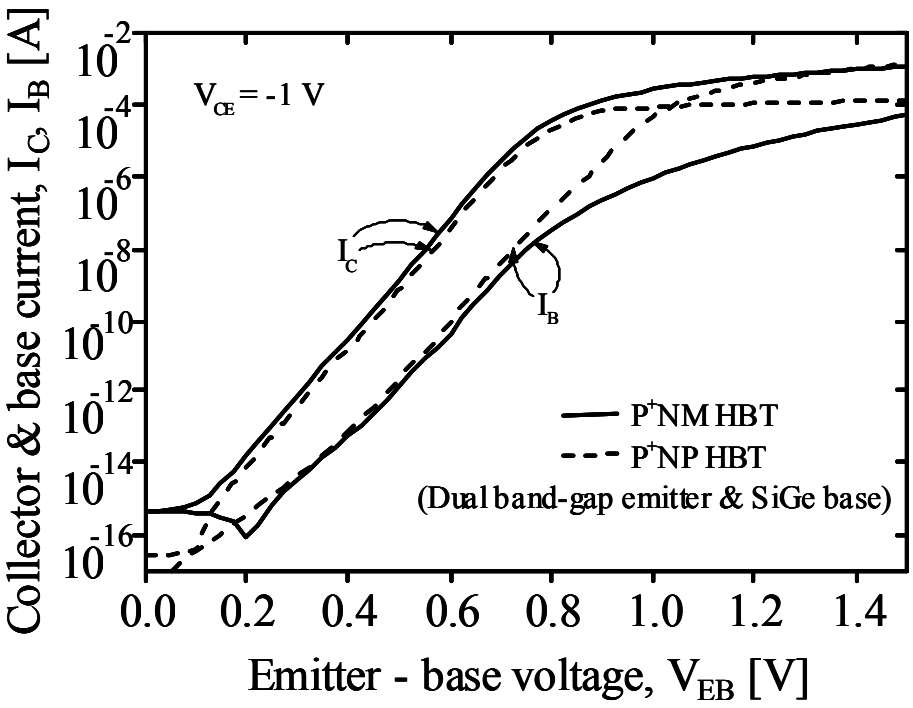


Fig. 5.9 Gummel plot of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with that of the dual bandgap emitter SiGe base PNP HBT (V_{CE} = -1 V).

We observe that the base current in the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT is smaller than that of the dual bandgap emitter SiGe base PNP HBT. This is mainly because of finite electron current I_{nm} caused by the electron flow from metal into the n-base [50]. As the electron current from emitter to base is fixed by the emitter-base forward bias voltage, the electron current I_{nm} from metal to n-base flows into the base terminal [50] reducing the total base current. As a result of this, the current gain of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT is higher than that of the dual bandgap emitter SiGe base PNP HBT as shown in Fig. 5.10.

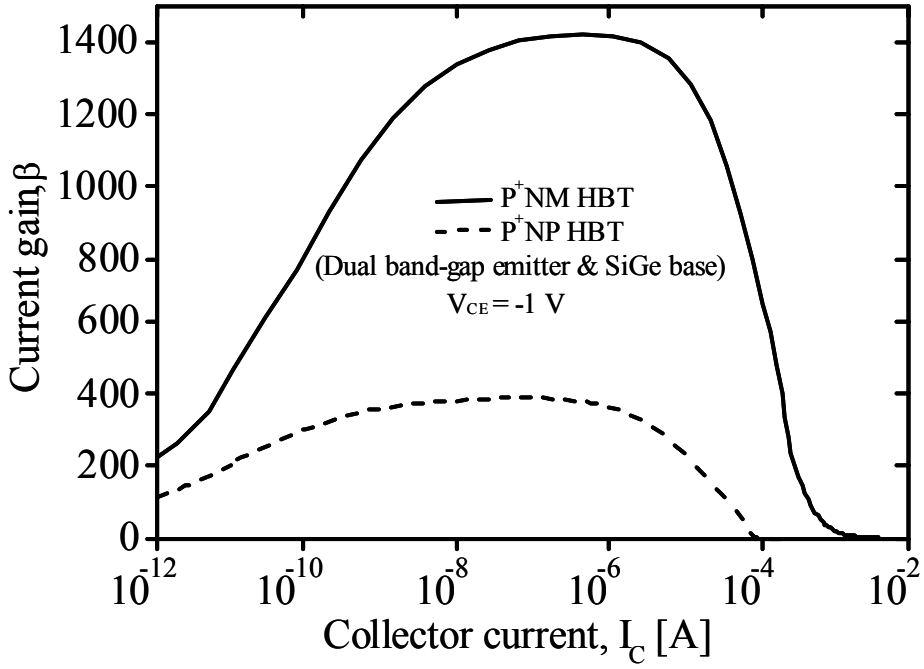


Fig. 5.10 Gain versus collector current characteristics of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with that of the dual bandgap emitter SiGe base PNP HBT (V_{CE} = -1 V).

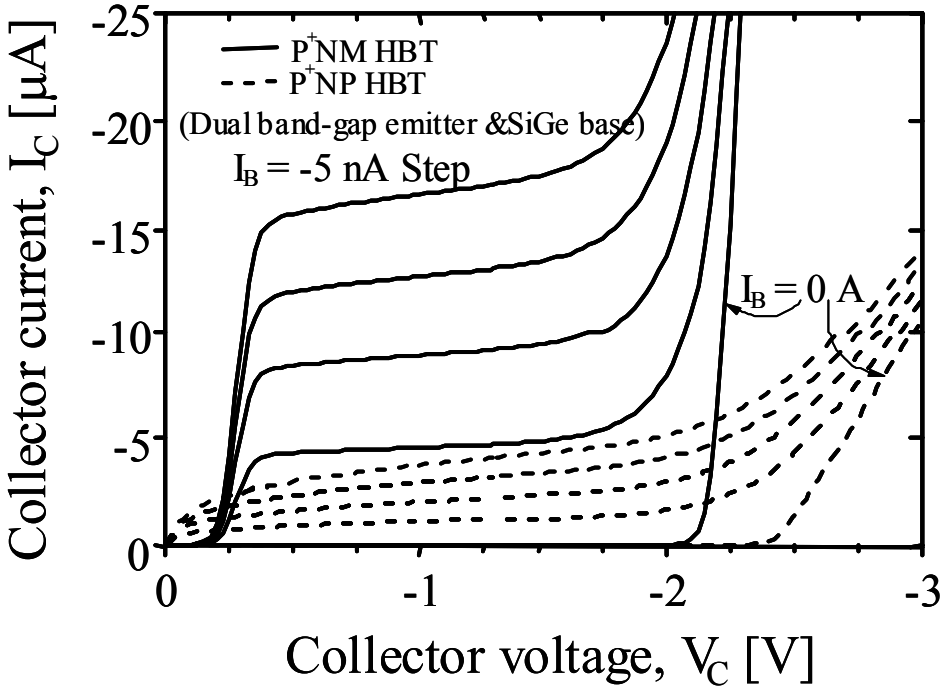


Fig. 5.11 Common-emitter IV – characteristics of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with that of the dual bandgap emitter SiGe base PNP HBT.

An interesting point is that the base current of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT is less than that of the dual bandgap emitter SiGe base PNP HBT even at high–level injection of carriers as shown in Fig. 5.9 which clearly shows the suppression of the Kirk effect [43] in the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT. The simulated I-V characteristics of dual bandgap emitter SiGe base lateral Schottky collector PNM HBT and dual bandgap emitter SiGe base PNP HBT are shown in Fig. 5.11. As can be seen, the current-voltage characteristics of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT are superior to those of the dual bandgap emitter SiGe base PNP HBT in terms of reduced collector resistance. However, there is a finite offset voltage for the dual bandgap emitter SiGe base Schottky collector PNM HBT mainly due to the reduced built-in potential of base-collector Schottky junction.

Fig. 5.12 shows the transient behaviour of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with the dual bandgap emitter SiGe base PNP HBT. It is clear that the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT exhibits excellent transient response with nearly zero base charge storage time due to its metal collector and suppressed Kirk effect while compared dual bandgap emitter SiGe base PNP HBT shows a higher storage time due to the Kirk effect and also the electron pile-up at the collector-base hetero-junction [43, 48].

Fig. 5.13 shows the unity gain cut-off frequency versus collector current of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT and is compared with the dual bandgap emitter SiGe base PNP HBT. As can be observed, the cut-off frequency of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT is higher than that of dual bandgap emitter SiGe base PNP HBT due to its metal collector and higher transconductance $g_{m.}$

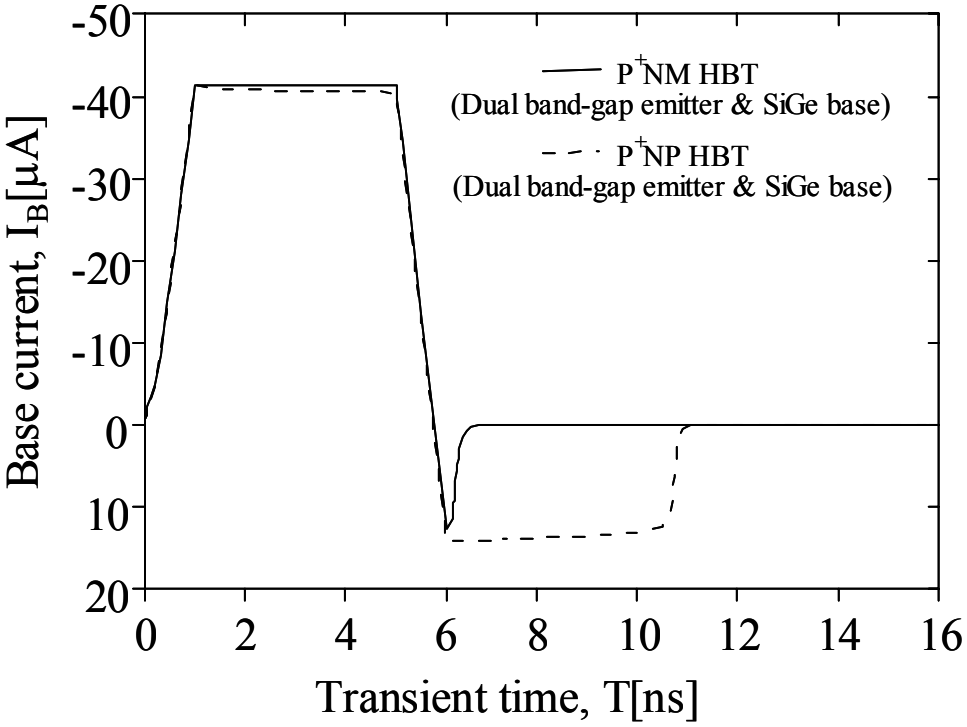


Fig. 5.12 Transient behaviour of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with that of the dual bandgap emitter SiGe base PNP HBT.

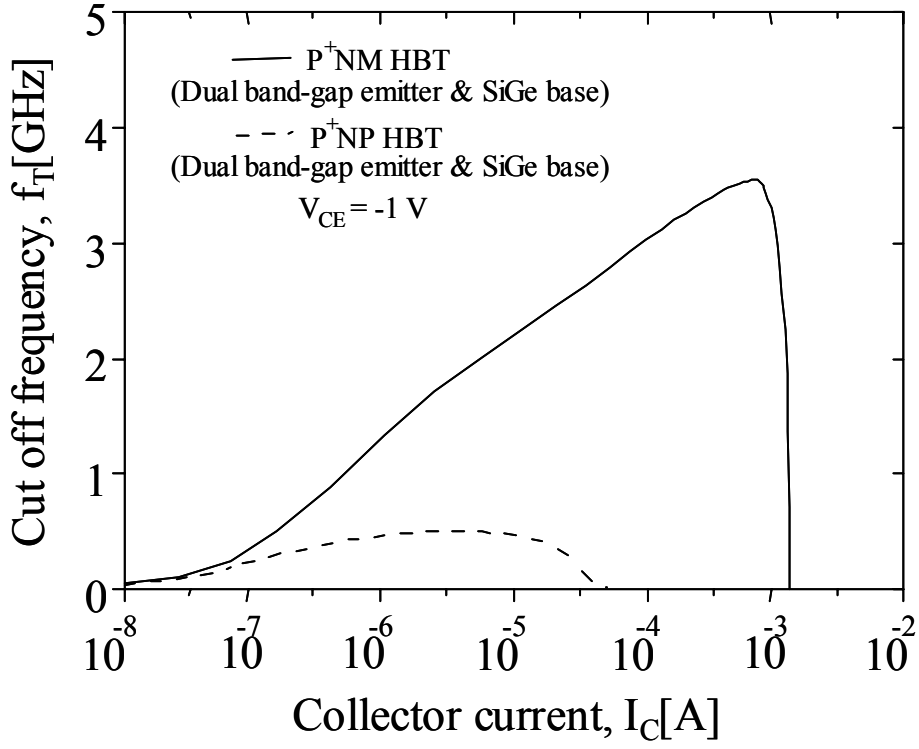


Fig. 5.13 Unity gain cut-off frequency versus collector current of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT compared with that of the dual bandgap emitter SiGe base PNP HBT.

The dual bandgap emitter SiGe base lateral Schottky collector PNM HBT exhibits an f_T of 3.55 GHz at a collector current of 0.6 mA, whereas for the comparable dual bandgap emitter SiGe base PNP HBT, f_T falls to a negligible value at the above current due to Kirk effect and decrease in transconductance.

5.6 THE EFFECT OF DOPING AND Ge % IN THE BASE

In all the above simulations we have assumed the base Ge concentration to be 20% which is the practical upper limit on Ge in most practical applications. However, it will be interesting to see the how the current gain and the breakdown voltage of the proposed structure change if the Ge concentration in the base region is varied. If ion-implantation is used to create the SiGe base, it is quite possible that the Ge content may lie in the range of 10 to 12 %. Therefore, we have next investigated the effect of base doping on peak current gain and breakdown voltage BV_{CEO} (for zero base current) for various germanium concentrations in the SiGe-base of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT.

Fig. 5.14 shows the peak current gain versus base doping for various germanium concentrations in the SiGe-base of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT. It can be observed from this figure that the peak current gain decreases as we decrease the germanium concentration in the SiGe base for a given base doping and the gain also decreases as we increase the base doping for a given Ge concentration because of low emitter injection efficiency.

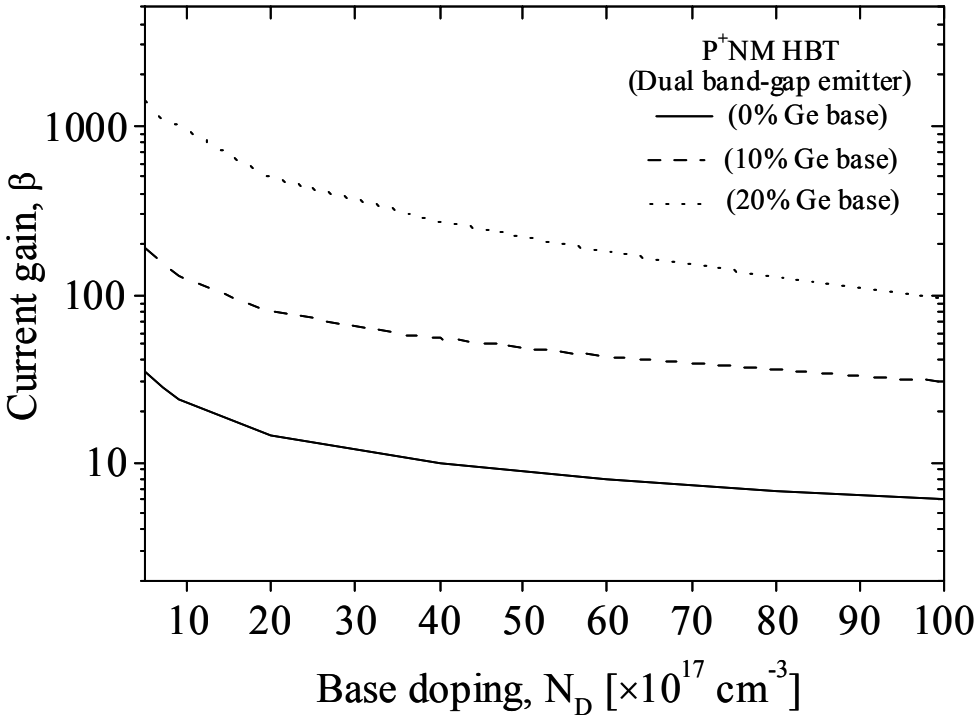


Fig. 5.14 Gain versus base doping for various germanium concentrations in the base of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT.

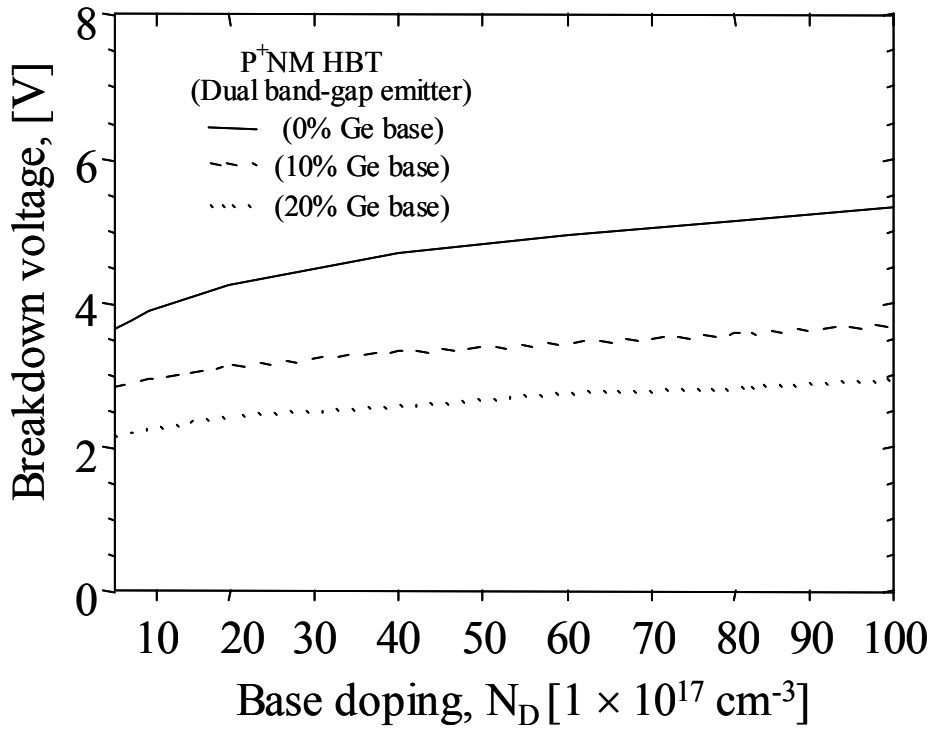


Fig. 5.15 Breakdown voltage BV_{CEO} (for zero base current) versus base doping for various germanium concentrations in the base of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT.

Fig. 5.15 shows the breakdown voltage BV_{CEO} (for zero base current) versus base doping for various germanium concentrations in the SiGe base of the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT. We note that for a given base doping, the breakdown voltage BV_{CEO} (for zero base current) increases as we decrease the germanium concentration and for a given Ge concentration, the breakdown voltage increases as we increase the base doping due to increasing critical electric field. The above design curves provide useful indicators on the required Ge concentration and base doping to realize a given current gain and breakdown voltage.

5.7 PROPOSED FABRICATION PROCEDURE

Fabrication of the proposed structure can be realized by introducing a few extra steps in the reported fabrication procedure of the lateral BJTs on SOI [8]. We can start with an SOI wafer having n-type epitaxial layer thickness of 0.2 μm and doping of 5×10^{17} cm^{-3}. In the first step, a thick CVD oxide is deposited and patterned as shown in Fig. 5.16(a). The uncovered N-region is converted into P-region by implanting a p-type dopant at a calibrated tilt angle as discussed in [17] as shown in Fig. 5.16(b). The P-type emitter region is then etched to a thickness of 0.05 μm as shown in Fig. 5.16(c). In the next step, we deposit the p^+ SiC on the horizontal edge (at point X in Fig. 5.16(d)) of the silicon surface which acts as a seed and the SiC grows [28-29] as shown in Fig. 5.16(d). Subsequent to this step, CMP process is performed and then a thick CVD oxide is deposited and patterned as shown in Fig. 5.16(e). Following this step, a nitride film is deposited as shown in Fig. 5.16(f). In the next step, an unmasked RIE etch is performed until the planar silicon nitride is etched. This retains the nitride spacer at the vertical edge of thick CVD oxide as shown in Fig. 5.16(g).

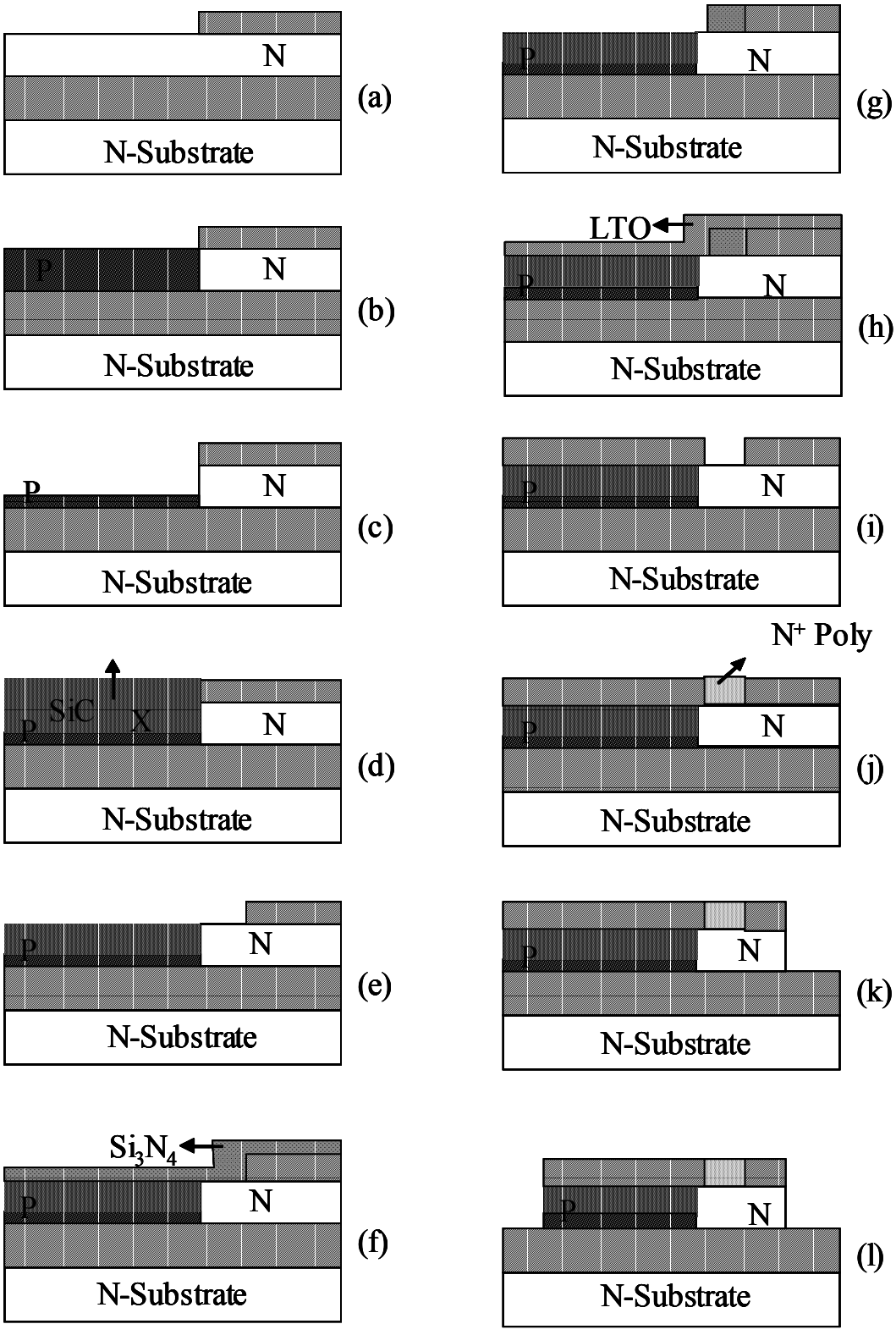


Fig. 5.16 Proposed fabrication steps for the dual bandgap emitter SiGe base lateral Schottky collector PNM HBT on SOI.

After a thick oxide is deposited as shown in Fig. 5.16(h), CMP process is carried out to planarize the surface. Next, nitride spacer is removed with selective etching, which will create a window in the oxide as shown in Fig. 5.16(i). Germanium can now be implanted [34-36, 51] through this window to convert silicon in the base region to SiGe. Ge implantation can be performed at an energy of 130 KeV with fluences of 1, 2, or 3 x $10^{16}cm^{-2}$ according to the reported works in the literature [34]. To re-crystallize the implanted SiGe layer, a rapid thermal annealing (RTA) need to be performed at 1000 ^{o}C for about 10 s. This process is to ensure complete re-crystallization of SiGe amorphous layer [34].

After converting, silicon in the base region to SiGe, we then deposit n^{+} - poly and then the wafer is once again planarized using CMP leaving n^{+} - poly in the place where the nitride film was present earlier as shown in Fig. 5.16(j). Following this step, a contact window is opened for metal Schottky collector as shown in Fig. 5.16(k) and subsequent to this step, the p^{+} emitter contact window is opened as shown in Fig. 5.16(l). Finally, platinum silicide is deposited to form the Schottky collector contact and ohmic contacts on the emitter and p^{+} - poly base region.

5.8 CONCLUSION

In this, we have first discussed the reasons for the significant collector-emitter offset voltage observed in wide bandgap SiC P-emitter HBTs. Based on numerical simulations, we have demonstrated that using a dual bandgap SiC-on-Si emitter in the presence of the SiC P-emitter, greatly reduces the collector-emitter offset voltage of wide bandgap PNP HBTs. However, the presence of Si in the emitter results in a reduced current gain and the low hole mobility in the P-collector gives rise to a high collector resistance. To overcome this problem, we have applied the SiGe base and a metal Schottky collector to the proposed structure and demonstrated that the resulting device not only will have very low collector emitter offset voltage but will also exhibit high current gain and negligible storage time. Based on reported experimental results for the lateral BJTs on SOI, we have also suggested a possible fabrication procedure for the proposed structure. We conclude from our study of the dual bandgap SiC P-emitter HBT with the combination of SiGe base and Schottky collector that the proposed structure should be a good candidate for BiCMOS applications requiring both NPN and PNP HBTs with comparable performance.

Chapter 6

Conclusions

In this thesis work, we have proposed a few novel BiCMOS compatible lateral Schottky devices namely:

- A Novel high voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) rectifier with ideal forward and reverse characteristics,
- Application of Lateral Dual Sidewall Schottky (LDSS) concept for improved rectifier performance on SOI,
- 2D-Simulation and analysis of lateral SiC N-emitter SiGe P-base Schottky Metal-collector (NPM) HBT on SOI and
- A New lateral Dual – bandgap P-Emitter N-SiGe base Schottky Metal-collector (PNM) HBT on SOI with reduced collector-emitter offset voltage.

Based on our simulation results in chapters 2 & 3, we conclude that the proposed LDSS concept, makes it possible to achieve low forward drop which is close to that of a Lateral Trench Sidewall Schottky (LTSS) rectifier using a low-barrier metal as well as less reverse leakage current close to that of the LTSS rectifier using a high-barrier metal. Our simulation work demonstrates that using our proposed structure, near ideal Schottky characteristics can be obtained in terms of low forward drop and low reverse current.

In the latter two chapters, we have proposed HBTs with Schottky collector junction which exhibit excellent performance in terms of high current gain, high cut-off frequency, excellent switching response, high collector current driving capability and suppressed Kirk effect over its counterparts. We have demonstrated that using a novel dual bandgap emitter concept, it is possible to significantly reduce the collector-emitter offset voltage in wide bandgap emitter PNP/PNM HBTs by eliminating the built-in potential difference between emitter-base (EB) junction and base-collector (BC) junction. We have also presented a BiCMOS compatible fabrication procedure for all our proposed devices.

Future Work:

It would be interesting to fabricate and test the above devices. This could be taken up as an extension of this work as fabrication of these devices will provide a further understanding of the problems involved in making these devices work.

APPENDIX – A

```
TITLE     NEW 4H-SIC LDSS RECTIFIER 2D SIMULATION (FORWARD CHARACTERISTICS)

COMMENT   *** SPECIFY A RECTANGULAR MESH ***
MESH
X.MESH    X.MIN=0.00    X.MAX=1.50     H1=0.250
X.MESH    X.MIN=1.50    X.MAX=1.60     H1=0.050
X.MESH    X.MIN=1.60    X.MAX=7.00     H1=0.250
X.MESH    X.MIN=7.00    X.MAX=8.00     H1=0.125

Y.MESH    Y.MIN=-1.00   Y.MAX=0.00     H1=0.100
Y.MESH    Y.MIN=0.00    Y.MAX=1.75     H1=0.125
Y.MESH    Y.MIN=1.75    Y.MAX=1.76     H1=0.005
Y.MESH    Y.MIN=1.76    Y.MAX=2.00     H1=0.125

COMMENT   *** REGION DEFINITION ***
REGION    NAME=1  SIC
REGION    NAME=2  SIC   X.MIN=7.50   X.MAX=8.0   Y.MIN=0.00   Y.MAX=2.00
REGION    NAME=4  OXIDE X.MIN=0.00   X.MAX=8.0   Y.MIN=-1.0   Y.MAX=0.00

COMMENT   *** ELECTRODE DEFINITION ***
ELECTR    NAME=AHB      X.MIN=4.00   X.MAX=6.00   Y.MIN=-1.00   Y.MAX=-0.40
ELECTR    NAME=AHB      X.MIN=1.50   X.MAX=5.00   Y.MIN=-1.00   Y.MAX=-0.40
ELECTR    NAME=AHB      X.MIN=0.00   X.MAX=1.50   Y.MIN=-1.00   Y.MAX=1.75
ELECTR    NAME=ALB      X.MIN=0.00   X.MAX=1.00   Y.MIN=1.76    Y.MAX=2.00
ELECTR    NAME=CATHODE  X.MIN=7.50   X.MAX=8.00   Y.MIN=-1.00   Y.MAX=0.00

COMMENT   *** SPECIFY IMPURITY PROFILES ***
PROFILE   REGION=1  N-TYPE N.PEAK=1E17   UNIFORM OUT.FILE=G1DS
PROFILE   REGION=2  N-TYPE N.PEAK=1E20   UNIFORM

PLOT.2D   GRID  TITLE="INITIAL GRID"   FILL  SCALE

COMMENT   *** REGRID ON DOPING ***
REGRID    DOPING  LOG  RATIO=2  SMOOTH=1
+         IN.FILE=G1DS
PLOT.2D   GRID  TITLE="DOPING REGRID"  FILL  SCALE

COMMENT   *** SPECIFY CONTACT PARAMETERS ***
CONTACT   NAME=ALB  WORKFUNC=4.75  SURF.REC
CONTACT   NAME=AHB  WORKFUNC=5.40  SURF.REC

COMMENT   *** SPECIFY MATERIAL PAREMETERS ***
MATERIAL  REGION=(1,2)  EG300=3.1  PERMITTI=9.66  AFFINITY=3.90
+         ARICHN=140    ARICHP=32
MATERIAL  REGION=1  TAUN0=2E-6    TAUP0=2E-6
MATERIAL  REGION=2  TAUN0=0.1E-6  TAUP0=0.05E-6

MOBILITY  REGION=(1,2)     MUN1.ARO=50     MUN2.ARO=950    AN.ARORA=0.88
+             CN.ARORA=2.2E17   EXN1.ARO=-0.57  EXN2.ARO=-2.33  EXN3.ARO=2.40
+             EXN4.ARO=-0.146   MUP1.ARO=10     MUP2.ARO=180    AP.ARORA=0.88
+             CP.ARORA=2.35E17  EXP1.ARO=-0.57  EXP2.ARO=-2.33  EXP3.ARO=2.40
+             EXP4.ARO=-0.146

COMMENT   *** SPECIFY PHYSICAL MODELS ***
MODELS    FERMIDIR INCOMPLE IMPACT.I CONSRH ARORA AUGER FLDMOB
```

```
COMMENT   *** SYMBOLIC FACTORIZATION, SOLVE ***
SYMBOL    CARRIERS=2  NEWTON
METHOD    ICCG  DAMPED
SOLVE

COMMENT   *** POTENTIAL REGRID ***
REGRID    POTEN  RATIO=2  MAX=1  SMOOTH=1
+         IN.FILE=G1DS    OUT.FILE=G1MS
PLOT.2D   GRID TITLE="POTENTIAL REGRID"  FILL SCALE
SYMBOL    CARRIERS=2  NEWTON
METHOD    ICCG  DAMPED
SOLVE     V(ALB)=0    V(AHB)=0

COMMENT   *** FORWARD CHARACTERISTICS ***
LOG       OUT.FILE=DATAFNEW
LOOP      STEPS=5
ASSIGN    NAME=BIAS   N.VALUE=(0.01,0.02,0.05,0.07,0.08)
EXTRACT   NAME=EMAX1 UNITS=V/CM  EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+         COND="@Y>1.76&@Y<2.0&@X=1.0" NOW
EXTRACT   NAME=EMIN1  UNITS=V/CM  EXPRESS="MIN(@EMIN1;@EM)"  INITAL.V=0
+         COND="@Y>1.76&@Y<2.0&@X=1.0" NOW
EXTRACT   NAME=E1     UNITS=V/CM
+         EXPRESS=((@EMAX1+@EMIN1)/2)  NOW
EXTRACT   NAME=DPHIL  UNITS=EV   NOW
+         EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL   UNITS=EV
+         EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=ALB    WORKFUNC=@NWFL  SURF.REC

EXTRACT   NAME=EMAX2 UNITS=V/CM  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+         COND="@Y>0.0&@Y<2.0&@X=1.55"  NOW
EXTRACT   NAME=EMIN2 UNITS=V/CM  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+         COND="@Y>0.0&@Y<2.0&@X=1.55"  NOW
EXTRACT   NAME=E2     UNITS=V/CM
+         EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT   NAME=DPHIH  UNITS=EV   NOW
+         EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT   NAME=NWFH   UNITS=EV
+         EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=AHB    WORKFUNC=@NWFH  SURF.REC
METHOD    ICCG  DAMPED
SOLVE     V(ALB)=@BIAS  V(AHB)=@BIAS
L.END

LOOP      STEPS=19
ASSIGN    NAME=BIAS   N.VALUE=0.1  DELTA=0.05
EXTRACT   NAME=EMAX1 UNITS=V/CM   EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+         COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=EMIN1 UNITS=V/CM   EXPRESS="MIN(@EMIN1;@EM)"  INITAL.V=0
+         COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=E1     UNITS=V/CM
+         EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT   NAME=DPHIL  UNITS=EV   NOW
+         EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL   UNITS=EV
+         EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=ALB    WORKFUNC=@NWFL  SURF.REC
EXTRACT   NAME=EMAX2 UNITS=V/CM  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+         COND="@Y>0.0&@Y<2.0&@X=1.55"  NOW
EXTRACT   NAME=EMIN2 UNITS=V/CM  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
```

```
+       COND="@Y>0.0&@Y<2.0&@X=1.55"  NOW
EXTRACT   NAME=E2    UNITS=V/CM
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT   NAME=DPHIH  UNITS=EV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT   NAME=NWFH   UNITS=EV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=AHB    WORKFUNC=@NWFH  SURF.REC
METHOD    ICCG  DAMPED
SOLVE     V(ALB)=@BIAS  V(AHB)=@BIAS
L.END

EXTRACT   NAME=JF  UNITS=A/CM^2  EXPRESS=((@I(ALB)+@I(AHB))/(2E-8))
EXTRACT   NAME=IF  UNITS=A/CM    EXPRESS=(@I(ALB)+@I(AHB))*(1E4)
EXTRACT   NAME=VF  UNITS=VOLTS    EXPRESS=@V(AHB)/(1.0)

PLOT.1D   Y.LOG    Y.AXIS=JF  X.AXIS=VF POINTS
+       COLOR=2  TITLE="FORWARD CHARACTERISTIC"
+       LEFT=0.0 RIGHT=2.0  BOTTOM=1E-7  TOP=1E4  OUT.FILE=DJFNEWLDSS

PLOT.1D   Y.LOG    Y.AXIS=IF  X.AXIS=VF  POINTS
+       COLOR=2  TITLE="FORWARD CHARACTERISTIC"
+       LEFT=0.0 RIGHT=2.0  BOTTOM=1E-7  TOP=1E4  OUT.FILE=DCFNEWLDSS

COMMENT   *** CURRENT FLOW VECTORS ***
PLOT.2D   BOUND  JUNC
+       TITLE="CURRENT FLOW VECTORS"
VECTOR    J.TOTAL  COLOR=1  V.SIZE=2.0  CLIPFACT=0.01

STOP
```

```
TITLE   NEW SIC LDSS RECTIFIER 2D SIMULATION (Reverse
characteristics)

COMMENT   *** Specify a rectangular mesh ***
MESH
X.MESH   X.MIN=0.00   X.MAX=3.00   H1=0.250
X.MESH   X.MIN=3.00   X.MAX=7.00   H1=0.500
X.MESH   X.MIN=7.00   X.MAX=8.00   H1=0.125

Y.MESH   Y.MIN=-1.00  Y.MAX=0.00   H1=0.100
Y.MESH   Y.MIN=0.00   Y.MAX=1.75   H1=0.125
Y.MESH   Y.MIN=1.75   Y.MAX=1.76   H1=0.005
Y.MESH   Y.MIN=1.76   Y.MAX=2.00   H1=0.125

COMMENT   *** Region definition ***
REGION   NAME=1  SIC
REGION   NAME=2  SIC   X.MIN=7.50   X.MAX=8.00   Y.MIN=0.00   Y.MAX=2.00
REGION   NAME=4  OXIDE  X.MIN=0.00   X.MAX=8.00   Y.MIN=-1.00   Y.MAX=0.00

COMMENT   *** Electrode definition ***
ELECTR   NAME=Ahb      X.MIN=4.00   X.MAX=6.00   Y.MIN=-1.00   Y.MAX=-0.40
ELECTR   NAME=Ahb      X.MIN=1.50   X.MAX=4.00   Y.MIN=-1.00   Y.MAX=-0.40
ELECTR   NAME=Ahb      X.MIN=0.00   X.MAX=1.50   Y.MIN=-1.00   Y.MAX=1.75
ELECTR   NAME=Alb      X.MIN=0.00   X.MAX=1.00   Y.MIN=1.76   Y.MAX=2.00
ELECTR   NAME=Cathode   X.MIN=7.50   X.MAX=8.00   Y.MIN=-1.00   Y.MAX=0.00

COMMENT   *** Specify impurity profiles ***
PROFILE   REGION=1  N-TYPE N.PEAK=1E17   UNIFORM  OUT.FILE=G1DS
PROFILE   REGION=2  N-TYPE N.PEAK=1E20   UNIFORM

PLOT.2D   GRID  TITLE="Initial grid"  FILL  SCALE

COMMENT   *** Regrid on doping ***
REGRID   DOPING  LOG  RATIO=2  SMOOTH=1
+       IN.FILE=G1DS
PLOT.2D   GRID  TITLE="Doping regrid"  FILL  SCALE

COMMENT   *** Specify contact parameters ***
CONTACT   NAME=Alb  WORKFUNC=4.75  SURF.REC
CONTACT   NAME=Ahb  WORKFUNC=5.40  SURF.REC

COMMENT   *** Specify material parameters ***
MATERIAL  REGION=(1,2)  EG300=3.10  PERMITTI=9.66  AFFINITY=3.90
+       ARICHN=140    ARICHP=32
MATERIAL  REGION=1  TAUN0=2E-6    TAUP0=2E-6
MATERIAL  REGION=2  TAUN0=0.1E-6  TAUP0=0.05E-6

MOBILITY  REGION=(1,2)     MUN1.ARO=50    MUN2.ARO=950    AN.ARORA=0.88
+           CN.ARORA=2.2E17   EXN1.ARO=-0.57  EXN2.ARO=-2.33  EXN3.ARO=2.40
+           EXN4.ARO=-0.146   MUP1.ARO=10    MUP2.ARO=180    AP.ARORA=0.88
+           CP.ARORA=2.35E17  EXP1.ARO=-0.57  EXP2.ARO=-2.33  EXP3.ARO=2.40
+           EXP4.ARO=-0.146

COMMENT   *** Specify physical models ***
MODELS    FERMIDIR INCOMPLE IMPACT.I CONSRH  ARORA AUGER FLDMOB

COMMENT   *** Symbolic factorization, solve ***
SYMBOL    CARRIERS=2  NEWTON
METHOD    ICCG  DAMPED
SOLVE
```

```
COMMENT   *** Potential regrid ***
REGRID   POTEN  RATIO=2  MAX=1  SMOOTH=1
+       IN.FILE=G1DS   OUT.FILE=G1MS
PLOT.2D   GRID TITLE="Potential regrid"  FILL  SCALE
SYMBOL   CARRIERS=2  NEWTON
SOLVE    V(Alb)=0    V(Ahb)=0

COMMENT   *** Reverse characteristics ***
LOG      OUT.FILE=DATARNEW
LOOP     STEPS=12
ASSIGN   NAME=BIAS  N.VALUE=(-1,-2,-4,-6,-8,-10,-20,-30,-40,-50,-60,-70)
EXTRACT   NAME=EMAX1 UNITS=V/cm  EXPRESS="MAX(@EMAX1;@EM)"   INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=EMIN1 UNITS=V/cm  EXPRESS="MIN(@EMIN1;@EM)"   INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT   NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL   UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=Alb  WORKFUNC=@NWFL  SURF.REC

EXTRACT   NAME=EMAX2  UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=EMIN2  UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT   NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT   NAME=NWFH   UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
SOLVE    V(Alb)=@BIAS  V(Ahb)=@BIAS
L.END

LOOP     STEPS=6
ASSIGN   NAME=BIAS  N.VALUE=-80  DELTA=-20
EXTRACT   NAME=EMAX1 UNITS=V/cm   EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=EMIN1 UNITS=V/cm   EXPRESS="MIN(@EMIN1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT   NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL   UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=Alb  WORKFUNC=@NWFL  SURF.REC

EXTRACT   NAME=EMAX2  UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=EMIN2  UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT   NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
```

```
EXTRACT   NAME=NWFH   UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
METHOD            ICCG DAMPED   CONT.STK=8
SOLVE     V(Alb)=@BIAS  V(Ahb)=@BIAS
L.END

LOOP      STEPS=13
ASSIGN    NAME=BIAS  N.VALUE=-200  DELTA=-50
EXTRACT   NAME=EMAX1 UNITS=V/cm    EXPRESS="MAX(@EMAX1;@EM)" INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=EMIN1 UNITS=V/cm    EXPRESS="MIN(@EMIN1;@EM)" INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT   NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL   UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=Alb  WORKFUNC=@NWFL  SURF.REC

EXTRACT   NAME=EMAX2  UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)" INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=EMIN2  UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)" INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT   NAME=E2     UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT   NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT   NAME=NWFH   UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
METHOD            ICCG DAMPED  CONT.STK=8
SOLVE     V(Alb)=@BIAS V(Ahb)=@BIAS
L.END

LOOP      STEPS=7
ASSIGN    NAME=BIAS  N.VALUE=-860 DELTA=-20
EXTRACT   NAME=EMAX1 UNITS=V/cm  EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=EMIN1 UNITS=V/cm  EXPRESS="MIN(@EMIN1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT   NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT   NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT   NAME=NWFL  UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT   NAME=Alb  WORKFUNC=@NWFL  SURF.REC
EXTRACT   NAME=EMAX2 UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50" NOW
EXTRACT   NAME=EMIN2 UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50" NOW
EXTRACT   NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)  NOW
EXTRACT   NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT   NAME=NWFH  UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT   NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
```

```
METHOD          ICCG DAMPED   CONT.STK=8
SOLVE    V(Alb)=@BIAS  V(Ahb)=@BIAS
L.END

LOOP     STEPS=2
ASSIGN   NAME=BIAS  N.VALUE=-980  DELTA=-.0005
EXTRACT  NAME=EMAX1 UNITS=V/cm   EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT  NAME=EMIN1 UNITS=V/cm   EXPRESS="MIN(@EMIN1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT  NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT  NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT  NAME=NWFL  UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT  NAME=Alb  WORKFUNC=@NWFL  SURF.REC

EXTRACT  NAME=EMAX2 UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT  NAME=EMIN2 UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT  NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT  NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT  NAME=NWFH  UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT  NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
METHOD          ICCG DAMPED   CONT.STK=8
SOLVE    V(Alb)=@BIAS  V(Ahb)=@BIAS
L.END

LOOP     STEPS=2
ASSIGN   NAME=BIAS  N.VALUE=-982.15  DELTA=-.0005
EXTRACT  NAME=EMAX1 UNITS=V/cm     EXPRESS="MAX(@EMAX1;@EM)"  INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT  NAME=EMIN1 UNITS=V/cm     EXPRESS="MIN(@EMIN1;@EM)" INITAL.V=0
+       COND="@Y>1.76&@Y<2.0&@X=1.0"  NOW
EXTRACT  NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)   NOW
EXTRACT  NAME=DPHIL  UNITS=eV   NOW
+       EXPRESS=(3.63E-4*@E1**(1/2))-1E-3*EXP(3.52*((@E1**3-1E12)/(@E1**3)))
EXTRACT  NAME=NWFL  UNITS=eV
+       EXPRESS=(4.75-@DPHIL)  NOW
CONTACT  NAME=Alb  WORKFUNC=@NWFL  SURF.REC

EXTRACT  NAME=EMAX2  UNITS=V/cm  EXPRESS="MAX(@EMAX2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT  NAME=EMIN2  UNITS=V/cm  EXPRESS="MIN(@EMIN2;@EM)"  INITAL.V=0
+       COND="@Y>0.0&@Y<2.0&@X=1.50"  NOW
EXTRACT  NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)   NOW
EXTRACT  NAME=DPHIH  UNITS=eV   NOW
+       EXPRESS=(1.54E-4*@E2**(1/2))+1E-3*EXP(6.458*((@E2**3-1E12)/(@E2**3)))
EXTRACT  NAME=NWFH  UNITS=eV
+       EXPRESS=(5.40-@DPHIH)  NOW
CONTACT  NAME=Ahb  WORKFUNC=@NWFH  SURF.REC
METHOD          ICCG DAMPED   CONT.STK=8
SOLVE    V(Alb)=@BIAS  V(Ahb)=@BIAS
```

```
L.END

EXTRACT   NAME=JR  UNITS=A/cm^2  EXPRESS=((@I(Alb)+@I(Ahb))/(2E-8))
EXTRACT   NAME=IR  UNITS=A/cm    EXPRESS=(@I(Alb)+@I(Ahb))*(1E4)
EXTRACT   NAME=VR  UNITS=volts   EXPRESS=@V(Alb)/(-1.0)
EXTRACT   NAME=E1  UNITS=V/cm
+       EXPRESS=((@EMAX1+@EMIN1)/2)
EXTRACT   NAME=E2  UNITS=V/cm
+       EXPRESS=((@EMAX2+@EMIN2)/2)

COMMENT         *** VR Vs. IR plot ***
PLOT.1D   Y.LOG    Y.AXIS=IR   X.AXIS=VR    CURVE    COLOR=2
+       TITLE="Reverse characteristic"
+       LEFT=0.0  RIGHT=1200  BOTTOM=1E-12  TOP=1E3  OUT.FILE=DCRNEW

COMMENT   *** VR Vs. JR plot ***
PLOT.1D   Y.LOG    Y.AXIS=JR   X.AXIS=VR    CURVE    COLOR=2
+       TITLE="Reverse characteristic"
+       LEFT=0.0  RIGHT=1200  BOTTOM=1E-7   TOP=1E3  OUT.FILE=DJRNEW

COMMENT   *** DPHIL(Low barrier Schottky) Vs. VR plot ***
PLOT.1D   Y.AXIS=DPHIL   X.AXIS=VR   POINTS     COLOR=1
+       TITLE="Barrier lowering"
+       LEFT=0.0  RIGHT=1200  BOTTOM=0.0    TOP=1.0  OUT.FILE=DBRLNEW

COMMENT   *** DPHIH(High barrier Schottky) Vs. VR plot ***
PLOT.1D   Y.AXIS=DPHIH   X.AXIS=VR   POINTS     COLOR=1
+       TITLE="Barrier lowering"
+       LEFT=0.0  RIGHT=1200  BOTTOM=0.0  TOP=1.0  OUT.FILE=DBRHNEW

PLOT.1D   Y.AXIS=E1  X.AXIS=VR   POINTS     COLOR=1
+       TITLE="Electric field"
+       LEFT=0.0   RIGHT=1200  BOTTOM=0.0  TOP=5E6  OUT.FILE=DE1NEW

PLOT.1D   Y.AXIS=E2  X.AXIS=VR   POINTS     COLOR=1
+       TITLE="Electric field"
+       LEFT=0.0   RIGHT=1200  BOTTOM=0.0  TOP=5E6  OUT.FILE=DE2NEW

COMMENT   *** E.FIELD at the 4H-SiC and SiO2 interface ***
PLOT.1D   E.FIELD  X.START=0    X.END=8    Y.START=0  Y.END=0
+       COLOR=2  POINTS  TITLE="Electric field "    OUT.FILE=SEFNEW
COMMENT   *** Electric field contours ***
PLOT.2D   BOUND    JUNC    DEPL  FILL  SCALE
+       TITLE="Electric field contours"
CONTOUR   E.FIELD  WINDOW  NCONTOUR=15  COLOR=7

COMMENT   *** 2D E.FIELD ***
PLOT.3D   E.FIELD  PHI=50  TITLE="Electric field"
+       Y.MIN=0  Y.MAX=2.0  Z.MIN=0  Z.MAX=5E6  Y.LINES=30  X.LINES=70
+       X.LABEL="Horizontal distance (micron)"
+       Y.LABEL="Vertical distance (micron)"
+       Z.LABEL="Electric field (V/cm)"
3D.SURFACE   LINE.TYP=1

COMMENT   *** Current flow vectors ***
PLOT.2D   BOUND  JUNC  DEPL  Y.OFFSET=2.0  SCALE  FILL
+       TITLE="Current flow vectors"
VECTOR    J.TOTAL  COLOR=1

STOP
```

APPENDIX – B

```
COMMENT Simulation of LDSS rectifier in SOI

COMMENT *** Specify a rectangular mesh ***
MESH   SMOOTH=1

X.MESH X.MIN=0.0 X.MAX=1.0 H1=0.1
X.MESH X.MIN=1.0 X.MAX=4.5 H1=0.25

Y.MESH N=1 L=-0.50
Y.MESH N=2 L=-0.20
Y.MESH N=3 L=0.0

Y.MESH  DEPTH=0.4 H1=0.1
Y.MESH  DEPTH=0.01 H1=0.005
Y.MESH  DEPTH=0.09 H1=0.03
Y.MESH  DEPTH=2.0 H1=0.25
Y.MESH  DEPTH=2.0 H1=0.25

COMMENT *** Specify oxide and silicon regions ***
REGION  SILICON
REGION  OXIDE Y.MIN=0.5 Y.MAX=2.5
REGION  OXIDE IY.MIN=1 IY.MAX=3

COMMENT *** Electrode definition ***
ELECTR  NAME=Ahb X.MIN=0.0 X.MAX=1.0 IY.MIN=1 IY.MAX=3
ELECTR  NAME=Ahb X.MIN=0.0 X.MAX=1.0 Y.MIN=0.0 Y.MAX=0.4
ELECTR  NAME=Ahb X.MIN=1.0 X.MAX=3.5 IY.MIN=1 IY.MAX=2
ELECTR  NAME=Alb X.MIN=0.0 X.MAX=0.5 Y.MIN=0.41 Y.MAX=0.5

ELECTR  NAME=Cathode X.MIN=4.25 X.MAX=4.5 IY.MIN=1 IY.MAX=3
ELECTR  NAME=Sub BOTTOM

COMMENT *** Specify impurity profile ***
PROFILE N-TYPE N.PEAK=5E16 UNIFORM X.MIN=0.0 X.MAX=4.0 Y.MIN=0.0 Y.MAX=0.5
+          OUT.FILE=ldssDS
PROFILE N-TYPE N.PEAK=1E20 UNIFORM X.MIN=4.0 X.MAX=4.5 Y.MIN=0.0 Y.MAX=0.5
PROFILE N-TYPE N.PEAK=5E16 UNIFORM X.MIN=0.0 X.MAX=4.5 Y.MIN=2.5 Y.MAX=4.5

COMMENT *** Initial Grid ***
PLOT.2D          GRID TITLE="LDSS - INITIAL GRID" FILL SCALE

COMMENT *** Regrid on doping ***
REGRID           DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=1
+      IN.FILE=ldssDS
PLOT.2D GRID TITLE="LDSS - DOPED GRID" FILL SCALE

COMMENT *** Specify contact parameters ***
CONTACT NAME=Alb WORKFUNC=4.74 SURF.REC BARRIERL ALPHA=2E-7
CONTACT NAME=Ahb WORKFUNC=4.84 SURF.REC BARRIERL ALPHA=2E-7
CONTACT NAME=Cathode

COMMENT   *** Specify material parameters ***
MATERIAL  REGION=SILICON TAUN0=1E-6  TAUP0=1E-6

COMMENT *** Specify physical models ***
MODELS  FERMIDIR CONMOB FLDMOB CONSRH IMPACT.I
```

```
COMMENT *** Symbolic factorization, solve, regrid on potential ***
SYMB   CARRIERS=0
METHOD ICCG DAMPED
SOLVE
REGRID  POTEN IGNORE=OXIDE RATIO=.25 MAX=1 SMOOTH=1
+     IN.FILE=ldssDS
+     OUT.FILE=ldssMS
PLOT.2D GRID TITLE="LDSS - POTENTIAL REGRID" FILL SCALE

COMMENT *** Solve using refined grid save solution for later use ***
SYMB   CARRIERS=0
SOLVE   OUT.FILE=ldssS

COMMENT *** Impurity profile plots ***
PLOT.1D DOPING X.START=2.0 X.END=2.0 Y.START=0 Y.END=4.5
+          Y.LOG POINTS BOT=1E15 TOP=1E21 COLOR=2
+          TITLE= "LDSS - IMPURITY PROFILE NEAR ANODE"

PLOT.1D DOPING X.START=4.25 X.END=4.25 Y.START=0.0 Y.END=4.5
+          Y.LOG POINTS BOT=1E15 TOP=1E21 COLOR=2
+          TITLE= "LDSS - IMPURITY PROFILE NEAR CATHODE"

COMMENT       *** Forward characteristics ***

COMMENT       *** Read in simulation mesh ***
MESH   IN.FILE=ldssMS

COMMENT       *** Read in saved solution ***
LOAD   IN.FILE=ldssS

COMMENT       *** Use Newtons method ***
SYMB   NEWTON CARRIERS=2

COMMENT *** Setup log file for IV data ***
LOG      OUT.FILE=LDSSF

COMMENT *** Solve for Cathode=0.0 and then ramp Alb and Ahb ***
SOLVE  V(Cathode)=0.0 V(Sub)=0.0
SOLVE  V(Alb)=0 V(Ahb)=0.0 ELECTR="(Alb,Ahb)" VSTEP=.005 NSTEP=120

COMMENT       *** Plot If vs. Vf ***
EXTRACT       NAME=If UNITS=Amp/um EXPRESS="@I(Alb)+@I(Ahb)"
PLOT.1D       IN.FILE=LDSSF Y.AXIS=If X.AXIS=V(Alb)
+          CURVE COLOR=1 Y.LOG
+          TITLE="FORWARD CHARACTERISTICS"

COMMENT       *** Plot Jf vs. Vf ***
EXTRACT       NAME=Jf UNITS=Amp/Cm2 EXPRESS="(@I(Alb)+@I(Ahb))*(1E8)*2"
PLOT.1D       IN.FILE=LDSSF Y.AXIS=Jf X.AXIS=V(Alb)
+          CURVE COLOR=2 Y.LOG
+          BOTTOM=1E-3 TOP=1E4 LEFT=0.0 RIGHT=1.0
+          TITLE="FORWARD CHARACTERISTICS" OUT.FILE=SILDSSJF.DAT
```

```
COMMENT       *** Reverse characteristics ***

COMMENT       *** Read in simulation mesh ***
MESH   IN.FILE=ldssMS
COMMENT       *** Read in saved solution ***
LOAD   IN.FILE=ldssS

COMMENT       *** Use newtons method ***
SYMB   NEWTON CARRIERS=2

COMMENT *** Setup log file for IV data ***
LOG     OUT.FILE=LDSSR

METHOD  ICCG DAMPED CONT.STK=8
COMMENT SOLVE FOR Alb=0.0 AND THEN RAMP Cathode
SOLVE  V(Cathode)=0 V(Sub)=0.0
SOLVE  V(Alb)=0.0 V(Ahb)=0.0 ELECTR="(Alb, Ahb)" VSTEP=-1 NSTEP=60

COMMENT       *** Plot Ir vs. Vr ***
EXTRACT       NAME=Ir UNITS=Amp/um EXPRESS="(@I(Ahb)+@I(Alb))"
EXTRACT       NAME=Vr UNITS=Volt EXPRESS=(-1)*(@V(Ahb))
PLOT.1D       IN.FILE=LDSSR Y.AXIS=Ir X.AXIS=Vr
+         CURVE COLOR=1 Y.LOG
+         TITLE="REVERSE CHARACTERISTICS"

COMMENT       *** Plot Jr vs. Vr ***
EXTRACT       NAME=Jr UNITS=Amp/Cm2 EXPRESS="(@I(Ahb)+@I(Alb))*(1E8)*(-2)"
EXTRACT       NAME=Vr UNITS=Volt EXPRESS=(-1)*(@V(Ahb))
PLOT.1D       IN.FILE=LDSSR Y.AXIS=Jr X.AXIS=Vr
+         CURVE COLOR=2 Y.LOG
+         BOTTOM=1E-5 TOP=1E2 LEFT=0.0 RIGHT=100
+         TITLE="REVERSE CHARACTERISTICS" OUT.FILE=SILDSSJR.DAT

COMMENT   *** E.FIELD at the Si and SiO2 interface ***
PLOT.1D   E.FIELD  X.START=0    X.END=4.5    Y.START=0  Y.END=0
+       COLOR=2  POINTS  TITLE="Electric field "    OUT.FILE=SEFLDSS.DAT

STOP
```

APPENDIX – C

```
go atlas
TITLE SiC emitter and SiGe base SCBT on SOI device simulation (NPM): Gummel plot

#
mesh   space.mult=1.0
#
#
x.mesh loc=0.00    spac=0.50
x.mesh loc=3.50    spac=0.50
x.mesh loc=3.50    spac=0.10
x.mesh loc=3.80    spac=0.10
x.mesh loc=3.80    spac=0.025
x.mesh loc=3.90    spac=0.025
x.mesh loc=3.90    spac=0.10
x.mesh loc=4.20    spac=0.10
x.mesh loc=4.50    spac=0.10
x.mesh loc=4.50    spac=0.50
x.mesh loc=6       spac=0.50
x.mesh loc=11      spac=0.50
#
#
y.mesh loc=0.00    spac=0.06
y.mesh loc=0.18    spac=0.06
y.mesh loc=0.18    spac=0.02
y.mesh loc=0.38    spac=0.02
y.mesh loc=0.38    spac=0.20
y.mesh loc=0.78    spac=0.20
y.mesh loc=1.28    spac=0.20
#
#
eliminate columns y.max=0.18 x.min=4.4 x.max=7
eliminate columns y.min=0.58
eliminate columns y.min=0.58
#
#
region    num=1  silicon
region    num=2  sio2   y.min=0.00   y.max=0.18
region    num=3  sio2   y.min=0.38   y.max=0.78
region     num=4  poly   y.min=0.12   y.max=0.18  x.min=3.90 x.max=4.10
region     num=5 material=b-sic x.max=3.80   y.min=0.18  y.max=0.38
region     num=6 material=SiGe  x.min=3.80   x.max=4.20  y.min=0.18 y.max=0.38
x.com=0.20
#
#
#          define the electrodes
#
electrode   name=emitter     x.min=1.50  x.max=2.50   y.max=0.18
electrode   name=base        x.min=3.90  x.max=4.10   y.max=0.12
electrode   name=collector   x.min=4.20  y.max=0.38
electrode   substrate
#
```

```
#
#         define the doping concentrations
#
doping  reg=1       uniform conc=4.5e14  n.type  outf=/home/data/linga/lsic/npmsic_1.dop
doping  reg=4       uniform conc=1.25e20 p.type
doping  reg=5       uniform conc=5e19    n.type
doping  reg=6       uniform conc=5e17    p.type
#

save      outf=/home/data/linga/lsic/npmsic_initial.str
regrid  ignore=6 doping   ratio=3.00  logarithm max.level=2 smooth.k=4 \
      dopfile=/home/data/linga/lsic/npmsic_1.dop
outf=/home/data/linga/lsic/npmsic_regrid.str

material reg=1    taup0=1.5e-5      taun0=1.5e-5     nsrhn=1e22 nsrhp=1e22
material reg=4    taup0=5e-9        taun0=5e-9       nsrhn=1e22 nsrhp=1e22
material reg=5    taun0=2e-6        taup0=2e-6       nsrhn=1e22 nsrhp=1e22
material reg=6    taup0=6e-7        taun0=6e-7       nsrhn=1e22 nsrhp=1e22

material material=b-sic egalpha=3.3e-4 nc300=7.68e18 nv300=4.76e18 permittivity=9.66
eg300=3.2 affinity=3.9 edb=0.065 eab=0.191 arichn=140 arichp=32

material material=SiGe  permittivity=12.64

models   material=b-sic fldmob arora analytic  consrh auger bgn fermi incomplete ionize print
temperature=300

models   material=SiGe conmob fldmob kla consrh klaaug bgn fermi print

impact   selb

contact  name=base   p.poly   surf.rec
contact  name=collector surf.rec barrier workfunction=4.34
output   con.band   val.band   e.field

solve init
save  outf=/home/data/linga/lsic/npmsic_0.str master

method newton autonr trap maxtraps=10

solve init
solve vcollector=1.0

Log   outf=/home/data/linga/lsic/npmsic_gp.log master
Save  outf=/home/data/linga/lsic/npmsic_1.str master
Solve vbase=0.1 vstep=0.1 vfinal=0.4 name=base
Solve vbase=0.5 vstep=0.025 vfinal=1.80 name=base

extract name="beta" max(curve(i."collector", i."collector"/ i."base")) outf="beta_sic.dat"
extract name="gpb" max(curve(v."base", i."base")) outf="gpb_sic.dat"
extract name="gpc" max(curve(v."base", i."collector")) outf="gpc_sic.dat"
#
```

```
#
#       /*** IV characteristics ***/
#
#       I_C/V_CE with constant IB
#       ramp Vb
solve init
solve vbase=0.025
solve vbase=0.05
solve  vbase=0.1 vstep=0.1 vfinal=0.9 name=base
#
#       switch to current boundary conditions
contact name=base current
#       ramp IB and save solutions
solve ibase=5e-12
save  outf=/home/data/linga/lsic/npmsic_iv_0.str master

solve ibase=5e-9
save  outf=/home/data/linga/lsic/npmsic_iv_1.str master

solve ibase=10e-9
save  outf=/home/data/linga/lsic/npmsic_iv_2.str master

solve ibase=15e-9
save  outf=/home/data/linga/lsic/npmsic_iv_3.str master

solve ibase=20e-9
save  outf=/home/data/linga/lsic/npmsic_iv_4.str master

load  inf=/home/data/linga/lsic/npmsic_iv_0.str master
log   outf=/home/data/linga/lsic/npmsic_iv_0.log
solve vcollector=0.0  vstep=0.025  vfinal=0.5 name=collector
solve vcollector=0.5 vstep=0.0625 vfinal=2.25 name=collector
solve vcollector=2.25 vstep=0.0625 vfinal=3.0 name=collector
extract name="iv0" max(curve(v."collector", i."collector")) outf="npmsiciv0.dat"

load  inf=/home/data/linga/lsic/npmsic_iv_1.str master
log   outf=/home/data/linga/lsic/npmsic_iv_1.log
solve vcollector=0.0  vstep=0.025  vfinal=0.5 name=collector
solve vcollector=0.5 vstep=0.0625 vfinal=3.0 name=collector
extract name="iv1" max(curve(v."collector", i."collector")) outf="npmsiciv1.dat"

load  inf=/home/data/linga/lsic/npmsic_iv_2.str master
log   outf=/home/data/linga/lsic/npmsic_iv_2.log
solve vcollector=0.0  vstep=0.025  vfinal=0.5 name=collector
solve vcollector=0.6 vstep=0.0625 vfinal=3.0 name=collector
extract name="iv2" max(curve(v."collector", i."collector")) outf="npmsiciv2.dat"

load  inf=/home/data/linga/lsic/npmsic_iv_3.str master
log   outf=/home/data/linga/lsic/npmsic_iv_3.log
solve vcollector=0.0  vstep=0.025  vfinal=0.5 name=collector
solve vcollector=0.6 vstep=0.0625 vfinal=3.0 name=collector
extract name="iv3" max(curve(v."collector", i."collector")) outf="npmsiciv3.dat"

load  inf=/home/data/linga/lsic/npmsic_iv_4.str master
log   outf=/home/data/linga/lsic/npmsic_iv_4.log
```

```
solve vcollector=0.0 vstep=0.025  vfinal=0.5 name=collector
solve vcollector=0.6 vstep=0.0625 vfinal=3.0 name=collector
extract name="iv4" max(curve(v."collector", i."collector")) outf="npmsiciv4.dat"
#
#
#          /*** ft calculation ***/
#
solve init
solve vcollector=1.0
solve vbase=0.01
solve vbase=0.05
Log   outf=/home/data/linga/lsic/npmsic_ft.log master
Save  outf=/home/data/linga/lsic/npmsic_1.str master
Solve vbase=0.1 vstep=0.1 vfinal=0.4 name=base ac freq=1e6 aname=base
Solve vbase=0.5 vstep=0.025 vfinal=2.0 name=base ac freq=1e6 aname=base

extract name="ft" max(curve(i."collector", g."collector""base"/(6.18*c."base" "base")))
outf="npmsic_ft.dat"
#
#
#          /*** Transient analysic ***/
#
#          contact resistance definition
contact name=base resistance=1e5
contact name=collector resistance=50e3
#
method 2nd tauto autonr
#          collector voltage is kept at 2 volt
solve prev
solve vbase=0 vcollector=2

#          reverse recovery time is stored in the log file
log outf=/home/data/linga/lsic/npmsicstran_100.log master

#          Pulse is applied at the base with rise and fall time=1nanosecond
solve vbase=5 dt=1e-12 ramptime=1e-9 tstop=1e-9
solve vbase=5 tstop=5e-9

solve vbase=-0.5 dt=1e-12 ramptime=1e-9 tstop=6e-9
solve vbase=-0.5 tstop=20e-9

extract name="npmsicrrt"  max(curve("Transient time", i."base")) outf="npmsicrrt.dat"
#
quit
```

APPENDIX – D

```
go atlas
TITLE 0.15 SiC emitter and 0.05 Silicon emitter SiGe base SCBT on SOI device simulation
(PNM): Gummel plot

#
mesh   space.mult=1.0
#
#
x.mesh loc=0.00    spac=0.50
x.mesh loc=3.50    spac=0.50
x.mesh loc=3.50    spac=0.10
x.mesh loc=3.80    spac=0.10
x.mesh loc=3.80    spac=0.02
x.mesh loc=3.90    spac=0.02
x.mesh loc=3.90    spac=0.10
x.mesh loc=4.20    spac=0.10
x.mesh loc=4.50    spac=0.10
x.mesh loc=4.50    spac=0.50
x.mesh loc=6.00    spac=0.50
x.mesh loc=11.0    spac=0.50
#
#
y.mesh loc=0.00    spac=0.06
y.mesh loc=0.18    spac=0.06
y.mesh loc=0.18    spac=0.025
y.mesh loc=0.38    spac=0.025
y.mesh loc=0.38    spac=0.20
y.mesh loc=0.78    spac=0.20
y.mesh loc=1.28    spac=0.20
#
#
eliminate columns y.max=0.18 x.min=4.4 x.max=7
eliminate columns y.min=0.58
eliminate columns y.min=0.58
#
#
region      num=1  silicon
region      num=2  sio2   y.min=0.00   y.max=0.18
region      num=3  sio2   y.min=0.38   y.max=0.78
region       num=4  poly   y.min=0.06   y.max=0.18  x.min=3.90 x.max=4.10
region       num=5 material=b-sic x.max=3.80   y.min=0.18  y.max=0.33
region       num=6 material=SiGe  x.min=3.80   x.max=4.20  y.min=0.18 y.max=0.38
x.com=0.20
region       num=7 material=silicon x.max=3.80   y.min=0.33  y.max=0.38
#
#
#          define the electrodes
#
electrode   name=emitter     x.min=0.00  x.max=1.00   y.max=0.38
electrode   name=base        x.min=3.90  x.max=4.10   y.max=0.06
electrode   name=collector   x.min=4.20  y.max=0.38
```

```
electrode   substrate
#
#          define the doping concentrations
#
doping  reg=1       uniform conc=4.5e14  n.type
outf=/home/data/linga/offplay/pnmsic_.05sie_1.dop
doping  reg=4       uniform conc=1e20    n.type
doping  reg=5       uniform conc=5e19    p.type
doping  reg=6       uniform conc=5e17    n.type
doping  reg=7       uniform conc=5e19    p.type
#

save      outf=/home/data/linga/offplay/pnmsic_.05sie_initial.str
regrid  ignore=6 doping   ratio=3.00  logarithm max.level=2 smooth.k=4 \
       dopfile=/home/data/linga/offplay/pnmsic_.05sie_1.dop
outf=/home/data/linga/offplay/pnmsic_.05sie_regrid.str

material reg=1    taup0=1.5e-5       taun0=1.5e-5     nsrhn=1e22 nsrhp=1e22
material reg=4    taup0=5.32e-10     taun0=5.32e-10   nsrhn=1e22 nsrhp=1e22
material reg=5    taun0=0.4e-6       taup0=0.4e-6     nsrhn=1e22 nsrhp=1e22
material reg=6    taup0=2.29e-6      taun0=2.29e-6    nsrhn=1e22 nsrhp=1e22
material reg=7    taun0=2.45e-9      taup0=2.45e-9    nsrhn=1e22 nsrhp=1e22

material material=b-sic egalpha=3.3e-4 nc300=7.68e18 nv300=4.76e18 permittivity=9.66
eg300=3.2 affinity=3.9 edb=0.065 eab=0.191 arichn=140 arichp=32

material material=SiGe  permittivity=12.64

models material=b-sic fldmob arora analytic  consrh auger bgn fermi incomplete ionize print
temperature=300

models conmob fldmob kla consrh klaaug bgn fermi print

impact   selb

contact  name=base   n.poly   surf.rec
contact  name=collector surf.rec barrier workfunction=5.02
output   con.band   val.band   e.field

solve  init
save   outf=/home/data/linga/offplay/pnmsic_.05sie_0.str master
method newton autonr trap maxtraps=10

solve init
solve vcollector=0.0 vstep=-0.0625 vfinal=-1.0 name=collector
log   outf=/home/data/linga/offplay/pnmsic_.05sie_gp.log master
save  outf=/home/data/linga/offplay/pnmsic_.05sie_1.str master
solve vemitter=0.0 vstep=0.025 vfinal=0.5 name=emitter
solve vemitter=0.5 vstep=0.025 vfinal=3.0 name=emitter

extract name="pnmsic_.05sie_beta" max(curve( i."collector", i."collector"/ i."base"))
outf="pnmsic_.05sie_beta.dat"
extract name="pnmsic_.05sie_gpb" max(curve(v."emitter", i."base"))
outf="pnmsic_.05sie_gpb.dat"
```

```
extract name="pnmsic_.05sie_gpc" max(curve(v."emitter", i."collector"))
outf="pnmsic_.05sie_gpc.dat"

#       /*** IV characteristics ***/
#
#       I_C/V_CE with constant IB
#       ramp Vb
solve init
solve vbase=-0.025
solve vbase=-0.05
#
solve  vbase=-0.1 vstep=-0.1 vfinal=-0.9 name=base

#       switch to current boundary conditions
contact name=base current

#       ramp IB and save solutions
solve ibase=-5e-13
save  outf=/home/data/linga/offplay/pnmsic_.05sie_iv_0.str master

solve ibase=-5e-9
save  outf=/home/data/linga/offplay/pnmsic_.05sie_iv_1.str master

solve ibase=-10e-9
save  outf=/home/data/linga/offplay/pnmsic_.05sie_iv_2.str master

solve ibase=-15e-9
save  outf=/home/data/linga/offplay/pnmsic_.05sie_iv_3.str master

solve ibase=-20e-9
save  outf=/home/data/linga/offplay/pnmsic_.05sie_iv_4.str master

# load in each initial guess file and ramp V_CE
load  inf=/home/data/linga/offplay/pnmsic_.05sie_iv_0.str master
log   outf=/home/data/linga/offplay/pnmsic_.05sie_iv_0.log
solve vcollector=0.0  vstep=-0.025  vfinal=-0.5 name=collector
solve vcollector=-0.5 vstep=-0.025 vfinal=-2.25 name=collector
solve vcollector=-2.25 vstep=-0.025 vfinal=-2.5 name=collector
extract name="iv0" max(curve(v."collector", i."collector")) outf="pnmsic_.05sie_iv0.dat"

load  inf=/home/data/linga/offplay/pnmsic_.05sie_iv_1.str master
log   outf=/home/data/linga/offplay/pnmsic_.05sie_iv_1.log
solve vcollector=0.0  vstep=-0.025  vfinal=-0.5 name=collector
solve vcollector=-0.5 vstep=-0.025 vfinal=-2.5 name=collector
extract name="iv1" max(curve(v."collector", i."collector")) outf="pnmsic_.05sie_iv1.dat"

load  inf=/home/data/linga/offplay/pnmsic_.05sie_iv_2.str master
log   outf=/home/data/linga/offplay/pnmsic_.05sie_iv_2.log
solve vcollector=0.0  vstep=-0.025  vfinal=-0.5 name=collector
solve vcollector=-0.5 vstep=-0.025 vfinal=-2.5 name=collector
extract name="iv2" max(curve(v."collector", i."collector")) outf="pnmsic_.05sie_iv2.dat"
load  inf=/home/data/linga/offplay/pnmsic_.05sie_iv_3.str master
log   outf=/home/data/linga/offplay/pnmsic_.05sie_iv_3.log
solve vcollector=0.0  vstep=-0.025  vfinal=-0.5 name=collector
solve vcollector=-0.5 vstep=-0.025 vfinal=-2.5 name=collector
```

```
extract name="iv3" max(curve(v."collector", i."collector")) outf="pnmsic_.05sie_iv3.dat"

load  inf=/home/data/linga/offplay/pnmsic_.05sie_iv_4.str master
log   outf=/home/data/linga/offplay/pnmsic_.05sie_iv_4.log
solve vcollector=0.0 vstep=-0.025  vfinal=-0.5 name=collector
solve vcollector=-0.5 vstep=-0.025 vfinal=-2.5 name=collector
extract name="iv4" max(curve(v."collector", i."collector")) outf="pnmsic_.05sie_iv4.dat"
#
#
#          /*** ft calculation ***/
#
solve init
solve vcollector=-1.0
solve vbase=-0.01
solve vbase=-0.025
Log outf=/home/data/linga/offplay/pnmsic_.05sie_ft.log master
Save outf=/home/data/linga/offplay/pnmsic_.05sie_1.str master
Solve vbase=-0.05 vstep=-0.025 vfinal=-0.5 name=base ac freq=1e6 aname=base
Solve vbase=-0.5 vstep=-0.025 vfinal=-2.5 name=base ac freq=1e6 aname=base

extract name="pnmsic_.05sie_ft" max(curve(i."collector", g."collector""base"/(6.18*c."base"
"base"))) outf="pnmsic_.05sie_ft.dat"
#
#
#          /*** Transient analysis ***/
#
#*** contact resistance definition ***
contact name=base resistance=1e5
contact name=collector resistance=50e3
method 2nd tauto autonr
#*** Collector voltage is kept at -2 volt ***
solve prev
solve vbase=0 vcollector=-2

#*** Reverse recovery time is stored in the log file ***
log outf=/home/data/linga/offplay/pnmsic_.05sie_tran.log master

#*** Pulse is applied at the base with rise and fall time=1nanosecond
solve vbase=-5 dt=1e-12 ramptime=1e-9 tstop=1e-9
solve vbase=-5 tstop=5e-9
solve vbase=0.5 dt=1e-12 ramptime=1e-9 tstop=6e-9
solve vbase=0.5 tstop=20e-9
extract name="pnmsic_.05sie_rrt"  max(curve("Transient time", i."base"))
outf="pnmsic_.05sie_rrt.dat"
#
quit
```

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Publications from this work

1. M. Jagadesh Kumar and C. Linga Reddy, "A Novel 4H-SiC Lateral Dual Sidewall Schottky Rectifier with excellent forward and reverse characteristics," *IASTED International Conference on Circuits, Signals, and Systems (CSS' 03)* Cancun, Mexico, May 19-21, 2003.

2. M. Jagadesh Kumar and C. Linga Reddy, "A New High Voltage 4H-SiC Lateral Dual Sidewall Schottky (LDSS) Rectifier: Theoretical Investigation and Analysis," To appear in *IEEE Transactions on Electron Devices,* Vol.50, July 2003.

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