Abstract—In this paper, we report a new Surface Accumulation Layer Transistor (SALTran) on SOI which uses the concept of surface accumulation of electrons near the emitter contact to improve the current gain significantly. Using two-dimensional process and device simulation, the performance of the proposed device has been evaluated in detail by comparing its characteristics with those of the previously published conventional bipolar transistor structure. From our simulation results, it is observed that depending on the choice of emitter doping and emitter length, the proposed SALTran exhibits a current gain enhancement of 10 to 70 times that of the compatible bipolar transistor. We also demonstrate that the presence of the surface accumulation layer does not deteriorate the cut-off frequency as observed in the high–low emitter junction bipolar transistors. Our simulations also indicate that when the emitter is lightly doped, the SALTran is immune to hot carrier injection problems due to the reduced electric field in the emitter. The effect of surface states at the emitter contact and temperature on current gain have been examined.

Index Terms—Bipolar transistor, current gain, reflecting boundary, hot-carrier degradation, temperature effects.

I. INTRODUCTION

In many analog applications, such as accurate current mirrors, variable gain amplifiers bandgap voltage references and other high-speed mixed-signal circuits, bipolar transistors on SOI have been found to be of great interest with the advent of BiCMOS technologies. The advantages of BJTs over MOSFETs and the inherent isolation possible with the SOI devices led to the emergence of SOI-based BiCMOS technologies where both BJTs and MOSFETs can be fabricated on the same chip. In comparison to vertical bipolar devices, lateral bipolar transistors can be processed in a simpler technology with smaller parasitic transistor regions, making them particularly suitable for low-power wireless applications [1]–[3].

One of the crucial design parameters in a bipolar transistor is the current gain. A large current gain can be traded off against increased base doping to alleviate the problems associated with elevated base sheet resistance commonly observed in high-performance BJTs [4]. Current gain of a BJT can be increased by using a polysilicon emitter [5] or a SiGe base [6]. Both these techniques are widely used even though they require complex process steps. Another technique which has been reported to increase the current gain of a bipolar transistor is the application of low-high emitter junction [7], [8]. However, in the high–low emitter structures, the cut-off frequency deteriorates due to the increase of minority carrier transit time caused by the presence of the high–low junction [8]. It would be of great practical importance if the current gain of a BJT could be enhanced using a simple emitter contact concept while obviating the above shortcomings.

The aim of this work is to present, for the first time, a new technique of increasing the current gain of a bipolar transistor using a concept called the Surface Accumulation Layer Transistor (or SALTran). The process steps in the SALTran are similar to that of a conventional bipolar transistor except that in the SALTran, a lightly doped emitter with a metal contact, whose workfunction is less than that of silicon, is employed. This results in a reflecting boundary at the emitter contact for the minority holes injected into the emitter from the base region resulting in a significant reduction in the base current. By using two-dimensional process and device simulation, we show that the SALTran is superior in performance as compared to an equivalent npn BJT in respect of high current gain and cut-off frequency. We further demonstrate that unlike in the case of high–low emitter bipolar transistors, the cut-off frequency of the SALTran does not degrade by the presence of the reflecting boundary in the emitter if appropriate emitter doping and length are used.

This paper is organized as follows. We first discuss the SALTran concept in Section II, followed by the design methodology in Section III. Profile design using the process simulator is explained in Section IV. The simulation results are presented in Section V, which also includes an analysis of the dependence of current gain on temperature. The surface states at the metal–semiconductor contact are also analyzed. The reasons for the improved performance are explained in detail.

II. SURFACE ACCUMULATION LAYER TRANSISTOR (SALTRAN) CONCEPT

The SALTran is based on the concept that when a metal of low workfunction is brought in contact with a lightly doped n-type semiconductor having a high workfunction, an accumulation of electrons occurs in the semiconductor near the metal–semiconductor interface [9], as shown in Fig. 1. This results in an electric field due to the electron concentration gradient from the
metal–semiconductor interface toward the emitter–base junction. The direction of this field is such that it causes reflection of the minority holes injected from the base into the emitter, resulting in a reduced hole concentration gradient in the emitter region. As a consequence, the application of such a reflecting boundary to the holes at the emitter contact should result in a reduced base current, leading to a significant improvement in the current gain.

We establish in the following sections that the above forecast is indeed valid if a low emitter doping and an emitter metal contact of appropriate workfunction are chosen so that it results in a reflecting boundary to the holes at the emitter contact. Taking the room-temperature electron affinity and the bandgap of silicon to be $\chi_s = 4.05$ eV and $E_G = 1.12$ eV, respectively, and assuming that the metal work function $\phi_M$ is more than $\chi_s$, we can show that the emitter doping concentration $N_D$ below which the contact becomes a reflecting boundary for minority carriers can be given as

$$N_D = n_i \exp \left[ \frac{\chi_s + (E_C - E_i) - \phi_M}{k_BT} \right]$$

$$= n_i \exp \left[ \frac{4.61 \text{ eV} - \phi_M}{k_BT} \right]$$

(1)

where $E_C$ is the conduction band energy, $E_i$ is the intrinsic Fermi level, $n_i$ is the intrinsic carrier concentration, $k_B$ is the Boltzmann constant, and $T$ is the temperature in degrees Kelvin. For example, if aluminum is used for the metal contact, the emitter doping should be approximately $\leq 3.56 \times 10^{19}$/cm$^3$ for realizing a reflecting boundary to the holes at the emitter contact.

In the following sections, we shall demonstrate using accurate two-dimensional process and device simulations that the application of surface accumulation layer emitter contact does indeed enhance the bipolar transistor performance significantly.

### III. Design Methodology of SALTRAN

To demonstrate the SALTRAN concept on SOI and to calibrate our device simulations, we have first chosen an experimental process for an SOI npn lateral bipolar transistor (LBT) [10]. The top layout and the schematic cross-section of the SALTRAN and the LBT are shown in Fig. 2. For both the structures, we chose the epitaxial silicon film thickness as 0.2 $\mu$m, the oxide thickness as 0.38 $\mu$m, the p-base width as 0.4 $\mu$m with a peak doping level of $5 \times 10^{17}$/cm$^3$, the collector drift region width as 1.6 $\mu$m with a doping level of $4.5 \times 10^{14}$/cm$^3$, and the n$^+$ collector doping as $5 \times 10^{19}$/cm$^3$. In the case of LBT, the emitter n-region has a doping of $5 \times 10^{19}$/cm$^3$ with 0.3-$\mu$m length, while for the SALTRAN, we have varied the emitter doping from $4.5 \times 10^{14}$/cm$^3$ to $10^{19}$/cm$^3$, keeping the emitter length at 0.3 $\mu$m. We have implemented the fabrication steps of [10] in the process simulator ATHENA [11] and imported the structure and doping profiles into the device simulator ATLAS [12]. We have calibrated the default model parameters in ATLAS such that the simulated current gain and the cut-off frequency of the LBT match with the reported values [10] for the device dimensions (i.e., emitter length of 5.6 $\mu$m and all the other parameters as given above). We have then carried out the process simulation for the SALTRAN with different emitter dopings and emitter lengths, keeping all the other process steps
and device data the same as those of the reported LBT so that our simulations are well validated.

IV. PROFILE DESIGN USING THE PROCESS SIMULATOR ATHENA

We have used the following process steps in ATHENA to design the doping profiles for both the LBT and the SALTran. First, the n⁺ collector implant was done with a phosphorus dose of $5 \times 10^{14}$ cm$^{-2}$ at 100 keV after patterning of the deposited silicon nitride. Then, a 0.8-$\mu$m-thick CVD-oxide is deposited, patterned, and etched. Next, a screen oxide of 0.03-$\mu$m thickness is deposited, followed by a 0.24-$\mu$m-thick CVD-nitride deposition and etching to form a spacer. Following this, the emitter is formed by implanting phosphorus with a dose of $2.5 \times 10^{13}$ cm$^{-2}$ and an energy of 50 keV while the base region is protected by the spacer. The emitter is then driven in for 1 h at 965 °C in nitrogen followed by LOCOS for 1 h in wet oxygen at 900 °C to give a 0.18-$\mu$m-thick oxide over emitter. After opening the base area by a wet chemical etch and removal of the nitride spacer by phosphoric acid, three subsequent boron implants of $3 \times 10^{12}$ cm$^{-2}$ at 60 keV, $3 \times 10^{12}$ cm$^{-2}$ at 20 keV, and $5 \times 10^{12}$ cm$^{-2}$ at 20 keV are performed. Next, annealings at 965 °C for 20 min and at 800 °C for 60 min are done. This is followed by the deposition of a polysilicon layer of 0.3-$\mu$m thickness and doping by boron implantation of dose $2.5 \times 10^{15}$ cm$^{-2}$ with 70 keV energy and, finally, annealing at 850 °C for 80 min. The oxide layer is etched followed by silicon etching on the side of the emitter and the metal was deposited and patterned for providing the emitter contact. The final structure looks as shown in Fig. 2. The process for the LBT is the same as that of the SALTran except that the emitter implant dose and the nitride spacer width are $2.5 \times 10^{15}$ cm$^{-2}$ and 0.34 $\mu$m, respectively, in the case of the LBT. As an example, the final doping profiles of the SALTran and the LBT obtained by using the above process in ATHENA [11] are shown in Fig. 3 for an emitter doping of $10^{18}$ cm$^{-3}$. We have adjusted the process parameters to obtain different emitter doping values between $4.5 \times 10^{14}$ and $10^{18}$ cm$^{-3}$. This doping data is given as an input to the device simulator ATLAS [12] to evaluate the electrical characteristics of both the structures, as discussed in the following section.

V. SIMULATION RESULTS AND DISCUSSION

A. Device Characteristics

In our simulations, we have used suitable models for the bandgap narrowing, SRH and Auger recombination, and the concentration and field dependent mobility. The simulation parameters are given in Table I. The simulated output characteristics of the SALTran and the LBT are shown in Fig. 4. The emitter doping of the SALTran is $4.5 \times 10^{14}$ cm$^{-3}$ and the emitter length is 0.3 $\mu$m. It is clearly seen that SALTran has a higher current driving capability than the LBT for a given base current. The Gummel plot shown in Fig. 5(a) for two emitter dopings of the SALTran with an emitter length of 0.3 $\mu$m indicates that the base current of the SALTran is much smaller than that of the LBT resulting in an enhanced current gain, as shown in Fig. 5(b). We further notice that with the reduction in emitter doping from $10^{18}$ cm$^{-3}$ to $4.5 \times 10^{14}$ cm$^{-3}$, the base current decreases significantly resulting in a drastic improvement in the current gain. The ideality factor of the base current for the SALTran increases slightly as compared to the LBT, similar to what is observed in bipolar transistors with and without the polysilicon emitter contact [13]. This slight increase could be due to the barrier experienced by the injected holes at the emitter contact both in the case of the SALTran and the polysilicon emitter transistor. While the peak current gain of LBT is only 20, the SALTran exhibits a peak current gain.
of 200 and 1500 when the emitter doping is $10^{18}$ cm$^{-3}$ and $4.5 \times 10^{14}$ cm$^{-3}$, respectively. This significant enhancement in current gain can be understood from the electron profile and the electric field profile in the emitter region, as shown in Fig. 6. As pointed out in Section II, since we have chosen the workfunction (3.9 eV) of the emitter metal contact to be less than that of the silicon emitter region, we get an accumulation of electrons under the metal contact, as shown by the simulated electron profile in Fig. 6(a) for the SALTran structure with two different emitter dopings. In the case of LBT, since the emitter is heavily doped, the Fermi level moves closer to or above the conduction band and, therefore, the condition $\phi_m < \phi_n$ is not satisfied for the given metal. Hence, no electron accumulation is observed for the LBT even though the same metal is used for the emitter contact. The accumulated electron gradient in the SALTran results in a large electric field under the emitter, as shown in Fig. 6(b), and acts as a reflecting boundary for the holes arriving from the emitter–base junction. The base current of the SALTran will, therefore, be significantly smaller than that of the LBT, as demonstrated in the Gummel plots of Fig. 5.

The simulated cut-off frequency $f_T$ of SALTran and LBT are compared in Fig. 7. We notice that when the emitter doping of SALTran is $10^{18}$ cm$^{-3}$, the $f_T$ of SALTran is greater than that of the LBT. This is unlike the behavior shown by the high–low junction emitter bipolar transistors in which the presence of the high–low junction deteriorates the cut-off frequency due to an increase in the emitter transit time because of charge storage effects [8]. If the emitter doping is reduced to a low value ($4.5 \times 10^{14}$ cm$^{-3}$), a slight reduction in $f_T$ is observed in the case of SALTran, also indicating that one has to optimize both the emitter length and the emitter doping of SALTran to get the desired current gain enhancement without seriously affecting the cut-off frequency, as discussed next.

**B. Emitter Region Optimization**

An important aspect of the SALTran is that as the emitter length decreases, both the current gain and cutoff frequency begin to increase. A reduction in the emitter length causes the rate of reflection of the holes from the emitter to be significant. Fig. 8 shows the peak current gain variation for different emitter lengths and emitter dopings for both the SALTran and
the LBT structures. We notice that when the emitter doping is far smaller than the peak base doping, the current gain enhancement is maximum. For example, when the emitter doping is $4.5 \times 10^{24} \text{cm}^{-3}$, the current gain enhancement is largest for shallow emitter lengths, which makes the SALTran very attractive for scaled-down VLSI BJTs. We also notice that for deeper emitter lengths as well, the current gain enhancement is still impressive when the emitter is lightly doped. This is an indication that the SALTran concept can be conveniently applied to even high-voltage-power bipolar transistors in which low current gain is often a problem. In the case of the deeper emitter junctions, the current gain of the SALTran is smaller than that of the shallower emitter due to the increased emitter region recombination for the deeper emitters.

The peak cutoff frequency variation with the emitter length and the emitter doping is shown in Fig. 9. It is seen that when the emitter doping is $1 \times 10^{18} \text{cm}^{-3}$, at an emitter length of $0.5 \mu\text{m}$, the SALTran has almost the same peak cutoff frequency as that of the LBT, and at $0.3-\mu\text{m}$ emitter length, it surpasses the LBT in terms of both the current gain and the cutoff frequency. With proper optimization of the emitter length and the emitter doping, we can get both high current gain and high cutoff frequency.

VI. HOT-CARRIER INJECTION PROBLEM

In bipolar transistors, the heavy doping in the emitter and base regions results in a sufficiently large electric field even at the typical emitter–base reverse-bias voltages (<<5 V) and is the primary cause of the hot-carrier injection problem [14], [15]. In order to investigate this, we have compared the simulated reverse emitter–base characteristics of the SALTran and the LBT in Fig. 10(a). It can be seen that the low emitter doping ($4.5 \times 10^{14} \text{cm}^{-3}$) used in the SALTran, its reverse breakdown voltage is significantly larger than that of the LBT, which breaks down approximately at a reverse bias of 5.5 V. The electric field in the emitter region shown in Fig. 10(b) at the breakdown voltage of the LBT (5.5 V) clearly shows that in the case of LBT with its heavily doped emitter, there is a larger peak electric field at the emitter–base junction compared to that of the SALTran whose emitter is completely depleted because of the low doping. It may be pointed out that although the electric field at the metal–semiconductor interface of the SALTran...
is not negligible, carrier multiplication is very unlikely to take place here due to the extremely narrow thickness of the high electric field region [16]. This clearly indicates less vulnerability of the SALTran to the hot-carrier injection phenomenon if the emitter is lightly doped as compared to the LBT. In the case of the SALTran, therefore, the lightly doped emitter not only helps in realizing a large gain, it may also help in reducing the hot-carrier injection.

VII. TEMPERATURE EFFECTS ON CURRENT GAIN

The current gain of a silicon bipolar transistor increases with ambient temperature and this can cause problems in many applications. To understand the temperature effects, we have compared the current gain dependence of the SALTran with that of the LBT in Fig. 11(a) by plotting the normalized current gain as a function of temperature. We notice that the dependence of current gain on temperature is far less in the case of the SALTran as compared to the LBT.

It is well known [8] that the variation in peak current gain and the temperature can be related by \( \beta = \beta^0 \exp(\Delta E_g/k_BT) \)

where \( \beta^0 \) is the maximum current gain for activation energy \( \Delta E_g = 0 \), \( k_B \) is the Boltzmann constant, and \( T \) is the absolute temperature in degrees Kelvin. If \( E_{gb} \) and \( E_{gh} \) are the effective bandgap narrowing in the emitter and the base regions, respectively, the activation energy \( \Delta E_g \) can be obtained as \( \Delta E_g = E_{gb} - E_{gh} \). From the peak current gain variation of the SALTran and the LBT as a function of temperature, one can obtain the activation energy by plotting \( \ln(\beta) \) versus \( 1/(k_BT) \) as shown in Fig. 11(b). The activation energy for the SALTran comes out to be 30 meV and 34 meV for the emitter doping of \( 4.5 \times 10^{14} \) cm\(^{-3} \) and \( 10^{18} \) cm\(^{-3} \), respectively. The activation energy of the LBT is found to be 53 meV. This clearly shows that the SALTran can be operated at higher temperatures compared to the LBT while keeping the current gain variations much smaller than that of the LBT.

VIII. EFFECT OF INTERFACE TRAPS ON CURRENT GAIN

Since a low workfunction metal contact is employed on the lightly doped emitter of the SALTran, it is obvious that there could be interface traps at the metal–semiconductor interface depending on the surface preparation and metal deposition method employed. Both the acceptor and the donor type interface traps are known to be present, which will affect the band bending [17]. Since the band bending is crucial to create an accumulation of electrons in the SALTran, it is of practical interest to examine the extent to which the presence of interface states will affect the current gain.

While it is difficult to predict the number and the type of traps in the bandgap, which can vary from process to process, we can at least introduce in the simulator the typical range of interface traps to study their influence on the device characteristics. The effect of interface traps, for example, have been investigated earlier using simulations in the case of the Schottky junctions on silicon [18]. In the device simulator ATLAS, we have introduced both the acceptor and the donor type interface traps to see their effect on the current gain of the SALTran. For acceptor (or donor) type traps, we have set the trap energy level (E.level) at 0.49 eV from the conduction (or valence) band. The degeneracy factor (degen) for the trap level is chosen to be 12 and the capture cross-sections for electrons (sign) and holes (sigp) are taken to be \( 2.84 \times 10^{-15} \) cm\(^2 \) and \( 2.84 \times 10^{-14} \) cm\(^2 \), respectively.

Fig. 12 shows the peak current gain of the SALTran with an emitter doping of \( 4.5 \times 10^{14} \) cm\(^{-3} \) and an emitter length of 0.3 \( \mu \)m as a function of both the acceptor and the donor type traps at the interface. We observe that the current gain decreases as the interface trap concentration increases and that the effect is more pronounced if both the acceptor and the donor type traps are present. We have observed an increase in the simulated base current when the trap concentration is increased and this, therefore, will cause the current gain to decrease. However, even when the interface trap density exceeds \( 10^{10} \) cm\(^{-2} \), the current gain enhancement realized in the SALTran over that of the LBT is
approximately 40 times larger, which is very impressive. Therefore, if the surface preparation is well controlled, as is the practice in most advanced fabrication procedures, it should be possible to preserve the current gain enhancement of the SALTran. On the other hand, growing a native oxide of approximately 10–15 Å on the emitter surface using the RCA cleaning, as is commonly done in the case of polysilicon emitter bipolar transistors [13], will minimize the effect of the surface traps and may further enhance the current gain.

IX. Conclusion

For the first time, the concept of surface electron accumulation to increase the current gain and the cutoff frequency of bipolar transistors is successfully demonstrated by using two-dimensional process and device simulation. We have shown that the SALTran concept results in a reflecting boundary to the minority carriers at the emitter contact, leading to a significant improvement in the current gain of the bipolar transistors. We have also shown that the SALTran is less vulnerable to the hot-carrier injection as compared to the LBT. Our simulations show that the activation energy of the SALTran is significantly lower than that of the LBT, thus making its current gain less dependent on temperature variations. Unlike the high–low emitter bipolar transistors, the cut-off frequency of the SALTran does not deteriorate in the presence of the surface electron accumulation if an optimized emitter design is used. Since the SALTran structure obviates the need to create a high–low junction in the emitter region and since its performance improves for both the shallow and the deep emitters, the proposed SALTran concept should be useful to the designers to enhance the bipolar transistor performance in VLSI as well as high-voltage switching circuit applications.

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REFERENCES


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