Realizing high-voltage thin film lateral bipolar transistors on SOI with a collector-tub

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Abstract

Purpose – The main purpose of this paper is to find a simple method to improve the breakdown voltage of BJTs fabricated on SOI.

Design/methodology/approach – We have used two-dimensional device simulation to examine the effect of a collector tub on the collector breakdown of the SOI based BJTs. This method involves creating a collector tub by etching the buried oxide followed by an n-type implantation on the collector n/n+ junction side.

Findings – First, our method reduces the peak electric field at the silicon film-BOX interface and secondly, the collector-tub facilitates the collector potential to be absorbed by both collector drift and substrate regions improving the collector breakdown significantly.

Practical implications – An improved breakdown voltage improves the reliability of BJTs on SOI.

Originality/value – Our results show that the BVCEO of the bipolar transistors with a collector-tub is enhanced by 2.7 times when compared with a conventional lateral bipolar transistor (LBT) with identical drift region doping. This improvement has an important practical value in the fabrication of SOI-based LBTs.

Keywords Bipolar transistors, Breakdown voltage, Simulation

Paper type Research paper

1. Introduction

Thin film lateral bipolar transistors (LBTs) on silicon-on-insulator (SOI) (Baliga, 1991; Huang and Baliga, 1991; Kumar and Roulston, 1994; Ryter et al., 1996; Garner et al., 2001) have drawn wide attention in the recent past due to their compatibility with BiCMOS technology and possibility of integration in smart power ICs. This is particularly true for applications in medium voltage range (100-1,000 V) such as display driver or ballast circuits where high voltages LBTs are often used (Nagata et al., 1992; Arborg and Litwin, 1995; Gomez et al., 2000). Several studies have been conducted to improve the breakdown voltage of these LBTs, either by increasing the critical electric field for breakdown (Wondark et al., 1992; Nakagawa et al., 1991; Banna et al., 1997; Amaratunga and Udrea, 2001) or by using Redistribution of SURface Field (RESURF) principle (Merchant et al., 1991; Matsudai and Nakagawa, 1992; Lai et al., 1995; Zhang et al., 1999; Ludikhuize, 2000; Ventling et al., 2002) or using novel structures (Lu et al., 1992; Kim et al., 1994; Sunkavalli et al., 1995; Luo et al., 2003; Roig et al., 2004). However, a major problem associated with such thin silicon film (≤1 μm) on SOI, is the fact that the breakdown voltage is limited by the high electric field at the silicon film-BOX interface due to difference in dielectric constant between silicon film and BOX. The breakdown voltages, therefore, do not increase with the increase in drift region length and saturate at a lower value. This is because the device is operated with the substrate grounded and hence, the substrate-BOX interface acts as an equi-potential line and the entire collector voltage is dropped at the BOX and the silicon film on the collector high-low (NN+) junction side. This paper highlights the fact that an enhancement in the breakdown voltage is possible if a collector-tub concept is used to reduce the peak electric field at the silicon film-BOX interface, which we propose to achieve with an N-implantation at the NN+ -junction side of a conventional N⁺ PN₁ N⁺ LBT structure on SOI. Our two-dimensional simulation studies show that the presence of the collector-tub in a conventional LBT (CTLBT) enhances the collector-emitter breakdown voltage (BVCEO) by a factor of about 2.7. The paper also presents an analysis of the effect of different device parameters on the breakdown characteristics for optimum device performance of the CTLBT.

2. Simulation methodology

In order to demonstrate the efficacy of the collector-tub in enhancing the transistor performance, we have used both process as well as device simulation. We have first created the lateral bipolar transistor structure with and without the collector-tub using standard experimental parameters available in the literature (Shahidi et al., 1991; Edholm et al., 1993; Parke and Hu, 1993; Shino et al., 1998) in the two-dimensional process simulator ATHENA (Athena User’s Manual, 2000) so that the simulated device structures are close to that of an experimentally fabricated device in terms of junction depths/curvatures and impurity distribution. This structure is then imported to a two-dimensional device simulator ATLAS (Atlas User’s Manual, 2000) to evaluate the device characteristics using appropriate models as discussed in the following sections.

2.1 Process simulation to realize the device structure

To generate the CTLBT structure, we have chosen a P-type substrate (N⁺ = 5.0 × 10¹³ cm⁻³) and an N-type silicon film.
(N_D = 1.0 \times 10^{15} \text{ cm}^{-2}) on SiO_2 as the starting material in the two-dimensional process simulator ATHENA. The SOI film and BOX thickness are 1.0 and 1.2 \mu m, respectively. As shown in Figure 1, the process flow begins with the formation of the collector-tub by etching the silicon film and the BOX (Figure 1(a)) and followed by phosphorus implantation. The energy, dose, time and anneal temperature are varied to obtain different diffusion junction depths (2.8-20 \mu m). The etched region is then refilled with in situ doped N^+-polysilicon having a concentration of 5.0 \times 10^{19} \text{ cm}^{-3} (Figure 1(b)). Next the emitter and collector regions are implanted with phosphorus at a dose of 5.7 \times 10^{15} \text{ cm}^{-2} and an energy of 130 keV and annealed at a temperature of 950^\circ C for 20 min (Figure 1(c)). The base region is then opened and implanted with boron at an energy of 62 keV and a dose of 5.0 \times 10^{12} \text{ cm}^{-2} and a drive-in for 120 min at a temperature of 1,100^\circ C (Figure 1(d)). This is followed by the opening of the base contact window and deposition of 0.3 \mu m layer of in situ doped P^+-polysilicon having a concentration of 5.0 \times 10^{19} \text{ cm}^{-3} (Figure 1(e)). Finally, the emitter, base, and collector metalizations are made with Al deposition (Figure 1(f)).

The LBT structure is obtained following the same process sequence as described for the CTLBT but without the collector-tub. The overall process sequence gives the emitter/collector and base doping concentration values of 5.0 \times 10^{19} and 5.0 \times 10^{16} \text{ cm}^{-3}, respectively, and base-emitter junction depth of 7 \mu m. Figure 2 shows the generated CTLBT and LBT structures and Figure 3 their common doping profile.

2.2 Device simulation
The structures obtained in ATHENA are imported for simulation in the two-dimensional device simulator ATLAS. The various models activated in simulations are Fermi-Dirac distribution for carrier statistics, Klaassen’s unified mobility model for dopant-dependent low-field mobility, analytical field dependent mobility for high electric field, Slotboom model for bandgap narrowing, Selberherr’s ionization rate model for impact ionization and Shockley-Read-Hall (SRH) and Klaassen Auger recombination models for minority carrier recombination lifetime. The SRH recombination lifetime for silicon is chosen to be 2.0 \mu s for a carrier concentration of 5.0 \times 10^{16} \text{ cm}^{-3} and for all other concentrations recombination lifetimes are calculated using Roulston’s equation (Roulston et al., 1982). The collector-emitter breakdown voltage, BV_{CEO}, is calculated at a collector current of 1.0 \mu A. Figures 4 and 5 show the Gummel plots and current gain curves for both LBT and CTLBT for V_{CB} = 0 \text{ V}. The simulated peak common emitter current gain of both structures is approximately 30 at a collector current of 0.1 \mu A.
3. Simulation results on breakdown voltage

3.1 Effect of collector-tub on breakdown voltage

Figure 6 shows the output characteristics of CTLBT and LBT. Clearly, due to the presence of the collector-tub, the $BV_{CEO}$ of CTLBT is significantly enhanced when compared with that of the LBT. We notice that the breakdown voltage has increased from 93 V (for LBT) to 255 V (for CTLBT) indicating an improvement of 270 percent. The reason for this significant improvement in breakdown voltage can be understood from Figure 7, which shows the electric field profile along the drift region length for every 10 V increment in collector-emitter voltage ($V_{CE}$) and at breakdown.

As expected, the collector-tub allows the electric field buildup to shift from $NN^+$-junction side to base-collector junction. Also, the applied reverse voltage is now supported by both the drift and substrate regions. This is shown by the potential contours in Figure 8 and electric field vector diagram in Figure 9, both of which show spreading of electric filed lines. The maximum breakdown voltage of CTLBT, however, is limited by the peak electric field at the collector-base junction. On the other hand, as shown in the potential contour lines and electric field vector diagram of Figures 10 and 11, the LBT structure shows crowding of electric field lines in the BOX at the collector $NN^+$-junction and breakdown of silicon film at the silicon-BOX interface.
3.2 Effect of device parameters on breakdown voltage

To study how different parameters such as substrate doping, collector-tub junction depth, drift region doping affect the breakdown voltage of CTLBT, we have varied the above parameters and estimated the collector breakdown voltage. Figure 12 shows the effect of substrate doping ($N_S$) on breakdown voltage. We notice that the breakdown voltage is maximum for an optimum substrate doping. This can be understood from Figure 13, which shows the electric field profile at various substrate dopings. At low substrate dopings, the electric field build-up takes place at the collector-base junction. The depletion volume in the substrate becomes large and the substrate leakage current limits the device breakdown. At high substrate dopings, however, the electric field builds up at the $NN^+$-junction and breakdown takes place at the substrate and collector-tub junction interface. A low substrate doping and deep collector-tub junction depth makes the electric field build-up at the drift region and the device breakdown is then limited by both the drift region length and its doping.

Figure 14 shows the effect of collector-tub junction depth ($X_j$) on the breakdown voltage and Figure 15 shows the electric field profile at different collector-emitter voltages and at different drift dopings ($N_D$). As seen from the figure, both CTLBT and LBT breakdown at
the $NN^+$-junction side at low dopings. However, the nature of breakdown is different in both structures. The CTLBT structure breaks down at low drift dopings as the drift region is entirely depleted and because the electric field at the $NN^+$-junction is high. For LBT, breakdown occurs because the electric field at the silicon-box interface is high. In this case, the electric field distribution is two-dimensional in nature. The component of the electric field at the $NN^+$ junction side depletes the lowly doped thin silicon film. When the depletion front reaches the silicon-BOX interface, the electric field increases substantially causing breakdown. The breakdown
characteristics at high drift dopings are, however, same for both the structures, which is due to high electric field at the collector-base junction end.

Figure 17 shows the effect of drift region doping on the breakdown voltage of CTLBT and LBT. Clearly, both the structures show maximum breakdown voltage for an optimum doping. However, the optimum drift doping for maximum breakdown voltage in CTLBT is smaller than that of the LBT structure. This can be explained as follows. In CTLBT, due to the presence of the collector-tub, the critical electric field at the collector-base junction determines the maximum breakdown voltage, which is limited by the drift doping. In the case of LBT, a high drift doping makes the vertical component of the electric field large, and, therefore, the lateral electrical field component becomes responsible to cause depletion in the drift region beginning from the collector-base junction end. However, once the drift region is entirely depleted, the vertical component becomes dominant and the electric field at the silicon-BOX interface determines the maximum breakdown voltage. The critical electric field for breakdown at the silicon-BOX interface is increased with the increase in the drift region doping and hence the LBT shows optimum breakdown voltage at higher doping when compared with the CTLBT structure.

Figure 18 shows the influence of the drift region length ($L_D$) on the breakdown voltage both for the LBT and CTLBT. For LBT, the breakdown voltage saturates at lower values of $L_D$.

4. Conclusions

Two-dimensional numerical simulation studies of a CTLBT structure on SOI are presented. The CTLBT has an $N$-diffusion region at the collector high-low ($NN^+$) junction. The $BV_{CEO}$ of CTLBT is about 2.7 times higher than that of the conventional LBT on SOI with identical doping profile. The increased breakdown voltage in CTLBT is explained as due to the shifting of the electric field from the collector high-low junction side to the base-collector junction side and also due to the distribution of the applied reverse potential in the substrate and drift regions. This potential redistribution, for a given BOX thickness and SOI film thickness, is found to be dependent on substrate doping ($N_S$), drift doping ($N_D$) and collector-tub junction depth ($X$). To realize the CTLBT structure in a standard CMOS process, a process flow is proposed which needs only two additional masks.

References


