A High Current Gain Horizontal Current Bipolar Transistor (HCBT) Technology for the BiCMOS Integration with FinFETs

M. Jagadesh Kumar, Susheel Nawal and Sachit Grover

Abstract — We report a new bipolar transistor structure called the SALTran HCBT with extremely large current gain not reported so far in literature. The complete process steps and the device characteristics are analyzed using two-dimensional process and device simulations. It is also shown that the proposed SALTran HCBT can be fabricated without any additional process complexity.

Keywords — Bipolar transistor, Current gain, Simulation

I. INTRODUCTION

During the last several decades, there have been several bipolar transistor innovations used in integrated circuits ranging from double diffused pn-junction isolated devices to current self-aligned, double polysilicon, deep-trench devices. Many improved methods (such as HSST [1], SICOS [2], SPOTEC [3], etc.) are commonly used to enhance the transistor performance. However, all these transistor structures are based on the vertical current concept and are not easy to integrate in a standard CMOS process. Some of the bipolar device disadvantages cannot be overcome by conventional vertical current concept since they have large volume of extrinsic regions resulting in large area consumption, low packing density and large capacitances. Lateral Bipolar Transistor (LBT) is an alternative approach to overcome some of the above problems. However, their major disadvantage is that the intrinsic base doping profile is controlled by the lateral distribution of dopants resulting in lower controllability and repeatability of the base width than in self-aligned vertical structures. Recently a horizontal current bipolar transistor (HCBT) [4], [5] was reported based on a new concept of technology. It is the smallest bipolar device for the given emitter area since the active to total device volume ratio is very high in this device. HCBT has been shown to have the following advantages [4-8]: 1) reduced surface of the device for the same emitter–base junction area; 2) no need for the n−−layer; 3) absence of epitaxial layer; 4) single polysilicon layer; 5) reduced number of lithography masks and technological steps required for fabrication, compared to [1] [3]; 6) high packing density. The HCBT structure is highly compatible with pillar like MOSFETs such as FinFETs making it an ideal device for future BiCMOS integration. In this paper, we have combined the HCBT concept [4,5] with the recently reported SALTran concept [9-15] to realize high current gain SALTran HCBTs.

We have simulated the fabrication process for the new device using SUPREM-4 [16] process simulation program. The structure generated in SUPREM4 is used as an input to the device simulation program MEDICI [17] to examine the electrical properties of the resulting SALTran HCBT structure. We demonstrate that the SALTran HCBT exhibits a significantly enhanced current gain without increasing the process complexity. The large current gain can be traded-off to improve the high-speed performance of the HCBT. High gain bipolar transistors are required in many analog applications and high speed mixed signal circuits.

II. THE CONCEPT OF SALTRAN

A surface accumulation layer is formed near the emitter–metal contact when a metal of low work function is used for the emitter contact along with a lightly doped n-type emitter as shown in Fig.1(a). The band bending at the interface causes accumulation of electrons (Fig.1(b)). The accumulated electron gradient (Fig.1(c)) at the metal–semiconductor interface is such that it results in a high electric field (Fig.1(d)) and acts as a reflecting boundary for holes injected into the emitter from the base resulting in a reduced hole concentration gradient in the emitter region. This causes a considerable reduction in the base current leading to extremely high current gains. The resulting device is known as the Surface Accumulation Layer Transistor (SALTran) [9]. The key idea behind SALTran concept is that the emitter contact metal should have a work function lower than that of the emitter and the doping of the emitter region should be sufficiently low (10^{16} /cm^2 ) for the accumulated electrons to be significant.

III. DESIGN METHODOLOGY OF SALTRAN HCBT

To obtain the device characteristics for our structure, we have used the basic design of the HCBT structure [4] on a P-type substrate. Our device is built on a SOI substrate. The emitter consists of an epitaxial layer with a peak doping variation from 7x10^{16} to 5x10^{17}/cm^3 and an emitter length of 65 nm.
The base width is 0.2 μm with a peak doping level of 10^{17}/cm^{3}. The device has a collector drift region width of (0.38 μm) with a doping of 10^{16}/cm^{3}.

4x10^{12}/cm^{2}, with the wafer rotated at an angle of 20 degrees clockwise. The base formation is shown in Fig.2(F). The masking oxide is then etched away resulting in the structure shown in Fig.2(G). To prevent the boron trapped in the oxide from entering the emitter silicon, a thin layer of oxide is deposited selectively on the SOI, Fig.2(H). Next silicon is grown using epitaxial lateral overgrowth with a phosphorus doping of 7x10^{19}/cm^{3}, Fig.2(I). The wafer is then tilted anticlockwise by 35 degrees and phosphorus implantation is done to increase the n-doping in the region near the collector terminal, Fig.2(J). Now, a 0.4 μm layer of silicon is etched anisotropically to obtain the desired height of the epitaxial layers for the emitter and collector windows, Fig.2(K). This completes the basic transistor structure. After the removal of the nitride-oxide cap layer, Fig.2(L), a thick layer of CVD oxide is deposited, Fig.2(M). All the dopants are activated and the implantation damage is recovered by a single rapid thermal annealing (RTA). Then the contact windows are opened and metal is deposited to form the transistor terminals, Fig.2(N).

**IV. SIMULATION RESULTS AND DISCUSSION**

The device structure as obtained from the above SUPREM4 [16] simulation was imported to MEDIT[17] and the device simulation was carried out using a concentration dependent mobility model together with parallel field dependent mobility model. Band gap narrowing at high doping levels was taken into account. Shockley-Read-Hall recombination with concentration dependent lifetimes and Auger recombination models were also included. A detailed description of the physical models and the respective numerical methods are explained in detail in [9]. For the conventional HCBT, the emitter doping is 5x10^{18}/cm^{3}. For the SALTran HCBT, the emitter doping is 7x10^{16}/cm^{3}. For both the transistors, the emitter contact is made with a metal, such as Titanium, whose work functions is 3.9 eV which is less than that of the emitter silicon region. Our simulation results have shown that the electric field in the emitter region of SLATran HCBT is significant due to the accumulation of electrons, and therefore results in a reflecting boundary for the holes arriving from the base into the emitter region. The Gummel plot is shown in Fig. 3 which clearly shows that due to the presence of the reflecting boundary the base current of SALTran HCBT is significantly smaller than that of the conventional HCBT resulting in a significant enhancement in the current gain of the SALTran HCBT as shown in Fig. 4. While the conventional HCBT has a peak current gain of only 90, the SALTran HCBT exhibits a peak current gain of 4000. This significant enhancement in the current gain is achieved without complicating the fabrication process of the conventional HCBT.
Fig. 2 Fabrication steps of SLATran HCBT

Fig. 3 Comparison of Gummel plots.

Fig. 4 Comparison of current gain.

V. CONCLUSIONS

For the first time we have reported a complete fabrication process for the horizontal current bipolar transistor (HCBT) with significantly enhanced current gain which can be traded
off for further improving the performance of the HCBT. Since HCBT is a pillar like structure, it is highly compatible for integration with other pillar like MOSFET structures, such as FinFETs. With this enhanced current gain, the SALTran HCBT will be even more attractive for analog and mixed signal applications in BiCMOS technology.

REFERENCES


