Investigation of a new modified source/drain for diminished self-heating effects in nanoscale MOSFETs using computer simulation

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Abstract

In this paper, we demonstrate that by introducing a buried oxide in a bulk MOSFET only under the source and drain regions, i.e., using an oxygen implanted source/drain (OISD) structure, the drain capacitance of a nanoscale MOSFET can be made close to that of a silicon-on-insulator SOI MOSFET while the self-heating effects are highly diminished and are similar to that of a bulk MOSFET. Two-dimensional simulation is used to optimize the length and thickness of the OISD regions.

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1. Introduction

Silicon-on-insulator (SOI) MOSFETs have many advantages for high-performance and low-voltage applications in the sub-half-micron regime since they offer a steeper subthreshold swing, reduced parasitic capacitance and elimination of latch up [1]. However, self-heating is a major problem in SOI MOSFETs as compared to the bulk MOSFETs due to the decreased heat flow across the buried oxide. The temperature rise causes a decrease in the drain current and leads to more serious reliability problems such as increased electromigration and enhanced impact ionization. In the past, several attempts have been made to reduce the temperature rise stemming from this self-heating [2,3].

In this paper, we examine an alternative measure to reduce the self-heating effects by introducing a buried oxide in a bulk MOSFET only under the source and drain regions which can be easily created with implantation of oxygen molecules under source/drain regions. Using two-dimensional simulation [4], we demonstrate that introducing optimized oxygen implanted source and drain (OISD)
regions in a bulk MOSFET, we can achieve low junction capacitances comparable to that of an SOI MOSFET while the self-heating effects are significantly reduced.

2. Simulation method and device parameters

There is a lattice temperature advanced application module (LT-AAM) in MEDICI simulator [4]. Therefore, it is possible to couple the electrical and thermal characteristics of devices for their accurate modeling. In this case, a new state variable, “the temperature of the lattice”, is

![Diagram](image_url)

Fig. 2. 3-D temperature distribution of (a) OISD, (b) bulk and (c) SOI MOSFETs.
introduced into MEDICI in order to describe the self-heating of devices. Poisson’s equation, the current continuity equation, and the heat equation are solved in a completely coupled manner to obtain the temperature of the lattice.

A schematic cross-sectional view of the OISD MOSFET implemented using the 2-D device simulator MEDICI is shown in Fig. 1 where \(t_{OISD}\) and \(L_{OISD}\) are the thickness of OISD region and the distance between the two OISD regions, respectively. The simulation parameters of the structure are given in Table 1. We have compared this OISD structure with that SOI and bulk MOSFETs with equivalent parameters.

3. Results and discussions

Fig. 2 shows a typical MEDICI simulated 3-D temperature distribution in the OISD, SOI and bulk MOSFETs for \(V_{GS} = 1\) V and \(V_{DS} = 1.5\) V. The temperature in the substrate is fixed at 300 K. As can be seen from Fig. 2(a), the maximum temperature in the OISD structure (\(\approx 320\) K) is very close to that of the peak temperature in the bulk MOSFET (\(\approx 310\) K) as shown in Fig. 2(b) and is significantly smaller than the peak temperature (\(\approx 510\) K) shown in Fig. 2(c) for the SOI MOSFET. The reduced self-heating effect is also clearly reflected in the output characteristics shown in Fig. 3 in which the drain current of the OISD structure is close to that of the bulk MOSFET.

For optimizing the length and thickness of the OISD regions, we have carried out a comparison in terms of zero-bias drain capacitance and maximum device temperature as shown in Fig. 4. It can be observed clearly that when the distance between OISD regions \(L_{OISD}\) decreases, the maximum temperature of the device will increase. However, the zero-bias drain capacitance of the device is very weakly dependent on the distance between the OISD regions up to 90 nm and exhibits only about 5% variation. Therefore, in the OISD MOSFETs, by keeping the distance between the OISD regions \(L_{OISD}\) almost equal to that of the channel length, the temperature of the device can be kept close to that of the bulk MOSFET, while the drain current of the OISD MOSFET is close to that of the bulk MOSFET.
capacitance is close to that of the SOI MOSFET. However, if the distance between the OISD regions \( L_{\text{OISD}} \) is below the channel length (100 nm), the zero-bias drain capacitance abruptly increases. This can be understood from Fig. 5. Our simulation shows that when \( L_{\text{OISD}} \) is less than the channel length, the zero-bias depletion region is as shown schematically in Fig. 5(a). However, if \( L_{\text{OISD}} \) exceeds the channel length, the zero-bias depletion region forms over an extended length as shown schematically in Fig. 5(b) increasing the zero-bias drain capacitance. Fig. 6 shows the dependence of the maximum temperature and zero drain-bias capacitance on the thickness \( t_{\text{OISD}} \) of the OISD regions. The distance between OISD regions is set equal to the channel length at 100 nm. We can observe that the maximum device temperature is weakly dependent on the thickness of the OISD regions because heat removal takes place through the gap between the OISD regions. The drain capacitance is also weakly dependent on the thickness of the OISD regions if the thickness is more than 50 nm. However, if the thickness of the OISD regions \( t_{\text{OISD}} \) is smaller than 50 nm, the zero-bias drain capacitance increases abruptly. This can be understood from Fig. 7 in which, based on our simulation results, the formation of the depletion for two different \( t_{\text{OISD}} \) cases are schematically shown. If the thickness of the OISD-regions \( t_{\text{OISD}} \) is less than the zero-bias source/drain depletion region thickness (Fig. 7(a)), the length over which the depletion region forms is more than the case when the thickness of the OISD-regions \( t_{\text{OISD}} \) is greater than the zero-bias source/drain depletion region thickness (Fig. 7(b)). This clearly shows the reason why the drain capacitance increases when \( t_{\text{OISD}} \) is smaller than 50 nm.

The importance of the standby current or leakage current as a factor to be included in the performance figure of merit for deep submicron CMOS has recently been proposed and analyzed for bulk CMOS technology [5,6]. Therefore, the transfer characteristic of OISD structure is shown in Fig. 8. It can be seen from the figure that the leakage current of OISD device reduces when compared to the bulk MOSFET due to the junction area reduction. Also, the subthreshold slope of the device improves. Fig. 9 shows the threshold voltage of OISD, SOI, and bulk MOSFET structures versus the channel
length up to 50 nm. It is clear that the variation of threshold voltage for the OISD structure is similar or slightly better when compared to the bulk MOSFET.

4. Conclusions

In this paper, using two-dimensional simulation, we have demonstrated that by introducing an oxide region just under the source and drain of a MOSFET, one can realize self-heating effects close to that of a bulk MOSFET while the drain capacitance is similar to that of an SOI MOSFET. We have also shown that even if there are variations in the distance between the OISD regions or their thickness, it will not critically affect the projected benefits. In conclusion, we can design the OISD structure for best performance by choosing the distance between the OISD regions about the channel length, and the thickness of OISD regions greater than the difference between width of depletion region under the gate and the thickness of n+ source/drain regions.

References