Briefs

Study of the Extended p^+ Dual Source Structure for Eliminating Bipolar Induced Breakdown in Submicron SOI MOSFET's

Vikram Verma and M. Jagadesh Kumar

***Abstract*—Simulation results on a novel extended p^+ dual source SOI MOSFET are reported. It is shown that the presence of the extended p^+ region on the source side, which can be fabricated using the post-low-energy implanting selective epitaxy (PLISE), significantly suppresses the parasitic bipolar transistor action resulting in a large improvement in the breakdown voltage. Our results show that when the length of the extended p^+ region is half the channel length, the improvement in breakdown voltage is about 120% when compared to the conventional SOI MOSFET's.**

***Index Terms*—Floating body effect, parasitic bipolar transistor, SOI MOSFET's.**

I. Introduction

In silicon-on insulator (SOI) devices, the floating body effect causes the lowering of drain breakdown voltage due to the parasitic bipolar transistor inherently present in the structure. Several methods have been proposed to reduce the floating body effect [1], [2]. Ploeg *et al.* [3] proposed a dual source structure(DSFET) and showed that by placing a p^+ region underneath the n^+ source and using the aluminum spiking to electrically connect the two can effectively increase the breakdown voltage. However, as pointed out in [3], the spiking is susceptible to process variations and is also incompatible with modern VLSI technologies such as silicidation.

In this work, we propose a novel dual source structure in which the buried p^+ region under the n^+ source is laterally extended into the body of a partially depleted SOI MOSFET. Using numerical simulation, we show that this results in a significant improvement in the drain breakdown voltage without any need for the body contact through the metal spiking. We further demonstrate that the drain breakdown voltage is maximum if the length of the extended p^+ region is approximately half the channel length.

II. Device Structure with Extended P^+ Region

Fig. 1 shows the cross-section of the extended p^+ dual source SOI MOSFET (Ep^+ DSFET) considered in this study. This structure is similar to that of the DSFET[3] but with the buried p^+ region extended laterally into the body. However unlike in [3], we have assumed no aluminum spiking in our proposed structure. The device is simulated with a gate oxide thickness of 20 nm and back oxide thickness of 400 nm. The n^+ doping of the source and drain are both fixed at $5 \times 10^{19}/\text{cm}^3$. The channel has a uniform p-doping of $6 \times 10^{16}/\text{cm}^3$. The channel length is 0.5 μm and the silicon film thickness is 200 nm thus making it a partially depleted device. The above structure can be fabricated, for example, using the post-low-energy implanting selective epitaxy(PLISE)[4]. This technology has been shown to give extremely steep channel profiles in delta-doped NMOSFET's which we have verified for the proposed structure using TSUPREM4 [5]. All the simulations in this work are performed using MEDICI [6].

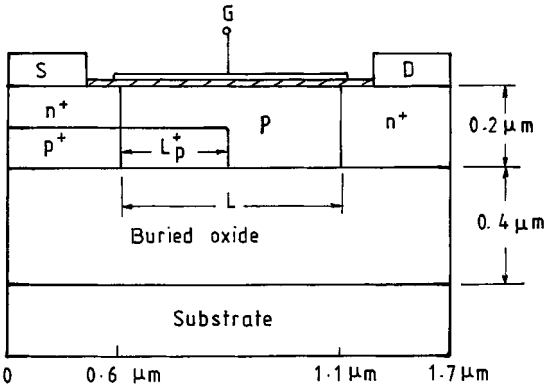

Fig. 1. Cross section of the extended p^+ dual source SOI MOSFET where L is the channel length and Lp^+ is the p^+ region extended into the channel (Not drawn to scale).

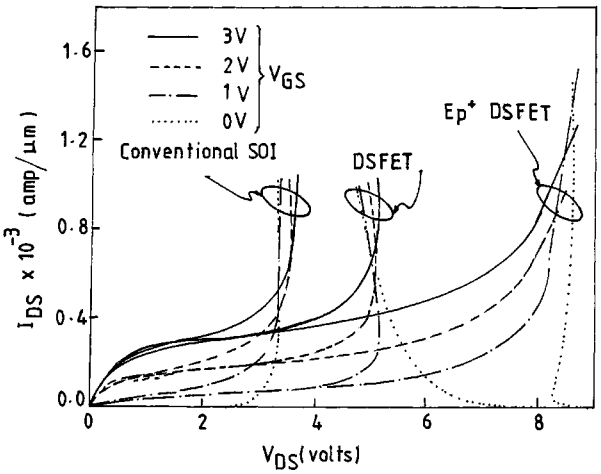

Fig. 2. Simulated $I_{DS} - V_{DS}$ characteristics of conventional SOI MOSFET, DSFET and Ep^+DSFET.

III. Effect of the Extended p^+ Region on the Drain Characteristics

In Fig. 2, the simulated drain characteristics of the Ep^+DSFET are compared with the drain characteristics of the DSFET and the conventional SOI MOSFET. Clearly, the drain breakdown voltage (defined as the drain voltage at $I_{DS} = 10^{-3}$A/μm for $V_{GS} = 0$ V) of Ep^+DSFET is much larger compared to the other two structures. In the case of a conventional SOI MOSFET, the holes generated by impact ionization near the drain junction forward bias the source-body (n^+p) junction which results in electrons being injected into the body and finally being collected by the drain. This added drain current augments the impact ionization, which in turn increases the source-body forward levels at the n^+p source-body junction [5] bias, thereby causing a regenerative action. The buried p^+ region in the case of a DSFET [3], being

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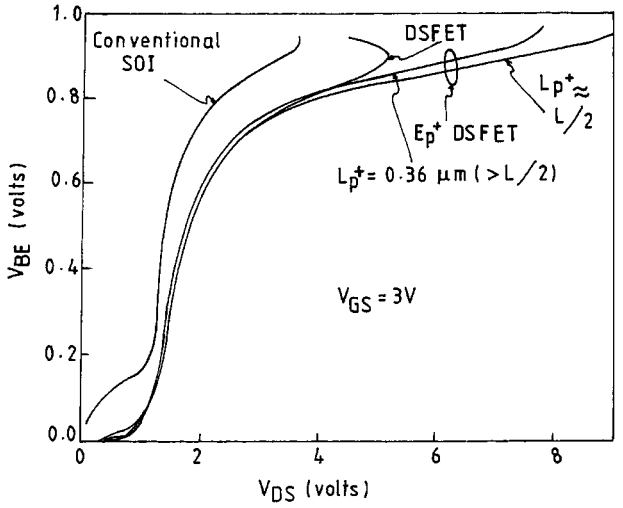

Fig. 3. Forward bias V_{BE} of the source-body junction versus the drain voltage V_{DS}.

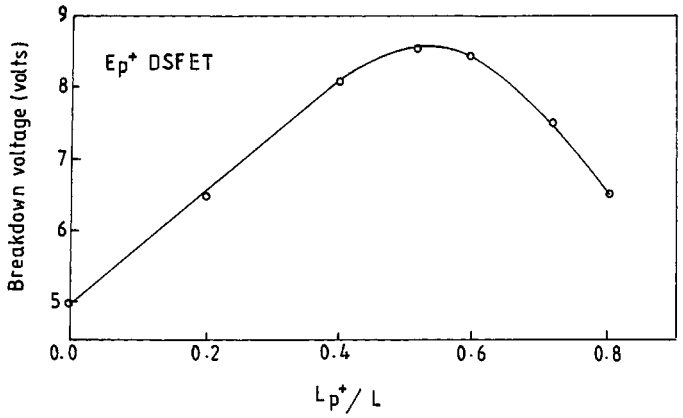

Fig. 4. Breakdown voltage versus $L_{\rm P}{}^{+}/L$ for the Ep^{+}DSFET with channel length $L = 0.5$ μm.

at a lower potential than the n^{+} source, collects the generated holes thereby lowering the forward bias of the source-body junction. This reduces the number of electrons in the drain depletion region available for avalanche multiplication and results in an increased breakdown voltage. If the buried p^{+} region is extended laterally into the body, the efficiency of the p^{+} region to attract the holes increases significantly reducing the number of holes that reach the n^{+} source facing the active channel region. This results in a reduced forward bias and, consequently, even higher breakdown voltage. The forward bias (V_{BE} of the parasitic npn transistor) calculated from the separation between the quasifermi levels at the n^{+}p source-body junction [7] is plotted in Fig. 3 for the three cases considered in Fig. 2. Clearly, V_{BE} is significantly large both for the conventional SOI MOSFET and the DSFET indicating that their breakdown voltage will be smaller than that of the Ep^{+}DSFET. For the Ep^{+}DSFET structure, the V_{BE} values are at their minimum when the length of the extended p^{+} region is approximately half the channel length ($L_{\rm P}{}^{+} \approx L/2$). It can further be observed that even in the case of Ep^{+}DSFET, for $L_{\rm P}{}^{+} > L/2$, V_{BE} increases considerably as the drain voltage is increased. This implies that it should be possible to minimize the source-body forward bias for maximum breakdown voltage by adjusting the length $L_{\rm P}{}^{+}$ of the extended p^{+} region.

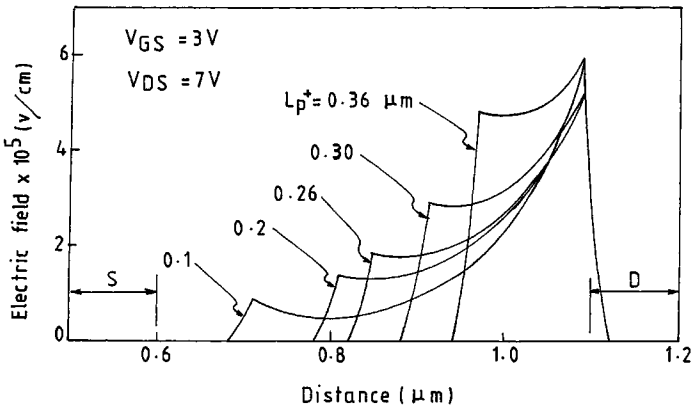

Fig. 5. Electric field along the x-axis in the body at a depth of 0.14 μm from the Si/SiO$_2$ interface for different values of $L_{\rm P}{}^{+}$.

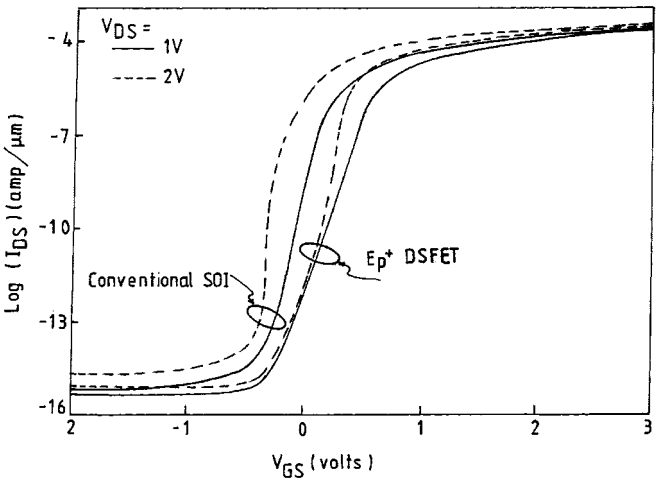

Fig. 6. Simulated $I_{DS} - V_{GS}$ characteristics of conventional SOI MOSFET, DSFET and Ep^{+}DSFET.

IV. Optimum Length of the Buried P^{+} Region for Maximum Breakdown Voltage

Fig. 4 shows the breakdown voltage for the Ep^{+}DSFET for different values of p^{+} extensions. There is an increase in breakdown voltage as the length of the buried p^{+} region is increased until $L_{\rm P}{}^{+} \approx L/2$. However when $L_{\rm P}{}^{+}$ exceeds $L/2$, the breakdown voltage decreases. This is because as the p^{+} region gets close to the drain nearly all the drain voltage is dropped between the n^{+} drain and the p^{+} extension and consequently the electric field becomes high (Fig. 5) resulting in a large multiplication of charge carriers. The fact that the breakdown voltage does not increase beyond $L_{\rm P}{}^{+} \approx L/2$ is not restricted to this case only. We have examined the effect of $L_{\rm P}{}^{+}$ by simulating the breakdown voltage of Ep^{+}DSFET structure for different channel lengths and channel dopings. Our simulations show that in both the cases, the breakdown voltage of Ep^{+}DSFET is larger than that of DSFET and the conventional SOI MOSFET. The drain current I_{DS} vs. gate voltage V_{GS} plot shown in Fig. 6 demonstrates that band-to-band tunneling at the source side n^{+}/p^{+} junction does not lead to a higher leakage current and therefore will not degrade the subthreshold slope in the proposed structure.

V. Conclusions

It is shown that placing a p^{+} region underneath the n^{+} source and extending it laterally into the channel significantly increases the break-

down voltage of SOI MOSFET's. This improvement is due to the effective suppression of parasitic bipolar action by the extended p^+ region. We have further shown that the increase in breakdown voltage is maximum when the length of the extended p^+ region is approximately half the channel length ($L_{p^+} \approx L/2$).

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A Transient SPICE Model for Digitally Modulated RF Characteristics of Ion-Implanted GaAs MESFET's

Mikhail S. Shirokov, Robert E. Leoni, III, Jianwen Bao, and James C. M. Hwang

***Abstract*—A transient SPICE model, which was previously developed for epitaxial GaAs MESFET's, was modified for ion-implanted GaAs MESFET's. The model accounts for both trapping and detrapping effects hence can simulate both low-frequency dispersion and gate-lag characteristics. The model was experimentally verified in terms of pulsed current–voltage (*I–V*) characteristics and digitally-modulated RF carrier waveforms.**

***Index Terms*—Charge carrier processes, digital communication, MESFET's, modeling, pulse measurements, signal analysis, SPICE, transient analysis.**

The transient response of a GaAs MESFET's isothermal characteristics is mainly determined by surface and substrate traps. The traps can cause drain lag and gate lag [1] in addition to low-frequency dispersion [2]. Many MESFET models [3] can account for low-frequency dispersion but not drain or gate lag. It was only recently that transient MESFET models were developed for both low-frequency dispersion and drain lag [4] or gate lag [5]. The model we reported in [5] was mainly for epitaxial MESFET's under the influence of surface traps. This model has been modified for ion-implanted MESFET's and substrate traps as will be described in the following.

The present model was developed for ion-implanted MESFET's having a gate length and width of 0.5 and 200 μm, respectively. The threshold voltage is -2 V. The saturated and maximum drain currents are 200 and 300 mA/mm. The MESFET's were found to exhibit gate lag due to substrate traps [6].

When occupied, substrate traps can cause the threshold voltage to shift. This can be seen in the dynamic transfer characteristics obtained by pulsing the MESFET from two different off-state gate-source voltages (V_{GS}^{OFF}), as shown in Fig. 1. Since a threshold voltage shift is

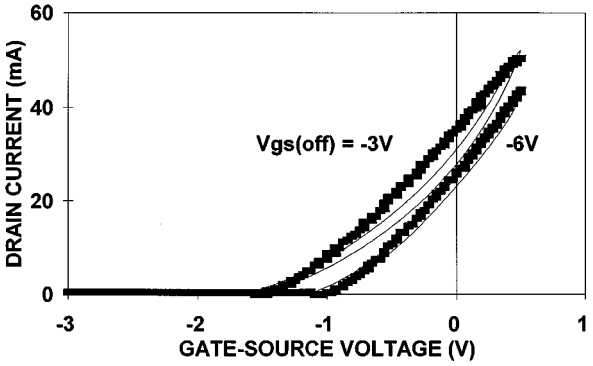

Fig. 1. Dynamic transfer characteristics, under a CW sinusoidal signal of 100 KHz and 3.5 V (peak to peak), measured approximately 1 μs after the gate-source bias voltage was pulsed from either -3 to -1.25 or from -6 to -1.25 V. Shift in threshold voltage between the two cases indicates different amounts of trapped charges under different off-state gate-source voltages. (■) measured. (—) simulated.

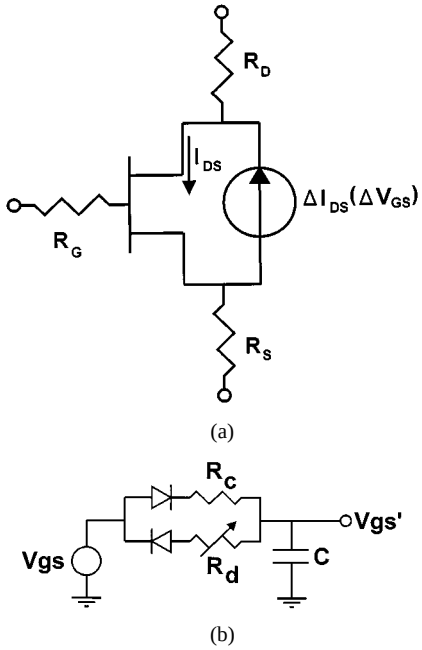

Fig. 2. Circuit model implemented in SPICE. (a) Parasitic current source ΔI_{DS} is modeled as another MESFET and is used to mimic the threshold voltage shift. (b) Nonlinear RC timing circuit is used to drive the parasitic current source. The voltage dependence of the detrapping time constant τ_D (V_{GS}, V_{DS}) is modeled by using a variable resistor.

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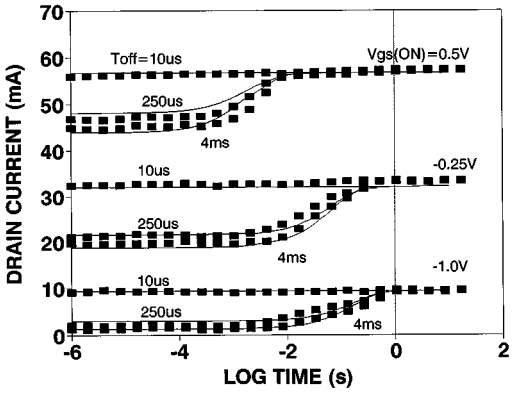
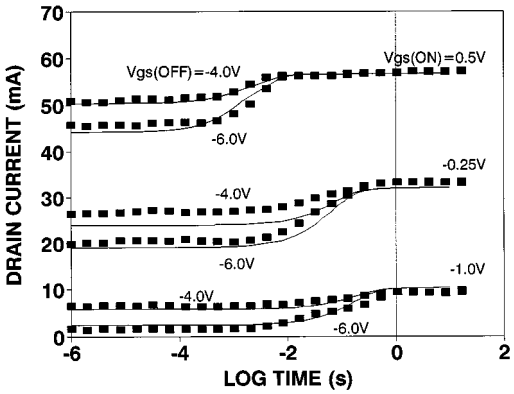


(a)



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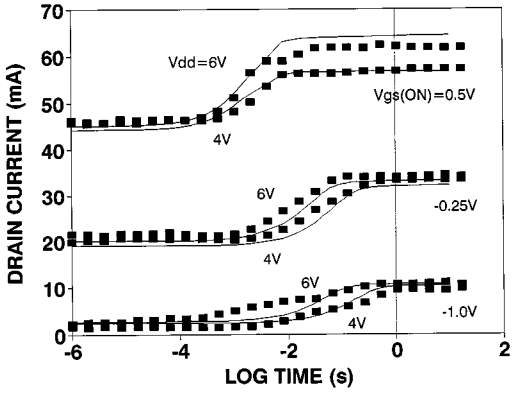

(c)

Fig. 3. (■) Measured and (—) simulated drain current transients showing their dependencies on on-state gate-source voltage as well as (a) off time, (b) off-state gate- source voltage, and (c) drain supply. When not varied, off time $=$ 1 ms; off-state gate-source voltage $=$ -6 V; drain supply $=$ 4 V.

difficult to implement in SPICE its effects on the instantaneous drain-source current (i_{DS}) is considered instead. The difference between the steady-state and transient drain-source currents, ΔI_{DS}, was found to depend mainly on the drain-source voltage (V_{DS}) as well as the difference between on- and off-state gate-source voltages ($V_{GS} - V_{GS}^{OFF}$). In fact, ΔI_{DS} (V_{DS}, $V_{GS} - V_{GS}^{OFF}$) and the steady-state drain-source current I_{DS} (V_{DS}, V_{GS}) have very similar functional forms.

Unlike epitaxial MESFET's, the present implanted MESFET requires only one set of trapping and detrapping time constants (τ_C and τ_D). Further, while τ_C is approximately constant over a wide range of on/off and gate/drain voltages, τ_D has strong exponential dependence on on-state gate-source and drain-source voltages, possibly due to impact ionization or field-induced barrier lowering. Based on these observations, [5, Eq. (1)] was reduced to

$$i_{DS} = I_{DS}(V_{DS}, V_{GS}) - \Delta I_{DS}(V_{DS}, V_{GS} - V_{GS}^{OFF}) \cdot \left(1 - e^{-(t_{OFF}/\tau_C)}\right) \cdot e^{-(t/\tau_D(V_{GS}, V_{DS}))} \quad (1)$$

where

I_{DS} steady-state drain-source current;
t_{OFF} time the MESFET is off;
t time the MESFET is turned back on.

Using *SPICE*, a voltage-dependent current source may be used to model ΔI_{DS} similarly to [5]. However, since the drain-gate access resistance remains approximately constant in the present case, the parasitic linear MESFET is no longer needed [Fig. 2(a)]. The parasitic current source ΔI_{DS} is modeled as another MESFET. Time-dependent control of the current source is provided by a nonlinear RC subcircuit with the detrapping time constant modeled by a voltage dependent resistor [Fig. 2(b)]. With unity capacitance, $R_C = \tau_C$ and $R_D = \tau_D = \tau_0 \exp -(\gamma V_{GS} + \delta V_{DS})$, where τ_0, γ, and δ are fitting constants. In the present case, $\tau_C = 1$ ms; $\tau_0 = 0.43$ s; $\gamma = 1.87$/V; $\delta = 0.71$/V. The subcircuit is driven by instantaneous V_{GS}. The instantaneous voltage across the capacitor is then used to control the parasitic current source ΔI_{DS}. The intrinsic MESFET is simulated by a conventional model using the steady-state drain characteristics I_{DS}.

For model verification, pulsed current–voltage (*I–V*) characteristics after various combinations of bias voltages and times were simulated (Fig. 3). To further verify the model, a MESFET is pulsed from off ($V_{GS}^{OFF} = -3$ or -6 V) to on ($V_{GS} = -1.25$ V) while a CW sinusoidal signal of 10 KHz and 3.5 V (peak to peak) is superimposed on the pulse (Fig. 1). In all cases, the simulated results compare well with the measured data.

In summary, a transient *SPICE* model, which was previously developed for epitaxial GaAs MESFET's, was successfully adapted for ion-implanted GaAs MESFET's. This illiterates the robustness of the model in simulating transients due to both surface and substrate traps.

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Forward Gated-Diode Measurement of Filled Traps in High-Field Stressed Thin Oxides

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***Abstract*—The forward gated-diode monitoring technique can find its potential applications in assessing the filled traps in MOSFET thin oxides, which are subjected to high-field stressing and then followed by hot-electrons filling scheme. Our measurement of the gate voltage shift associated with the forward current peak produces a power law relation between the filled trap density and the electron stress fluence, indeed in close agreement with that obtained by MOSFET threshold voltage shift.**

***Index Terms*—Gated-diode, hot electron, MOSFET, neutral trap, oxide breakdown, SILC, thin oxide.**

I. Introduction

The high-field Fowler–Nordheim (FN) electron tunneling through thin oxides can produce a variety of defects, among which the most concerned are the neutral electron traps. The principal reasons are that 1) the neutral electron traps can serve as a stepping stone for injected electrons, which gives rise to SILC in low voltage regime [1],[2], and 2) a certain trap density is critically encountered, leading to a breakdown event [3]–[6]. Thus, an essential knowledge of the total neutral trap density N_T created for imposed electron fluence Q_e is crucial to the study of SILC and oxide breakdown. To achieve this goal, Degraeve *et al.* [7], [8] have recently performed two independent experiments while introducing a key physical parameter, namely, filling or occupied fraction p [9], to connect the two. The first experiment is the hot-electrons filling scheme following the high-field stress. This scheme via a back-gate reverse bias can offer hot substrate electrons to climb over the Si/SiO_2 barrier height and fill the neutral traps within the oxide. Measurement of a saturation level in threshold voltage shift can be directly linked to the filled trap density N_{ox}, systematically leading to a power law relation [7], [8]: $N_{ox} \propto Q_e^{0.56\sim0.6}$. The second is the sphere-based Monte Carlo percolation simulation experiment treating N_T as well as its statistics. p is N_{ox} divided by N_T [9] and can be estimated by subsequently fitting intrinsic charge-to-breakdown data in the manufacturing processes [7], [8], [10], [11].

On the other hand, for MOSFET's biased in a reverse gated-diode mode [12], measurement of the reverse current I_r versus gate voltage from accumulation through depletion to inversion can provide information concerning interface states and/or oxide traps. This mode is usually insensitive to oxides having small areas as in miniaturized devices, and the large-area oxides are inevitably required. The same information can be substantially maintained for switching to the forward mode as reflected by a well-defined relation $I_f = I_r \exp(qV_f/2KT)$ [12], where I_f is the forward current measured at a forward bias V_f. Thus, operating in forward mode can not only make the gated-diode monitoring exponentially sensitive but also allow use of small-area oxides. Indeed, the forward gated-diode configuration formed on the stressed MOSFET's has exhibited these abilities [13]–[15]. This work is to extend such sensitive technique to the case of thin oxides that are subjected to FN tunneling stress and then followed by hot-electrons filling scheme. The ultimate objective is to build a power law relation between N_{ox} and Q_e as that in [7], [8].

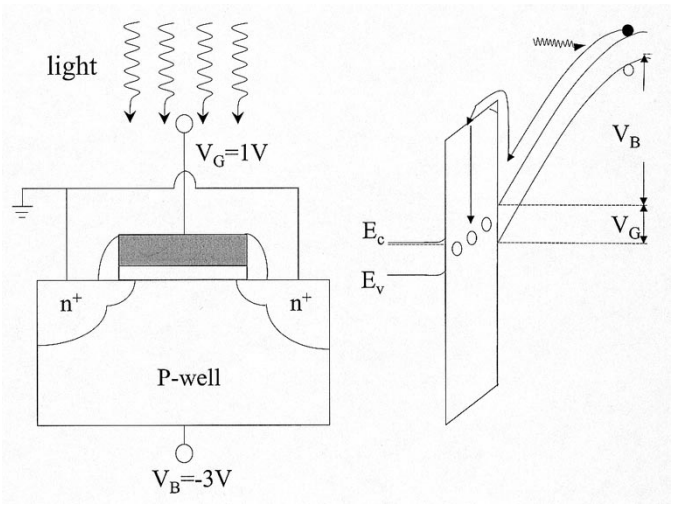

Fig. 1. Experimental setup and energy band diagram to schematically demonstrate the optically induced hot-electrons filling scheme.

II. Experimental

The n-channel MOSFET's under study had the gate width-to-length ratio of 20 μm/ 0.3 μm and the gate oxide thickness of 7 nm. The FN tunneling stress condition was carried out at the oxide field strength E_{ox} of 9.9 MV/cm with the source, drain, and substrate tied to ground, then followed by the optically induced hot- electrons filling scheme [16]. Fig. 1 shows schematically this scheme in terms of 1) the photogeneration technique via a tungsten lamp to produce electron seed in substrate, and 2) a negative back-gate bias of -3 V to make substrate electrons hot such as to surmount the Si/SiO_2 barrier height and fill the traps. During measuring the gated-diode forward current in the drain, the drain was connected to -0.2 V bias, the substrate was tied to ground, and the source was kept open.

Fig. 2 plots the measured forward current versus gate voltage for $Q_e = 0.22$ C/cm^2 with filling or illumination time as parameter. It can be observed that the current peak in depletion region shifts toward the positive gate voltage for increasing illumination time and gradually tends to saturate. Fig. 3 shows the corresponding voltage shift ΔV_G associated with the current peak versus illumination time. Detrapping and Coulombic repulsion [9], which limit only part of the neutral traps available for filling, are responsible for the saturating behavior in Fig. 3. Assuming that the occupied traps are distributed uniformly within the oxide as adopted elsewhere [7], [8], [16], the saturated voltage shift $\Delta V_{G(sat)}$ can be directly linked to the filled trap density through $\Delta V_{G(sat)} = qt_{ox}^2 N_{ox}/2\varepsilon_{ox}$ where t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity. The resulting N_{ox} for different Q_e is depicted in the inset of Fig. 3, showing a power law relation

$$N_{ox} = \eta Q_e^{0.5} \tag{1}$$

where $\eta = 1.62 \times 10^{18}$ cm$^{-2}C^{-0.5}$ for N_{ox} in 1/cm^3 and Q_e in C/cm^2. The carrier separation technique has measured the substrate hole current, yielding hole generation coefficient of 6.8×10^{-4} at the same stress field E_{ox} of 9.9 MV/cm. Thus, we have $N_{ox} = 6.21 \times$

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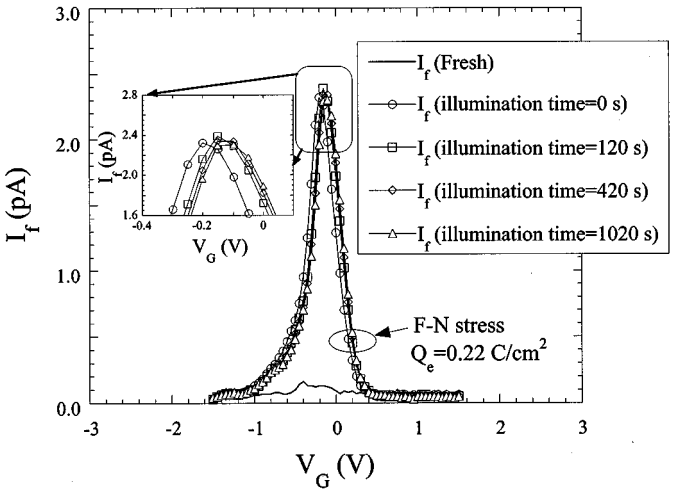

Fig. 2. Measured forward gated-diode current versus gate voltage from one n-MOSFET sample. The gate oxide area was 3 μm^2. For the selected illumination time following Q_e of 0.22 C/cm^2, the filling scheme was interrupted and the test setup was switched to the forward gated-diode configuration. The *I–V* near the current peak is magnified for clear viewing.

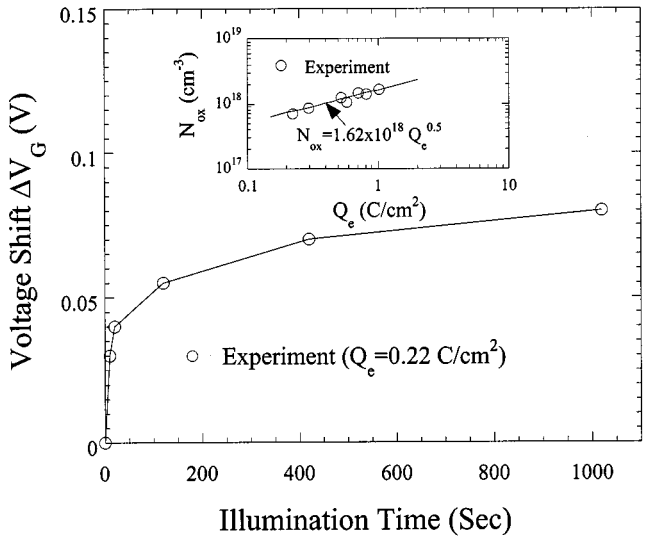

Fig. 3. Gate voltage shift versus illumination time corresponding to Fig. 2. The inset shows the estimated trap density N_{ox} versus Q_e from seven n-MOSFET samples. Each sample represents a specific Q_e. A power law relation is drawn by best fitting data points.

$10^{19}Q_p^{0.5}$ for hole fluence Q_p in C/cm^2, which is quite close to the published expression $N_{ox} = 5.3 \times 10^{19}Q_p^{0.56}$ [7], [8] with respect to the power exponent and the prefactor.

The above hot-electrons filling scheme has also been performed on the fresh devices, evidencing no noticeable voltage shift in the measured forward current versus gate voltage before and after the scheme. This means that no extra neutral traps can be generated *singly* due to filling action. Additionally, Fig. 2 clearly reveals that the current peaks for different illumination times following FN stress (including the zero illumination time) are almost unchanged, indicating that no significant interface states can be created under the influence of the illumination induced hot electrons.

III. Conclusion

The forward gated-diode technique has demonstrated its new merit of producing a power law relation between the filled trap density and the electron stress fluence. This relationship is found to agree closely with that obtained by MOSFET threshold voltage shift.

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