1. Half adders generate $P_i, G_i$  

2. CLA (1st layer) $\rightarrow$ $P_I, G_I$  

3. CLA (2nd layer) $\rightarrow$ $C_0, C_4, C_8, C_{12}$  

4. CLA (1st layer) $\rightarrow$ $C_1, C_2, C_3$ etc.  

5. Layer of half adders $\rightarrow$ $S_i$  

$$C_4 = G_I + P_I C_0$$  

$$C_5 = G_4 + P_4 C_4$$
\[ C_4 = G_1 I + P_1 C_0 \]
\[ C_8 = G_{II} + P_{II} G_I + P_{II} P_1 C_0 \]
\[ C_{12} = G_{III} + P_{III} G_{II} + P_{III} P_{II} G_I + P_{III} P_{II} P_1 C_0 \]
\[ C_{16} = G_{IV} + P_{IV} G_{III} + P_{IV} P_{III} G_{II} + P_{IV} P_{III} P_{II} G_I + P_{IV} P_{III} P_{II} P_1 C_0 \]
\[ C_{16} = G_{1}^{2} + P_{1}^{2} C_{0} \]

\[ C_{32} = G_{2}^{2} + P_{2}^{2} G_{1}^{2} + P_{2}^{2} P_{1}^{2} C_{0} \]

\[ C_{48} = G_{3}^{2} + P_{3}^{2} G_{2}^{2} + P_{3}^{2} P_{2}^{2} G_{1}^{2} + P_{3}^{2} P_{2}^{2} P_{1}^{2} C_{0} \]

Shouri Chatterjee
July-December 2009

Department of Electrical Engineering,
Indian Institute of Technology, Delhi,
Hauz Khas, New Delhi 110016
1. Layer of half adders → $P_i, G_i$  
2. Layer 1 of CLA (16x) → $P_i, G_i$  
3. Layer 2 of CLA (4x) → $P_i, G_i$  
4. Layer 3 of CLA (C0) → $C_{16, 32, 48}$  
5. Layer 2 of CLA → $C_{4, 8, 12}$  
6. Layer 1 of CLA → all other carries → $C_{20, 24, 28}$  
7. Half adders → $S_i$
Multiplexers

2:1 MUX

\[ \text{Output} = \begin{cases} \overline{S} & \text{if } S, \quad \text{Output} = A_0 \\ S & \text{if } \overline{S}, \quad \text{Output} = A_1 \end{cases} \]

\[ \text{Output} = A_1 S + A_0 \overline{S} \]

4:1 MUX

\[ \text{Output} = \overline{S_1 S_0} A_0 + \overline{S_1 S_0} A_1 + S_1 \overline{S_0} A_2 + S_1 S_0 A_3 \]
EEL201: Digital Electronic Circuits

Shouri Chatterjee
July-December 2009

Department of Electrical Engineering,
Indian Institute of Technology, Delhi,
Hauz Khas, New Delhi 110016

\[ f = \sum 0, 1, 5, 6, 7 \]