Error correction

Out of 7 bits, 3 code bits, 4 message bits

Out of 15 bits, 4 code bits, 11 message bits

Hamming

\[ D_1 = \text{XOR}(D_3, D_5, D_7) \]
\[ D_2 = \text{XOR}(D_3, D_6, D_7) \]
\[ D_4 = \text{XOR}(D_5, D_6, D_7) \]

\[ D_4, D_2, D_1 \]

1 → 0 0 1 1
2 → 0 1 0 0
3 → 0 1 1 0
4 → 1 0 0 0
5 → 1 0 1 0
6 → 1 0 1 1
7 → 1 1 1 1
\[ E_1 = \text{XOR}(R_1, R_3, R_5, R_7) \]
\[ E_2 = \text{XOR}(R_2, R_3, R_6, R_7) \]
\[ E_4 = \text{XOR}(R_4, R_5, R_6, R_7) \]

\[
\begin{array}{cccccc}
0 & 1 & 1 & 0 & 0 & 0 \\
R_1 & R_2 & R_3 & R_4 & R_5 & R_7 \\
\end{array}
\]

\[ E_1 = \text{XOR}(0, 1, 0, 1) = 0 \]
\[ E_2 = \text{XOR}(1, 1, 0, 1) = 1 \]
\[ E_4 = \text{XOR}(0, 0, 0, 1) = 1 \]
\[ D_1 = \text{XOR}(D_3, D_5, D_7, D_9, D_{11}, D_{13}, D_{15}) \]
\[ D_2 = \text{XOR}(D_3, D_6, D_7, D_{10}, D_{11}, D_{14}, D_{15}) \]
\[ D_4 = \text{XOR}(D_5, D_6, D_7, D_{12}, D_{13}, D_{14}, D_{15}) \]
\[ D_8 = \text{XOR}(D_9, D_{10}, D_{11}, D_{12}, D_{13}, D_{14}, D_{15}) \]
\[ D_{16} = \text{XOR}(D_1, \ldots, D_{15}) \]
\[ E_1 = \text{XOR}(R_1, 3, 5, 7, 9, 11, 13, 15) \]
\[ E_2 = \text{XOR}(R_2, 3, 6, 7, 10, 11, 14, 15) \]
\[ E_4 = \text{XOR}(R_4, 5, 6, 7, 12, 13, 14, 15) \]
\[ E_8 = \text{XOR}(R_8, 9, 10, 11, 12, 13, 14, 15) \]
\[ E_{16} = \text{XOR}(R_1, \ldots, 16) \]
Memory organization

write

read

write

read

1x8-demux

MUX 8x1

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