

## VLSI DESIGN TOOLS AND TECHNOLOGY (VDTT) PROGRAMME

Dated: 13.5.2010

**Sub: Admission to full time and Part-Time M. Tech programme in VDTT**

The following applicants have been tentatively selected pending approval from Dean, PGS&R, for Full Time and Part-Time M.Tech in VDTT Programme. On approval you will be intimated the date for payment of fees.

### Full-Time:

S. No.	Name	Sponsor's Name
1.	SUDARSHAN V.	NXP SEMICONDUCTORS
2.	DIVYA BHADAURIA	NXP SEMICONDUCTORS
3.	NIGESH	CADENCE
4.	HARIJOT SINGH BINDRA	CADENCE
5.	JASLEEN KAUR AHUJA	CADENCE
6.	DILEEP KUMAR R.	DST PROJECT
7.	L.N.V.LALITHA VURAKARANAM	EADS PROJECT
8.	POOJA SHARMA	IBM PROJECT
9.	BHUT PRASHANTKUMAR VALLABHBHAI	MHRD PROJECT
<b>Waiting List (Rank wise)</b>		
1.	SWAGATO BARMAN ROY	
2.	ARAVIND S.	
3.	VINNAKOTA L.B.K. MANOJA	
4.	ANAND ISSAC	
5.	SOUMIT BISWAS	
6.	I HITESHWAR RAO	
7.	HARIBABU CHIMAKURTHY	
8.	ANUEEJA S.	
9.	PRIYANKA KWATRA	
10.	AYAN DAS	
11.	S.J. BALAJI	
12.	SIDDHARTHA ASTHANA	
13.	MANUJ AGGARWAL	
14.	MANAS RANJAN DAS	
15.	DIPANJAN CHAKRABORTY	
16.	ADITYA ARVIND KAJWE	

Candidates in the waiting list will be offered admission based on the vacancy that arises for a given sponsor or project and the choice of the candidates & their performance in the interview.

**Part-Time:**

1.	SUNIL MEHTA	CADENCE
2	GAURAV SHARMA	CADENCE
3.	ABHISHEK CHAUDHARY	FREESCALE
4.	ROHIT SRIVASTVA	FREESCALE

(Prof. M. Jagadesh Kumar)  
Coordinator, VDTT Programme