

Metal-Oxide Semiconductor Field Effect Transistors

Need for a switch:

Diodes

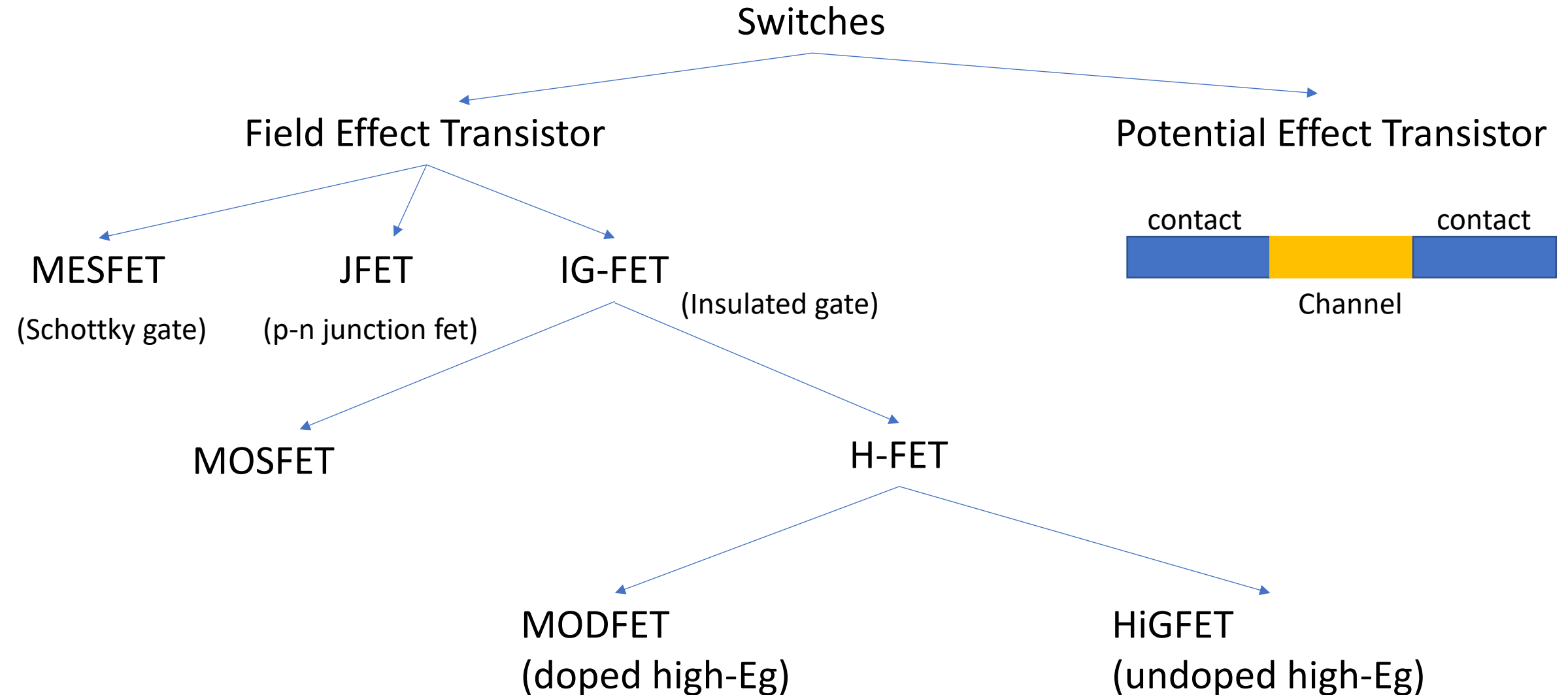
- Devices which current blocking characteristics used in rectifiers
- Varactors used in microwave devices and filters

Switches

- Three terminal devices useful in logic calculations
- Derived from vacuum tube devices used in computation



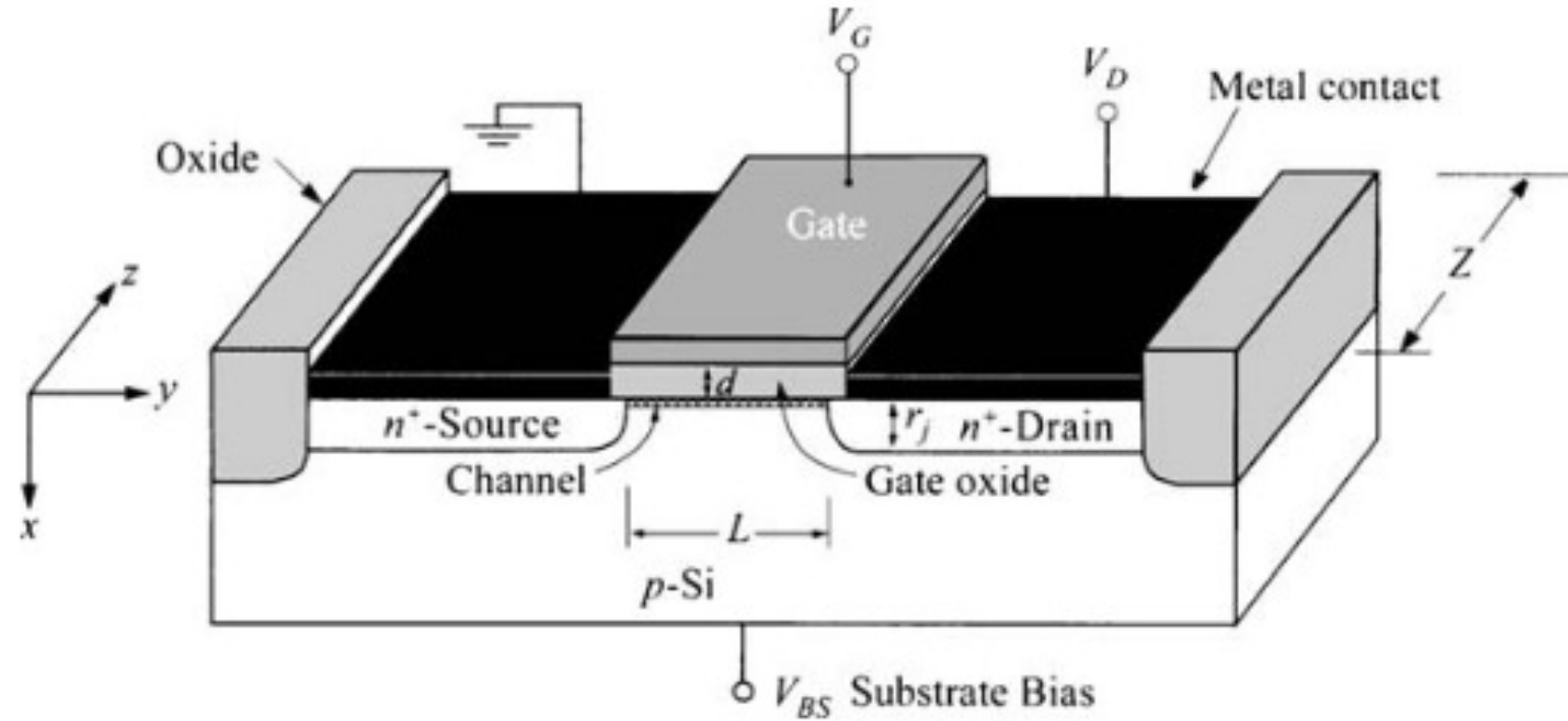
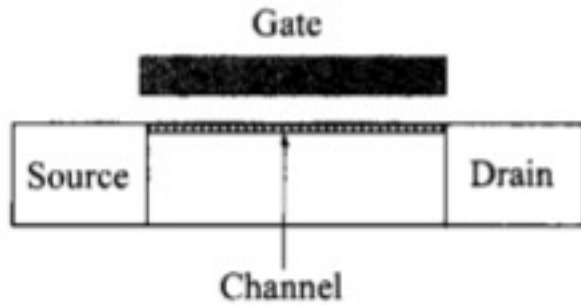
Electronic switch family



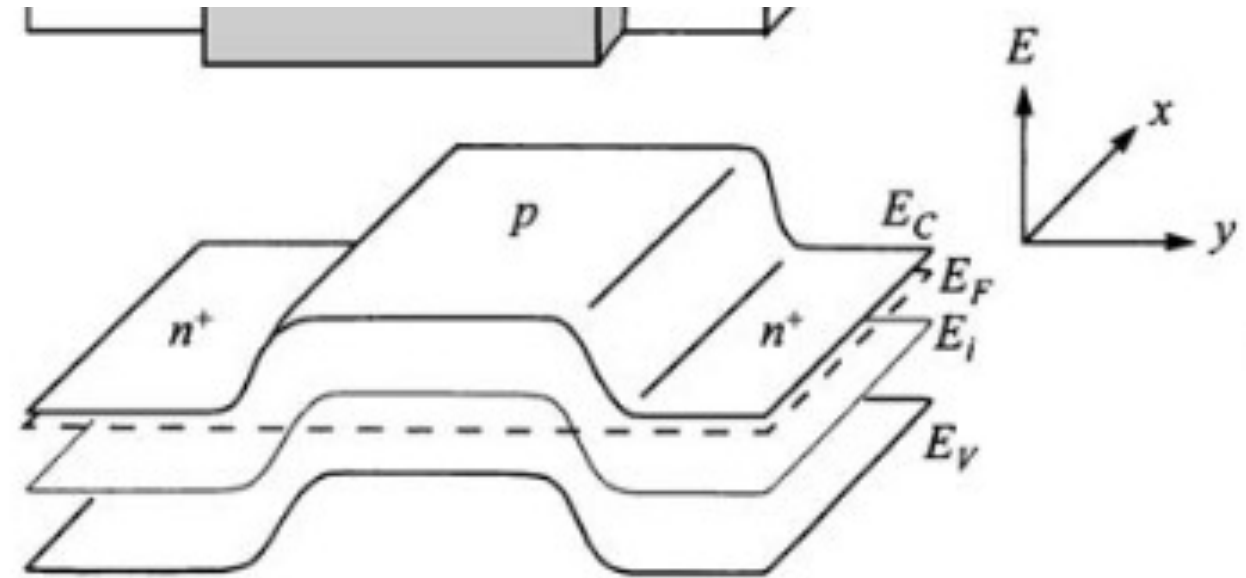
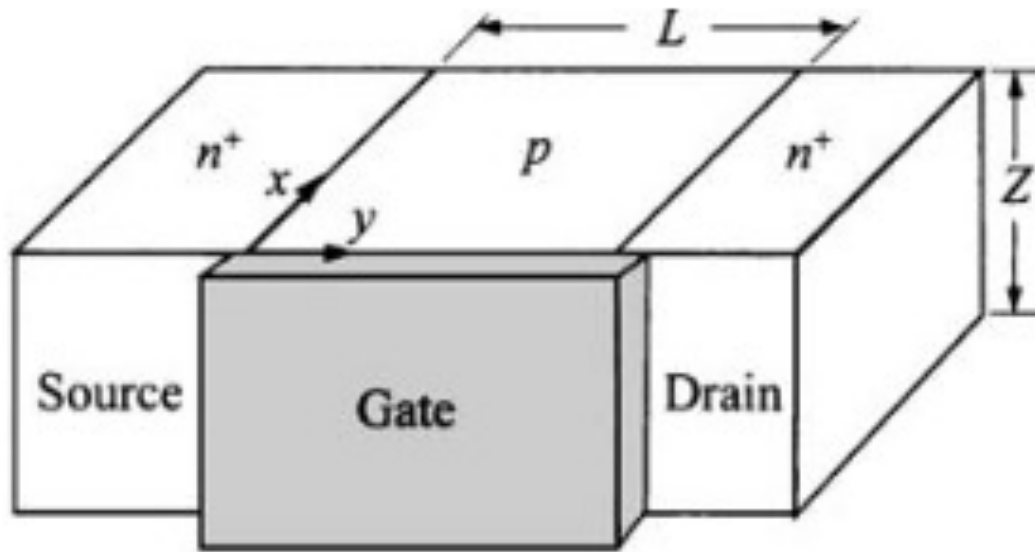
Advantages of FET

- The gate (insulated terminal) is formed either by oxide (MOSFET)/depletion width (JFET/MESFET)
- High input impedance
 - Input matched with microwave circuits
 - Can integrate multiple devices to same feed line
- Negative temperature coefficient, prevents thermal runaway
- No minority storage time/recovery
- Steep turn-on and turn off

Structure of MOS-FET

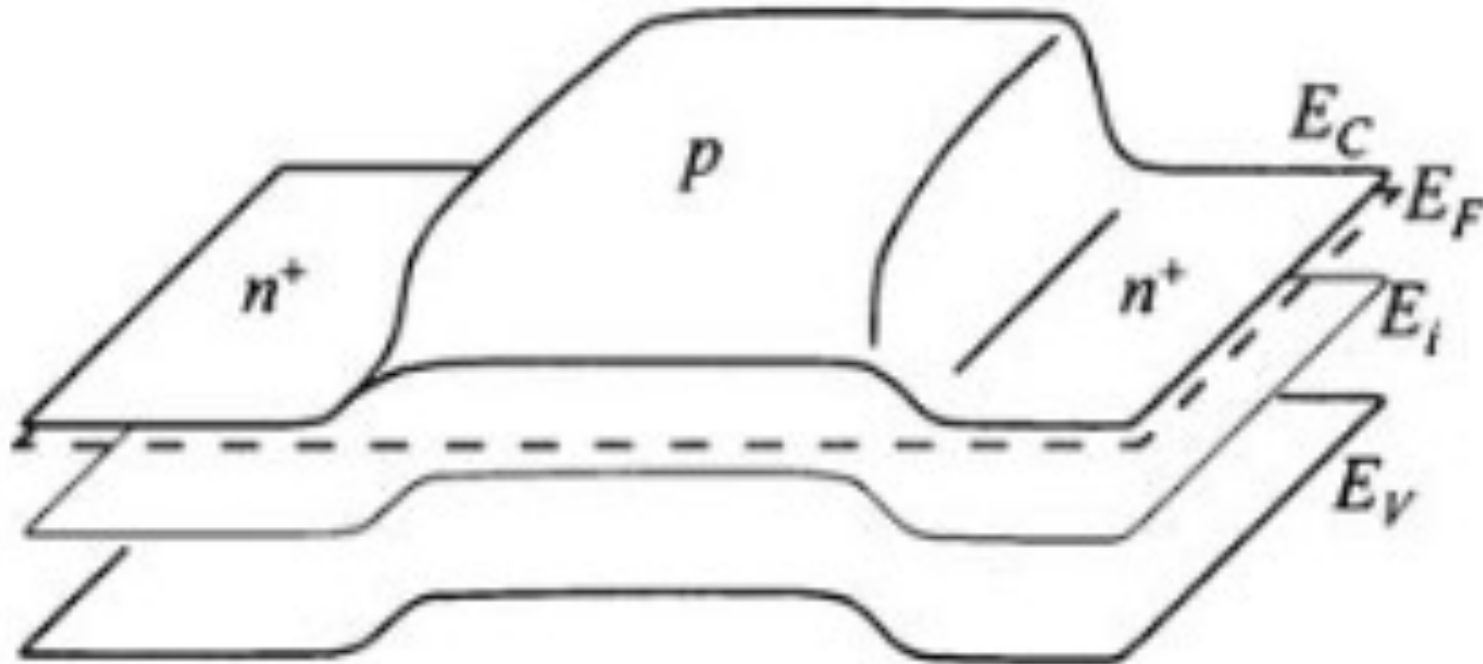
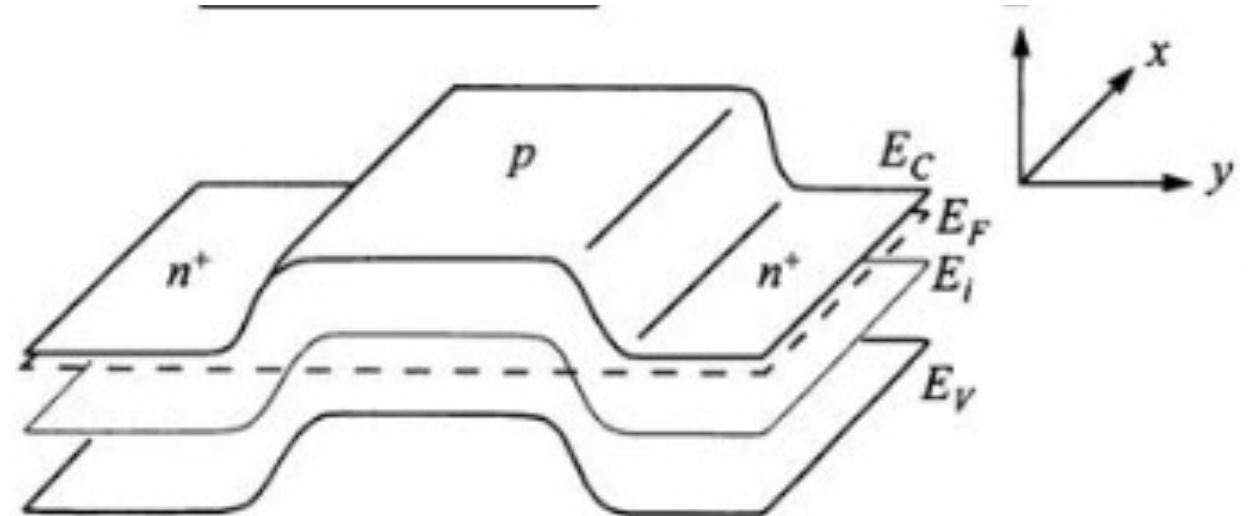
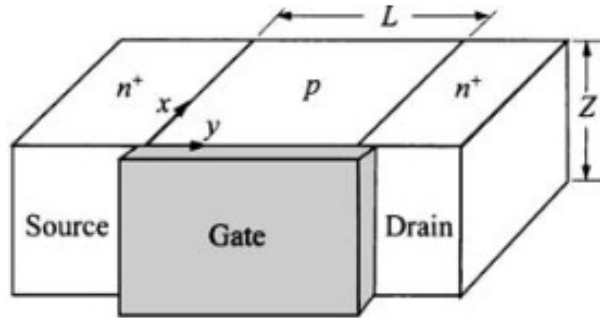


Equilibrium band structure



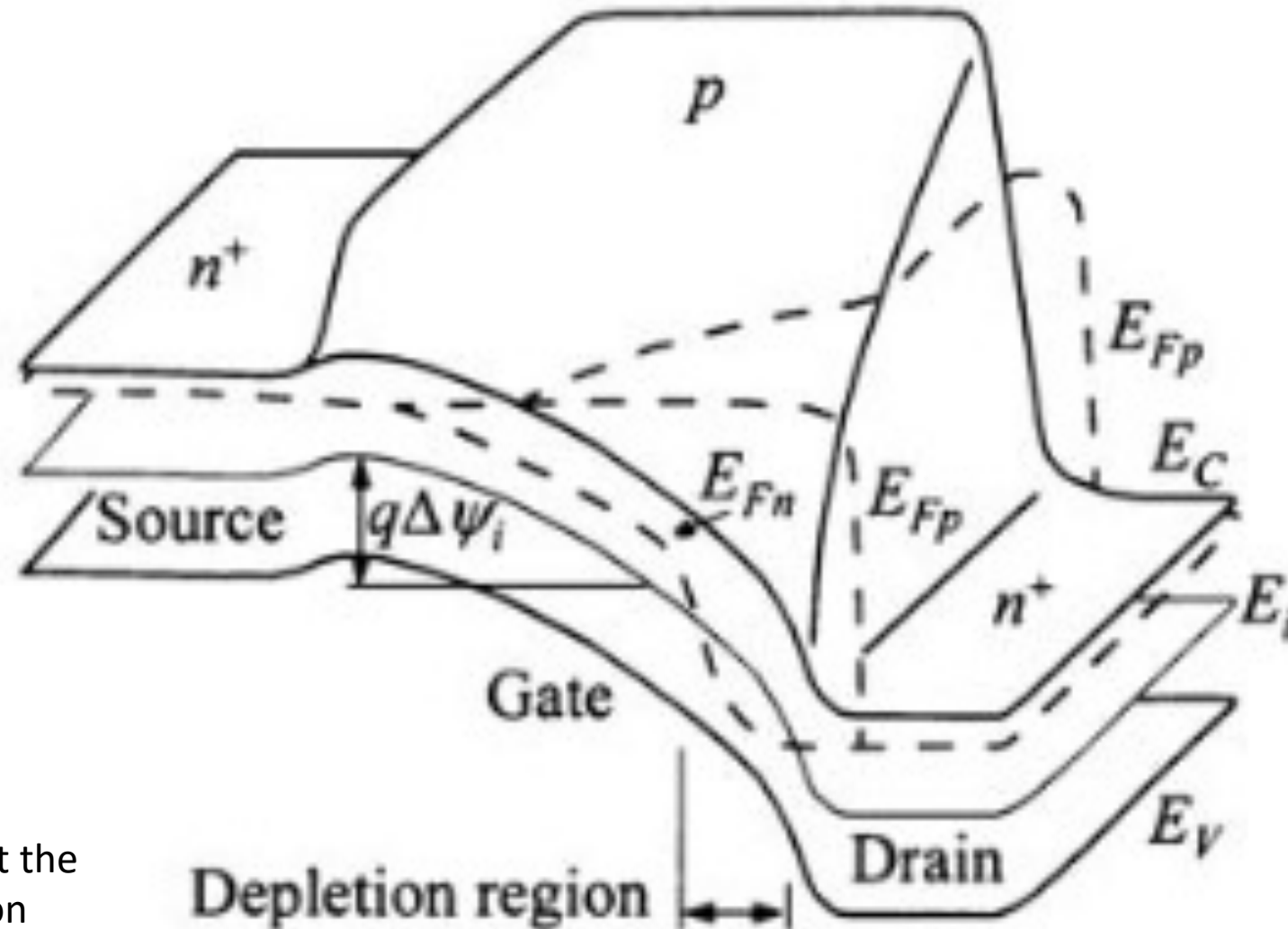
Equilibrium structure has band bending and depletion at junctions to prevent change carrier exchange

Channel Inversion



The P-type substrate is inverted to have a n-channel by applying a positive gate voltage

Under Drain and Gate Bias – Source grounded



Drain potential tends to offset the gate potential, reducing the electron population near the drain.

Effect of inversion under appropriate gate bias

Potential at the semiconductor-oxide surface $\psi_s = 2\phi_p = 2\phi_b$

The source potential changes the surface potential:

let the change in the potential be $\psi_i(y)$

The total potential at the surface is now $\psi_s(y) = 2\phi_b + \psi_i(y)$

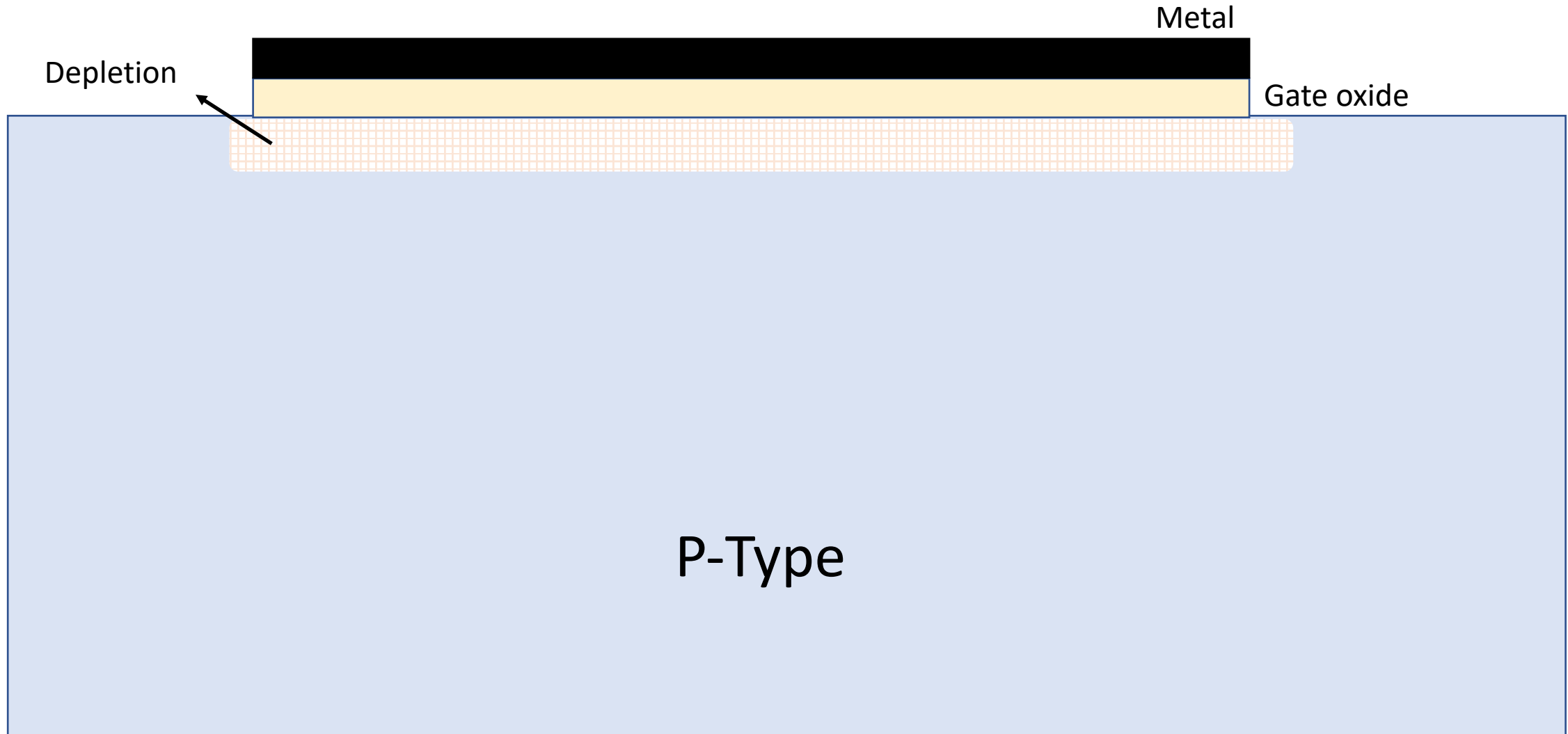
The electric field in the oxide $\mathcal{E}_{ox} = \frac{V_G - \psi_s}{t_{ox}}$

The electric field in the semiconductor $\mathcal{E}_s = \sqrt{\frac{2qN_A\psi_s}{\epsilon_s}}$

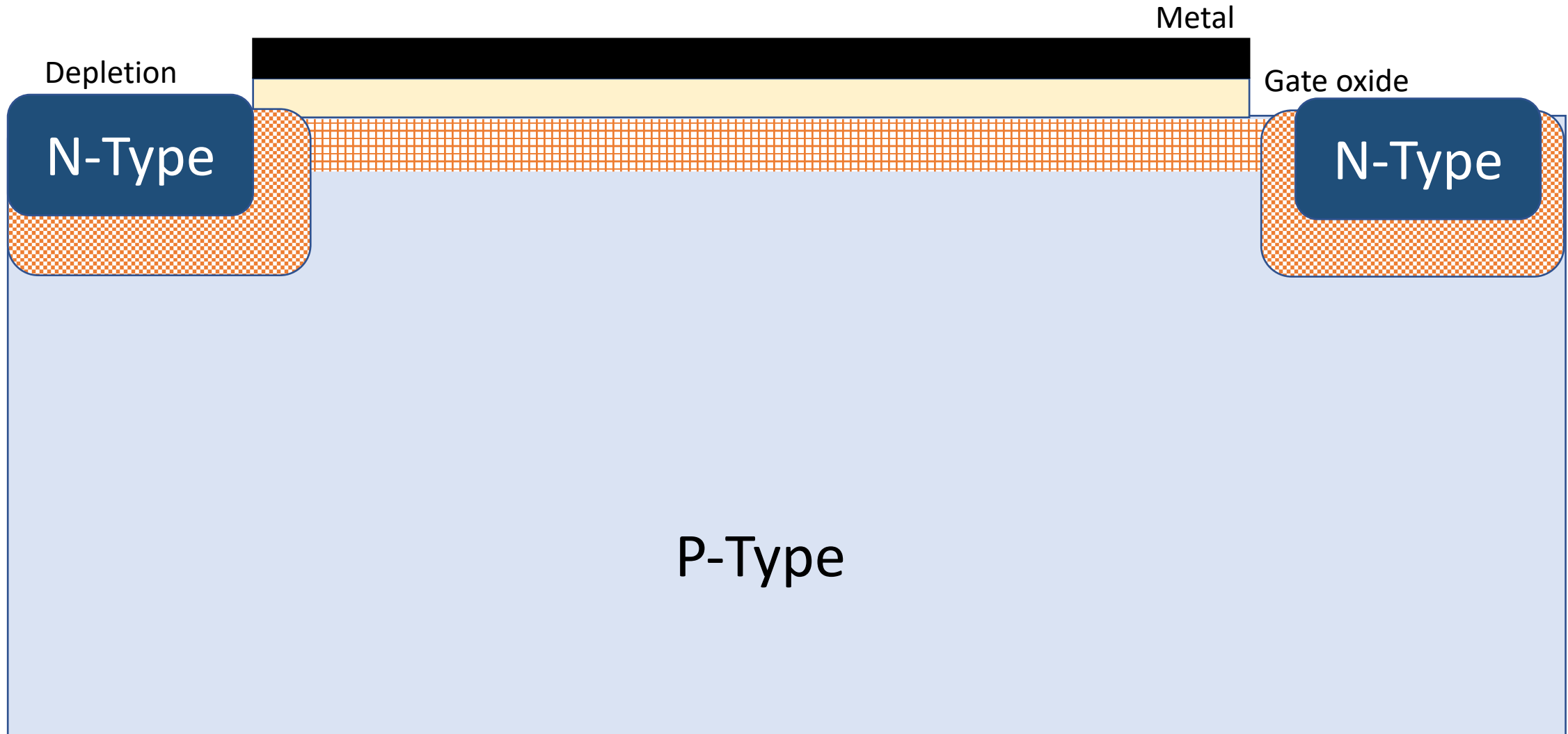
Gauss Law: Electric flux $\Phi = \frac{Q}{\epsilon}$

Flux emanating from a volume enclosed by a surface σ

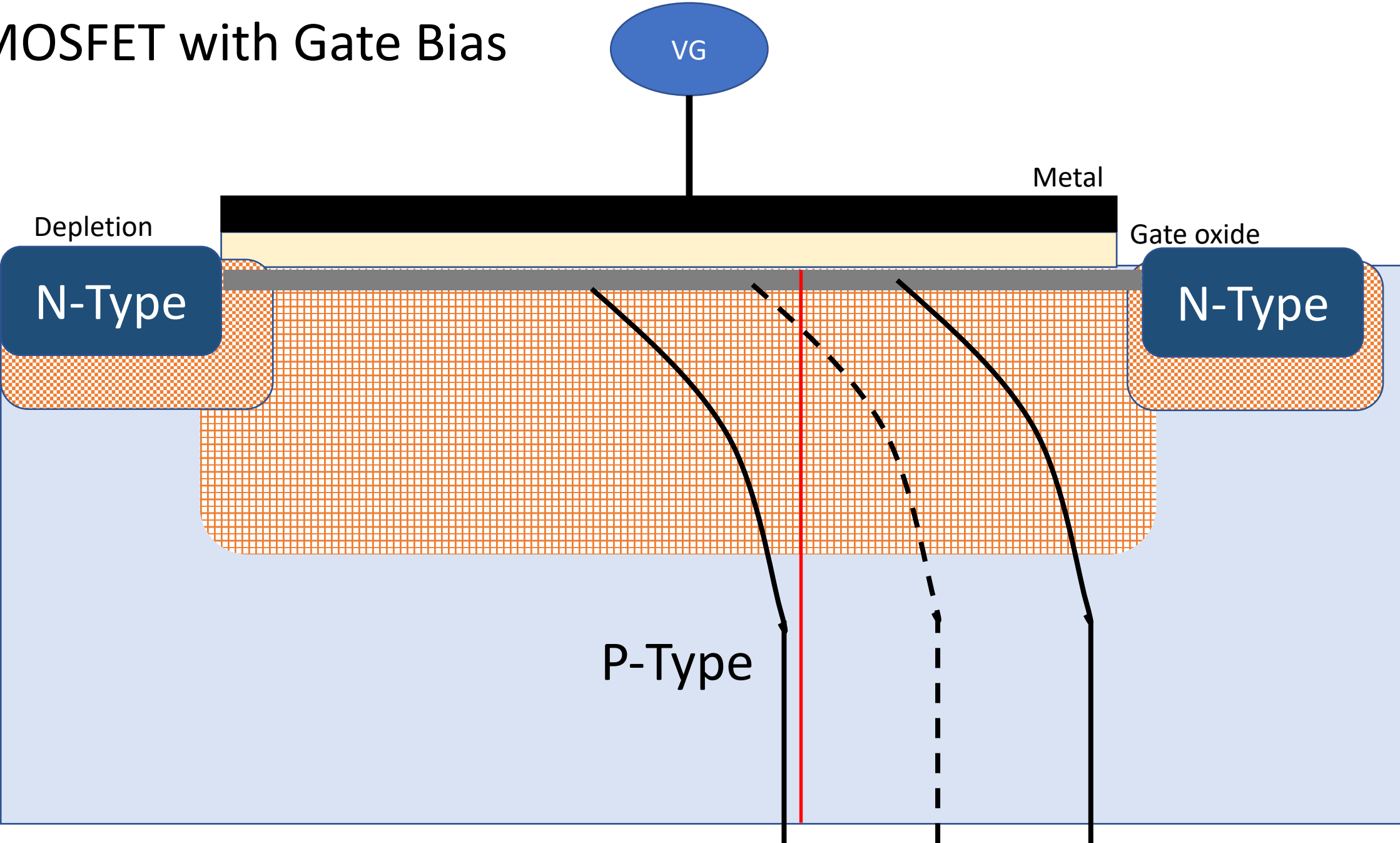
Thermal Equilibrium



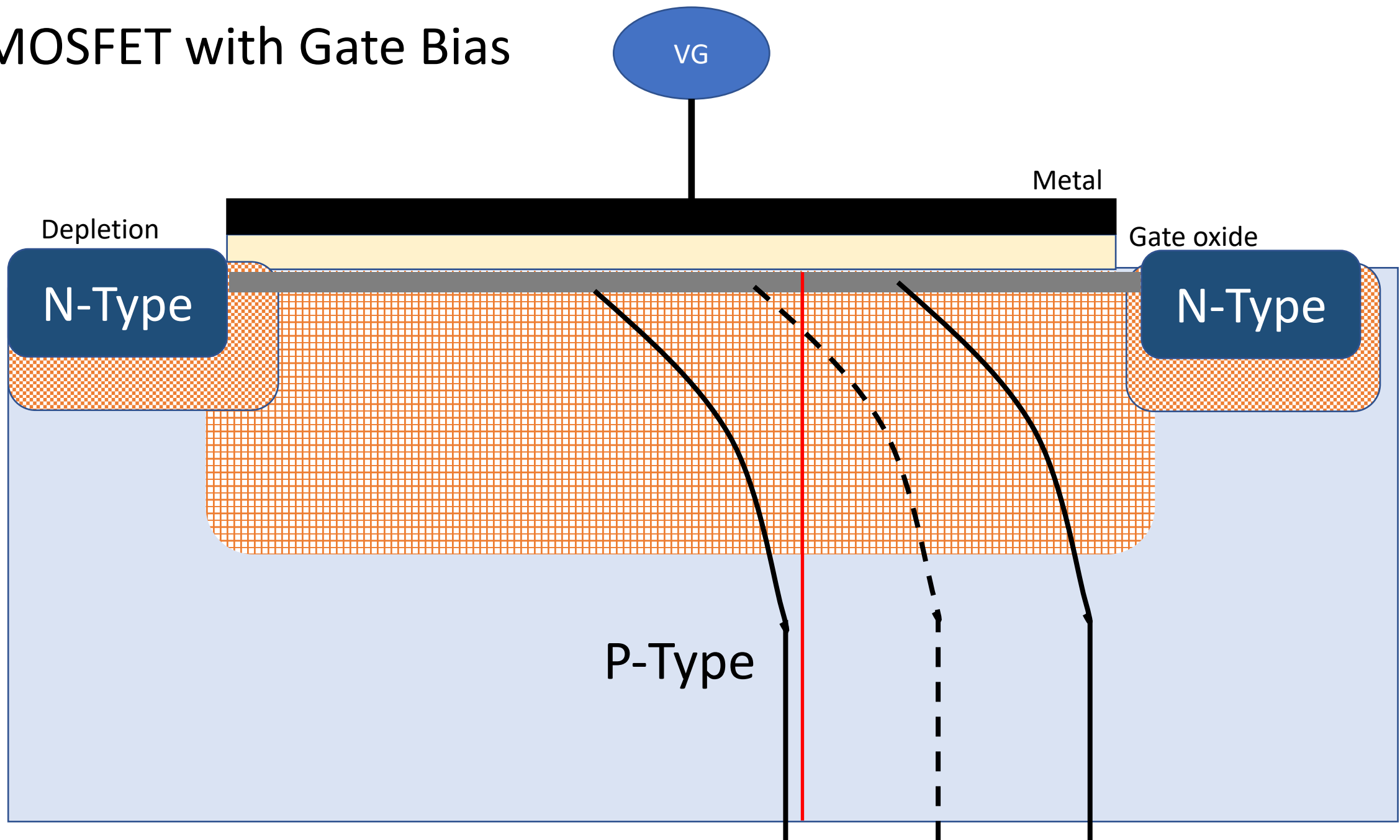
Source and Drain diffusions



MOSFET with Gate Bias



MOSFET with Gate Bias



Let us imagine a surface

The electric flux $\Phi = \oiint E \cdot dA$

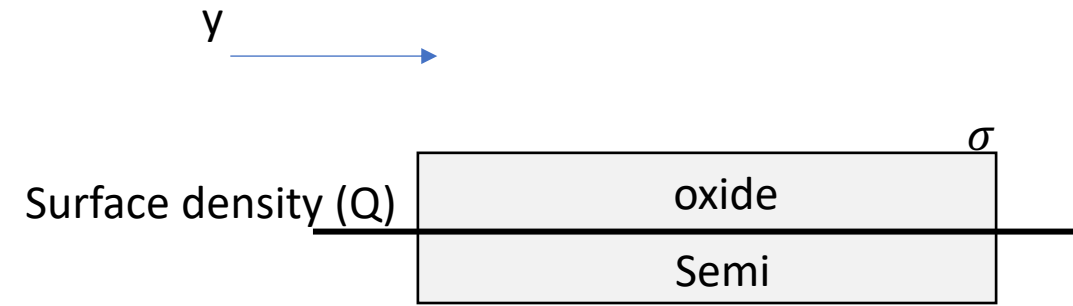
Assume things do not change in the x direction

Then the charge density varies along the y direction as

$$Q_n(y) = \left[\epsilon_{ox} \frac{V_G - \psi_s}{t_{ox}} - \epsilon_s \sqrt{\frac{2qN_A\psi_s}{\epsilon_s}} \right]$$

If we define the oxide capacitance as $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

$$Q_n(y) = [C_{ox}[V_G - \psi_s] - \sqrt{2q\epsilon_s N_A \psi_s}]$$



Ideal Current – voltage relationship

A few assumptions:

1. There are no interface traps sites and we start at flat band approximation
2. Current is mostly drift (what ever is the variation in charge in y , is not that significant for diffusion)
3. Channel doping is uniform and there is negligible reverse current
4. The gate field is much larger than the source-drain field (Gradual channel approximation)

Current at any point y is given by $I(y) = eWQ(y)v$

Where W is the width of the channel and v is the velocity

Constant mobility approximation: $v = \mu\mathcal{E}$

Length normalized current is given by $I = e\mu \frac{W}{L} \int_0^L Q(y)\mathcal{E}(y)dy$

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Field is gradient of potential

$$I = \frac{e\mu W}{L} \int_0^L Q_n \left(\frac{d\psi_i(y)}{dy} \right) dy$$

Changing the limits of integration: The potential varies from 0 at source to V_D at the drain

$$I = \frac{e\mu W}{L} \int_0^{V_D} Q_n(\psi_i) d\psi_i$$

$$Q_n(y) = [C_{ox}[V_G - \psi_s] - \sqrt{2q\epsilon_S N_A \psi_s}]$$

$$\psi_s(y) = 2\phi_b + \psi_i(y)$$

$$Q_n(y) = [C_{ox}[V_G - 2\phi_b - \psi_i(y)] - \sqrt{2q\epsilon_S N_A (2\phi_b + \psi_i(y))}]$$

$$I = \frac{W}{L} \mu C_{ox} \left\{ \left(V_G - 2\phi_b - \frac{V_D}{2} \right) V_D - \frac{2}{3} \frac{\sqrt{2\epsilon_S q N_A}}{C_{ox}} \left[(V_D + 2\phi_b)^{\frac{3}{2}} - (2\phi_b)^{\frac{3}{2}} \right] \right\}$$

In the presence of non-ideal situations, add the flat band condition $V_G = V_G - V_{FB}$

$$I = \frac{W}{L} \mu C_{ox} \left\{ \left(V_G - V_{FB} - 2\phi_b - \frac{V_D}{2} \right) V_D - \frac{2}{3} \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} \left[(V_D + 2\phi_b)^{\frac{3}{2}} - (2\phi_b)^{\frac{3}{2}} \right] \right\}$$

Situation: 1 Small V_D

$$I = \frac{W}{L} \mu C_{ox} \left\{ \left(V_G - V_{FB} - 2\phi_b - \frac{V_D}{2} \right) V_D - \frac{2}{3} \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} \left[3 \sqrt{\frac{\phi_b}{2}} V_D \right] \right\}$$

$$V_T = V_{FB} + 2\phi_b + \frac{\sqrt{2\epsilon_s q N_A (2\phi_b)}}{C_{ox}}$$

$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D$$

The current increases linearly with V_D for some extent and then decreases according to the equation

For the condition that $V_D \ll (V_G - V_T)$

Oh, it pinches

As the drain potential is raised, the current according to the approximation reaches a maximum and then decreases.

However, the decrease is unphysical due to the approximations taken

The increase in current with the potential decreases because, the channel is pinched.

The charge density near the drain is reduced due to the drain potential becoming as significant as the gate

The drain depletion width increases.

Pinch-off is a condition when $Q(y = L) = 0$ – That is the edge of the channel first gets depleted.

$$Q_n(y) = \left[C_{ox} [V_G - 2\phi_b - \psi_i(y)] - \sqrt{2q\epsilon_s N_A (2\phi_b + \psi_i(y))} \right]$$

The equation can be solved and the equation for saturation potential is given by

$$V_{Dsat} = \Delta\psi_i(L) = V_G - V_{FB} - 2\phi_b + K^2 \left[1 - \sqrt{1 + \frac{2(V_G - V_{FB})}{K^2}} \right] \quad \text{Where } K = \frac{\sqrt{\epsilon q N_A}}{C_{ox}}$$

Now as before

$$I_D = \frac{W}{L} \int_0^L Q_n(y) v(y) dy$$

Substitute the pinched off charge density

$$I_D = \frac{W}{2ML} \mu_n C_{ox} (V_G - V_T)^2$$

$$\text{Where } M = 1 + \frac{K}{2\sqrt{\phi_b}}$$

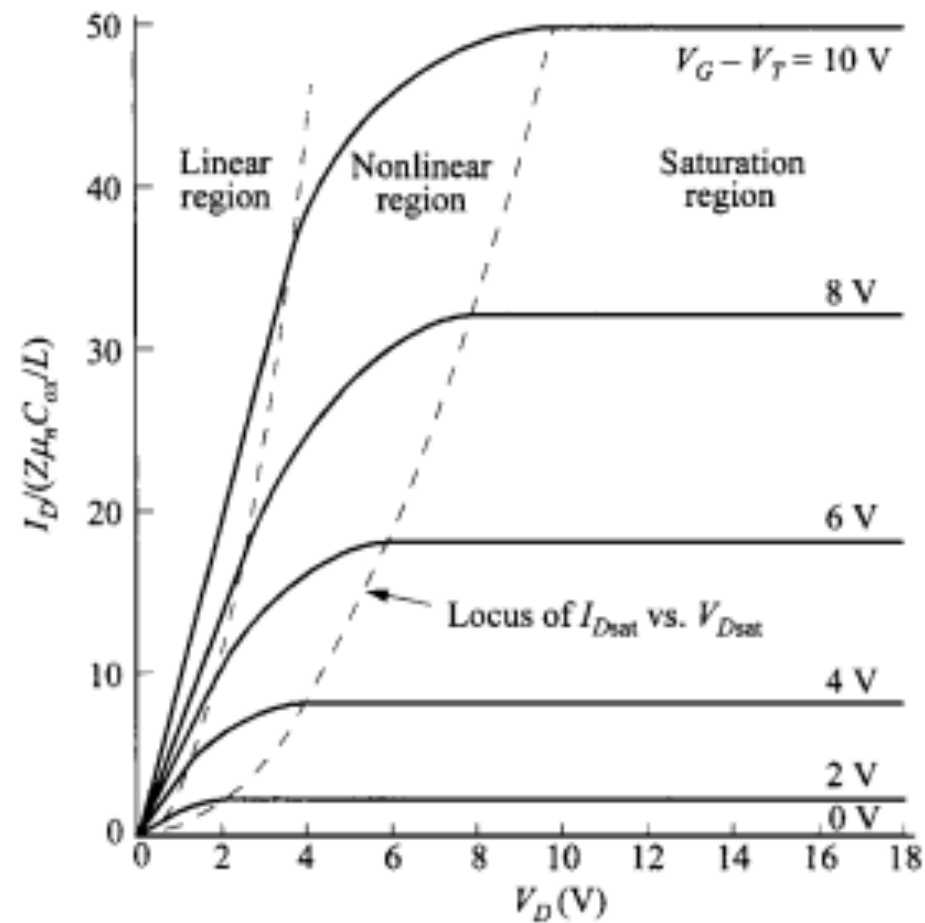
A more convenient expression for the saturation potential is $V_{Dsat} = \frac{(V_G - V_T)}{M}$

At any point one can define the conductance $\sigma = \frac{dI_D}{dV_D}$

In the linear region, there is constant conductance and the conductance drops significantly in the saturation as $\delta\sigma \rightarrow 0$

Finally in the nonlinear region, the current can be described by

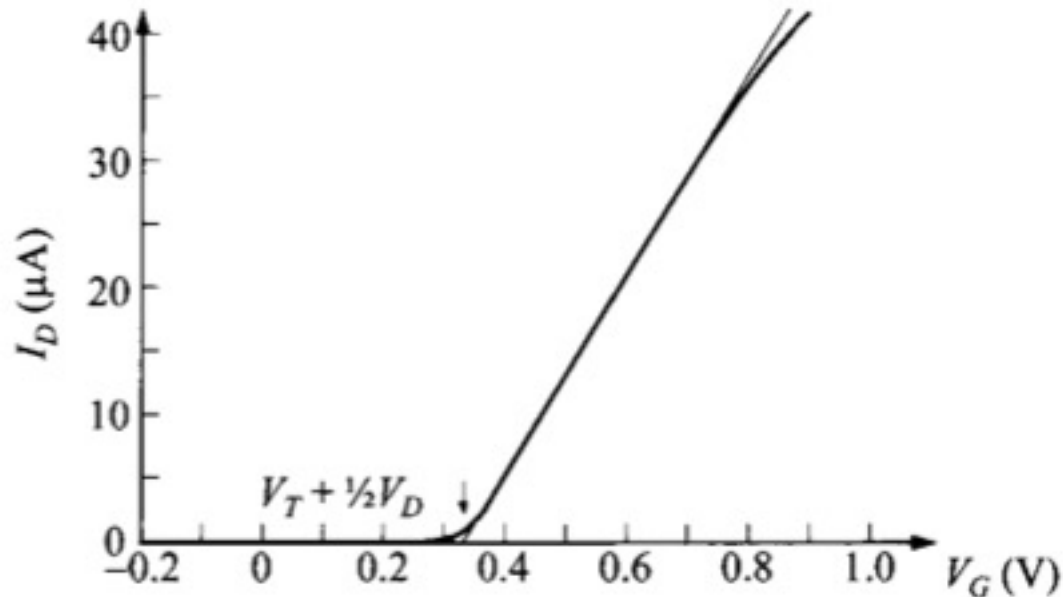
$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_T - \frac{M V_D}{2} \right) V_D$$



Threshold and Sub-Threshold

As in the moscap, in the presence of nonzero ϕ_{ms} and fixed oxide charges Q_f

$$\text{The threshold voltage } V_T = \phi_{ms} - \frac{Q_f}{C_{ox}} + 2\phi_b + \frac{\sqrt{4\epsilon q N_A \phi_b}}{C_{ox}}$$



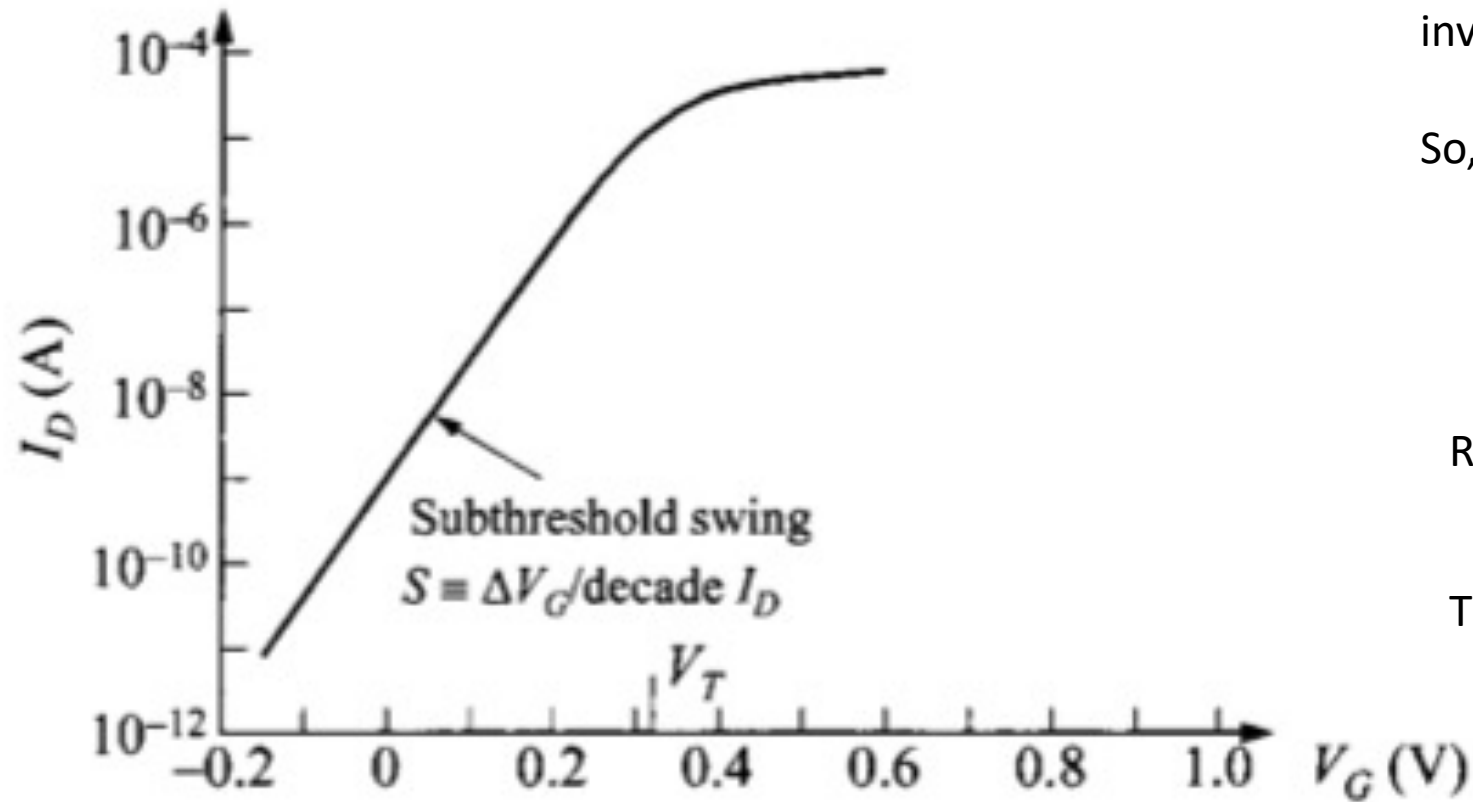
The current in the mosfet is linear for small drain voltages.

In a real-world mosfet, the linear region of I_D - V_G can be employed to identify the threshold voltage.

The extrapolated voltage (intercept to the x axis)

$$V_x = V_T + \frac{1}{2}V_D$$

Below the threshold voltage,



In the sub-threshold, there is absence of inversion region .

So, the current cannot be carried by drift.

$$J_D(y) = qD_n d \frac{N(y)}{dy}$$

Remember, y direction is along the S-D axis.

The overall current density can be approximated by

$$I_D = WqD_n \frac{N(S) - N(D)}{L}$$

Carrier density at the source: $N(S) = \int_0^{W_D} n(x)dx = n_{p0} \int_{\psi_s}^0 e^{\beta\phi_b} d\phi_b$

Since the potential in the depletion width is known the above expression can be simplified as

$$N(s) = \frac{1}{\beta} \sqrt{\frac{\epsilon}{2q\psi_s N_A}} n_{p0} e^{\beta\psi_s}$$

The carrier density at the drain end is lowered exponentially by the drain potential

$$N(D) = N(S)e^{-\beta V_D}$$

Substituting we get

$$I_D = \frac{W}{L} \frac{\mu_n}{\beta^2} e^{\beta\psi_s} [1 - e^{-\beta V_D}]$$

Sub-Threshold Swing

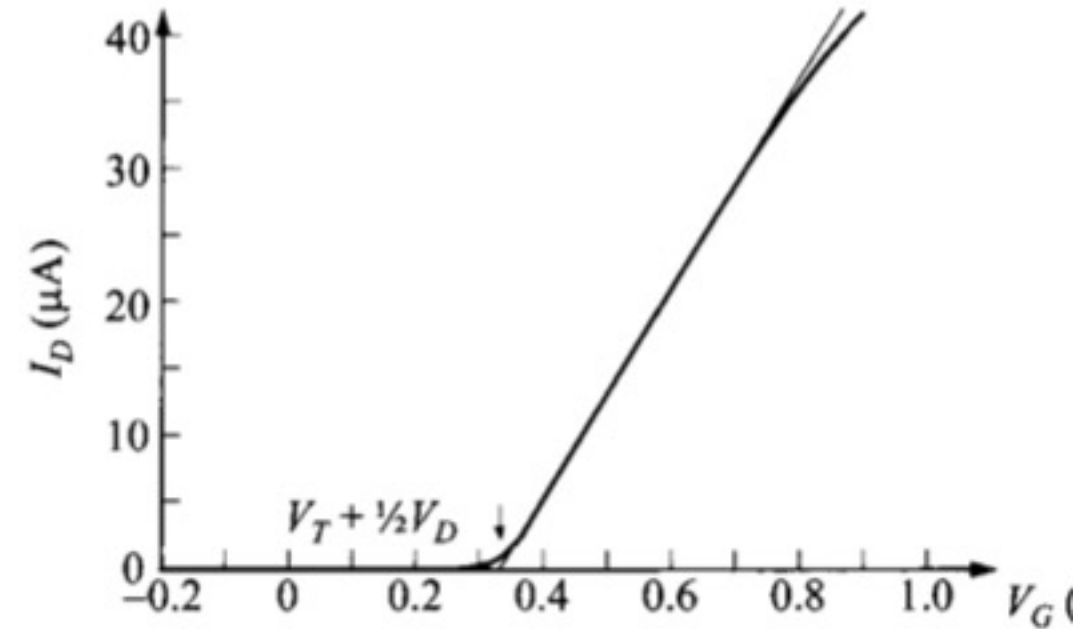
- The measure of how sharply the transistor can be turned on/off
- $\ln(I_D) = K(\beta\psi_s)$
- We define the sub-threshold slope

$$S = \ln(10) \frac{dV_G}{d(\ln I_D)}$$

Since, $V_G - V_{FB} = \psi_s + \sqrt{2\epsilon_s q N_A / C_{ox}}$

$$\frac{dV_G}{d\psi_s} = 1 + \frac{1}{C_{ox}} \left[\sqrt{\frac{\epsilon_s q N_A}{2\psi_s}} \right] = 1 + \frac{C_D}{C_{ox}}$$

$$S = \ln 10 \frac{1}{\beta} \frac{dV_G}{d\psi_s} = \ln 10 \frac{kT}{q} \left(1 + \frac{C_D}{C_{ox}} \right)$$



Steeper slope is obtained, when S is small. Hence, you want to work at low temperature and have small oxide thickness

Effect of Temperature

- Remember the three regions of transport in a MOSFET

- Linear $I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D$
- Saturation $I_D = \frac{W}{2ML} \mu_n C_{ox} (V_G - V_T)^2$
- Non-linear $I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_T - \frac{MV_D}{2} \right) V_D$
- Sub-threshold $I_D = \frac{W}{L} \frac{\mu_n}{\beta^2} \sqrt{\frac{q\epsilon_S N_A}{2\psi_S}} \left(\frac{n_i}{N_A} \right)^2 e^{\beta\psi_S}$

Temperature affects the electron distribution in the material and hence the threshold for the strong inversion.

Effect of Temperature on Threshold

$$V_T = \phi_{ms} - \frac{Q_f}{C_{ox}} + 2\psi_p + \frac{\sqrt{4\epsilon_s q N_A \psi_p}}{C_{ox}}$$

We can assume the work function and the density of fixed charges are temperature invariant

The resulting equation is mostly dependent on ψ_p and so if we know $\frac{d\psi_p}{dT}$

$$\text{Then } \frac{dV_T}{dT} = \frac{d\psi_p}{dT} \left(\frac{dV_T}{d\psi_p} \right) = \frac{d\psi_p}{dT} \left[2 + \frac{1}{C_{ox}} \sqrt{\frac{\epsilon_s q N_A}{\psi_p}} \right]$$

Since, ψ_p is the separation from the intrinsic energy level,

$$\psi_p = \beta \ln \frac{N_A}{n_i^2}$$

Remember, $n_i^2 = T^3 e^{-\frac{E_G}{KT}}$

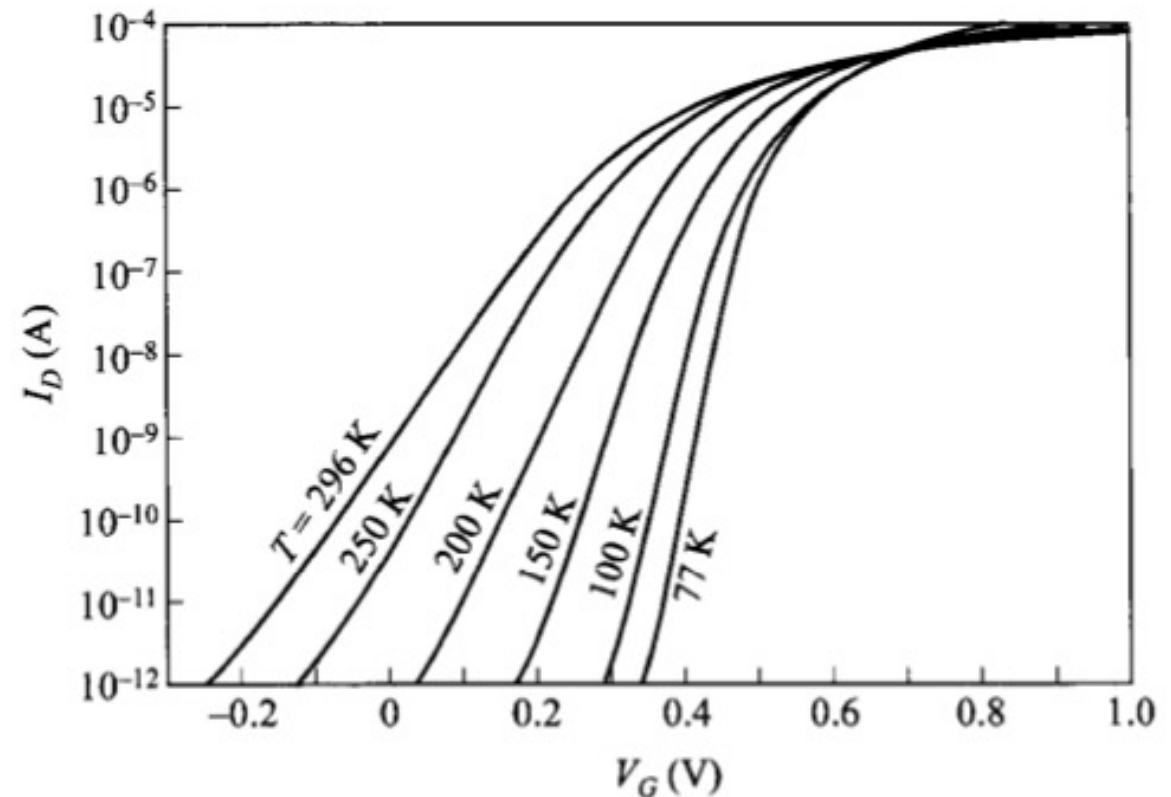
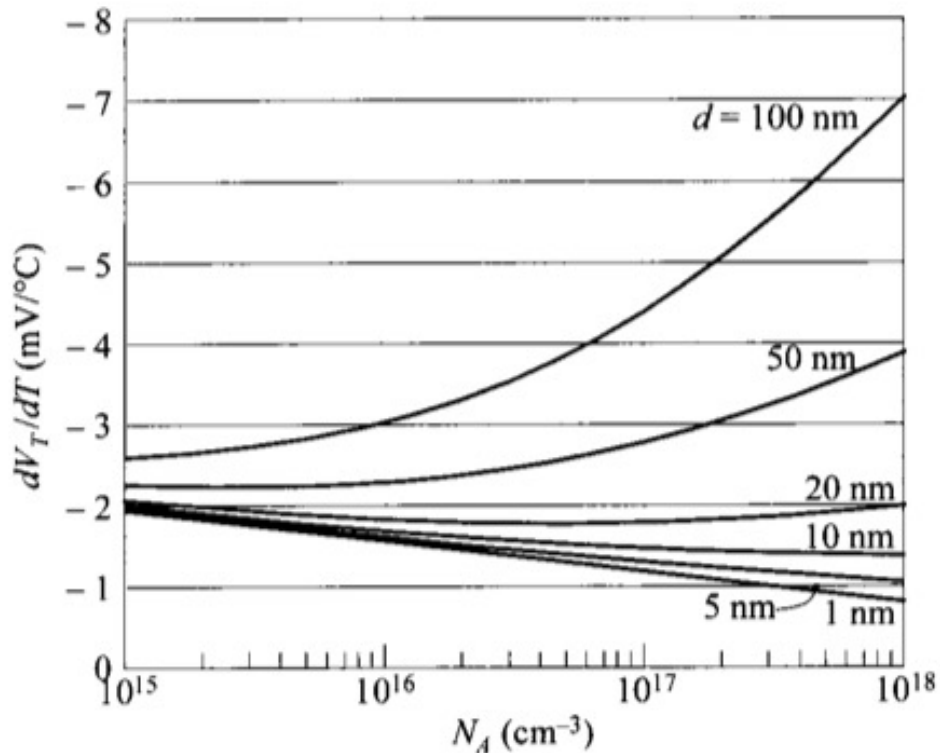
If we substitute everything $\frac{d\psi_p}{dT} = \frac{1}{T} \left[\psi_p - \frac{E_G}{2q} \right]$

Since $\psi_p < \frac{E_{G0}}{2}$, the function $\frac{d\psi_p}{dt}$ is always negative and hence, increase in temperature reduces the threshold.

Or decreasing the temperature increases the threshold voltage. This improves the MOSFET characteristics, by increasing the noise margin.

Decreasing the temperature also reduces S and provides steep transfer characteristics.

Improvement in sub-threshold swing at 77K is by about a factor of 4



Control over threshold

The expression for threshold potential $V_T = V_{FB} - \frac{Q_D}{C_{ox}} + 2\phi_p$

The depletion charge was initially $Q_D = -\sqrt{2\epsilon_s q N_A (2\phi_p)}$

If the body of the silicon substrate is set to a potential V_B , the source-body depletion and the source-drain depletion width are changed. This creates another field countering the gate field.

This will make the gate field to work even harder, causing the threshold voltage to increase.

The final threshold voltage $V_T = V_{FB} + 2\phi_p + \frac{\sqrt{2\epsilon_s N_A (2\phi_p - V_{BS})}}{C_{ox}}$

$$\Delta V_T = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} \left[\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p} \right]$$

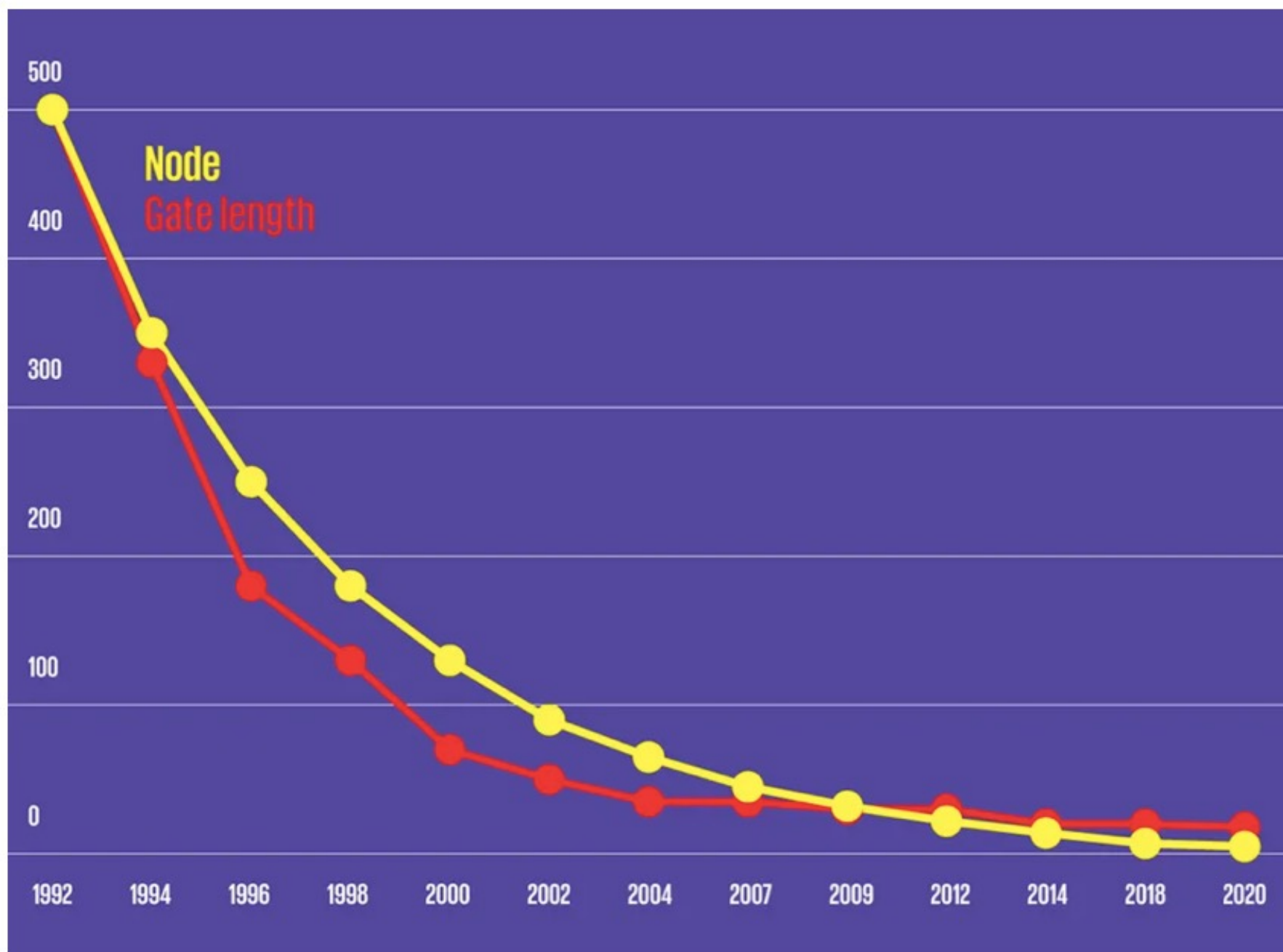
Remember for a N-channel, VBS is negative to increase the S-B depletion

Short Channel Effects

Scale the Device

Change the dimensions of the device: Why ?

- Dennard (IBM) in 1959 suggested, if you shrink the MOSFET dimensions with an appropriate change in the other device dimensions, an improvement in packing density, speed and power dissipation can be obtained.
- If the length and width of the MOSFET channel (typically the gate dimension) is reduced by K , then the vertical dimensions of source drain junction depths, gate insulator thickness and other dimensions should be suitably scaled along with the power supply voltage as well
- However, voltage cannot be scaled independently as the transistor in a processor needs to work with other devices on the mother board as well.
- This causes enormous issues and has been the area of research in semiconductor device physics for more than 50 years now!!!



SOURCES: STANFORD NANOELECTRONICS LAB, WIKICHIP, IEEE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2020

Deviation from the long-channel approximation [gradual-channel approximation]

When the devices are scaled (shrunk), if the electric field in the channel (S-D)

$$\mathcal{E}_y = \frac{V_{DS}}{L}$$

Can increase such that $\mathcal{E}_y$ becomes comparable to $\mathcal{E}_x$

Thus the two-dimensional potential at the surface deviates from GCA and the simplified expressions we obtained.

We therefore have the famous short channel effect

So what happens when the electric field gets increased ?

Mobility is the ease of an electron to respond to the electric field. For small enough fields

$$v = \mu \mathcal{E}$$

ie, the velocity increases linearly with the applied electric field.

However, there are many other processes in the semiconductor. The electron scatters off defects, phonons and other impurities

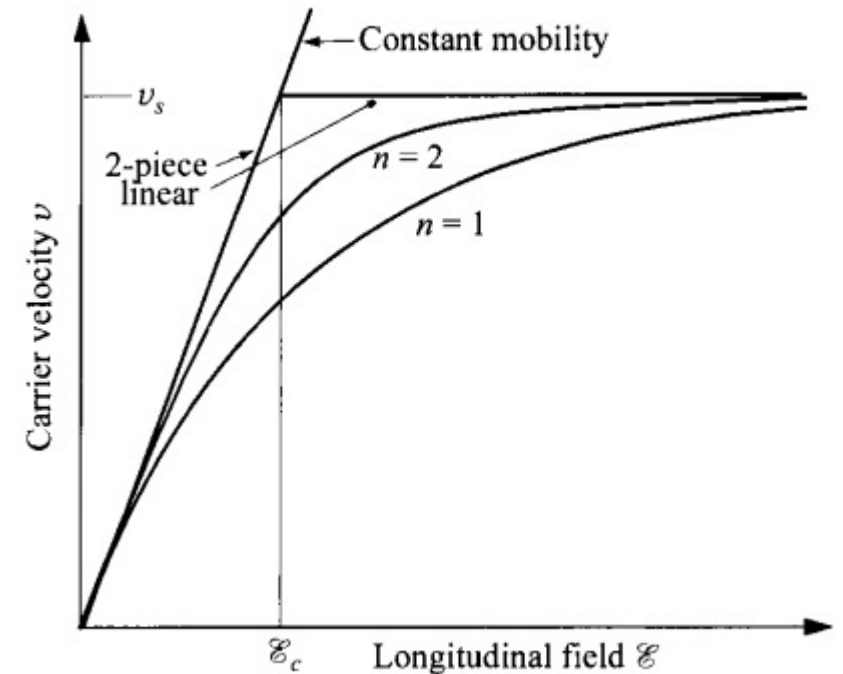
This leads to issues with velocity scaling linearly with the electric field.

After a certain point, the electron velocity cannot increase further. The scattering rate increases with the electron velocity.

This causes the velocity to saturate called as the saturation velocity v_s

In-between the linear mobility and the saturation regime, the velocity is described by the relation

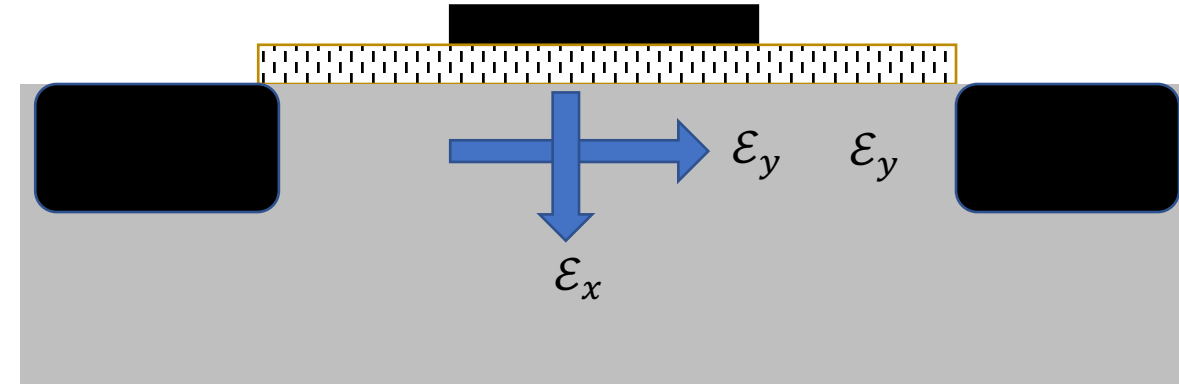
$$v(\mathcal{E}) = \frac{\mu \mathcal{E}}{\left[1 + \left(\frac{\mu \mathcal{E}}{v_s} \right)^n \right]^{\frac{1}{n}}}$$



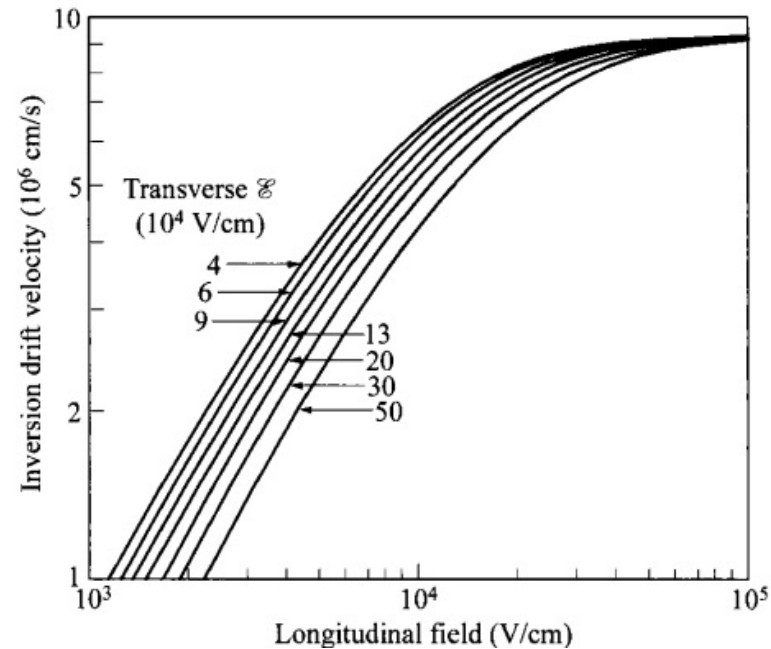
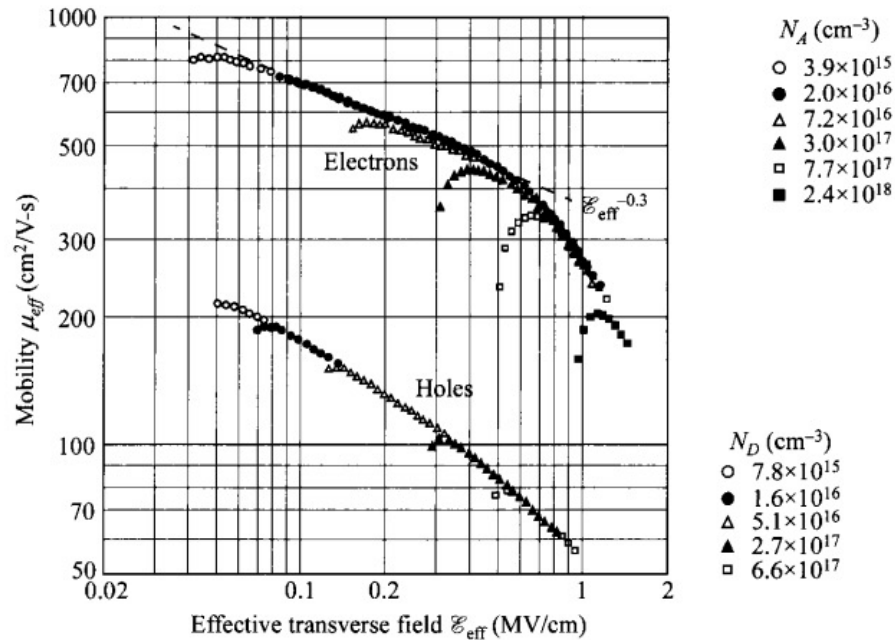
Fields in the MOSFET channel

Longitudinal field $\mathcal{E}_y$ parallel to the surface

Transverse field $\mathcal{E}_x$ parallel to the gate



Experimental measurements show that the low field mobility is a unique function of $\mathcal{E}_x$



As the transverse field is increased, the velocity saturation behavior is altered significantly. This causes strong deviations from the long-channel approximation

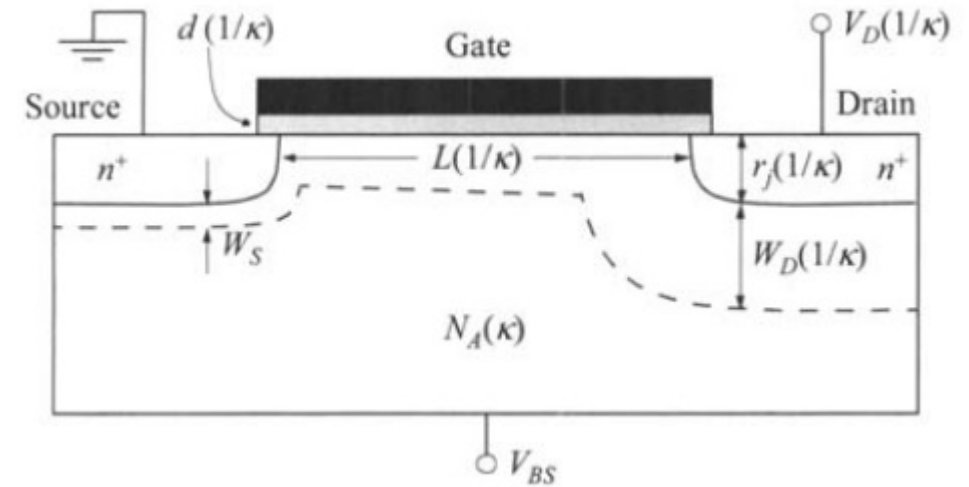
Ideal scaling rule

Ideal scaling is obtained, when you maintain the electric fields constant before and after scaling

If the channel length and the width is reduced by K

- Oxide thickness scaled by $1/K$
- V_T scaled by $1/K$
- V_D scaled by $1/K$
- N_A scaled by K

Keeps the $\mathcal{E}$ the same in the semiconductor.



Sub-threshold swing S remains unaffected since $1 + C_D/C_{ox}$ remains unaffected.

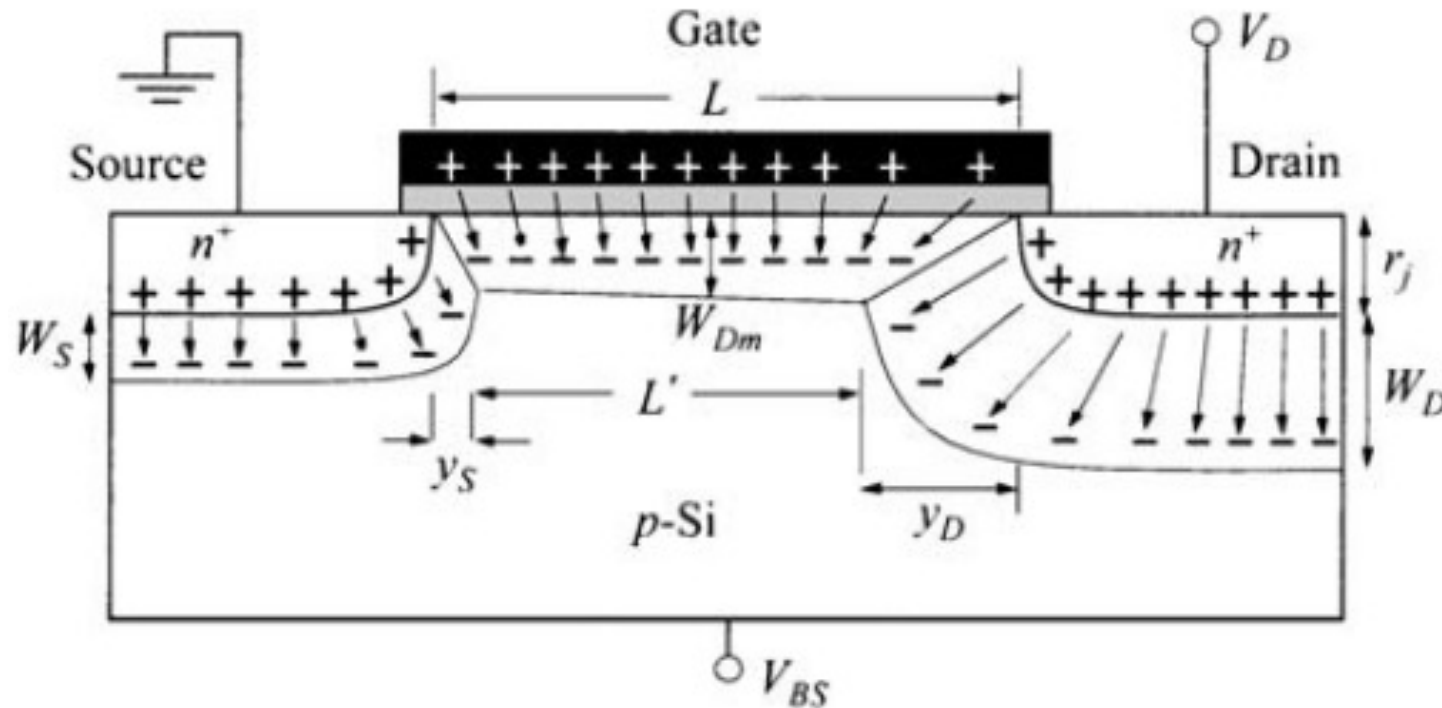
Though ideal, it all seems, the properties could not be scaled in practice.

- V_T cannot be scaled so easily by the doping density due to log dependence. 10% change is obtained by an order of magnitude change in the doping density
- Gate oxide cannot be made very thin due to practical difficulties, defects and tunneling through very thin films
- The source and drain contact resistances scale with the shrinking contacts
- Increasing the substrate doping density reduces the depletion width in the drain side, this causes P-N junction breakdown
- The voltage supply cannot be changed independently, it depends on several other factors.

Charge Sharing

Till now, the gate charge was assumed to be totally countered by the semiconductor depletion and inversion.

However, in practice, the gate field will also be terminated by source and drain depletion .



(a)

$$V_T = V_{FB} + 2\phi_p + \frac{Q_D}{C_{ox}A} \text{ where } A \text{ is the } W \cdot L \text{ the area of the transistor in the ideal case.}$$

However, as discussed before, for the long channel, the source and drain depletion widths are much smaller in comparison with L

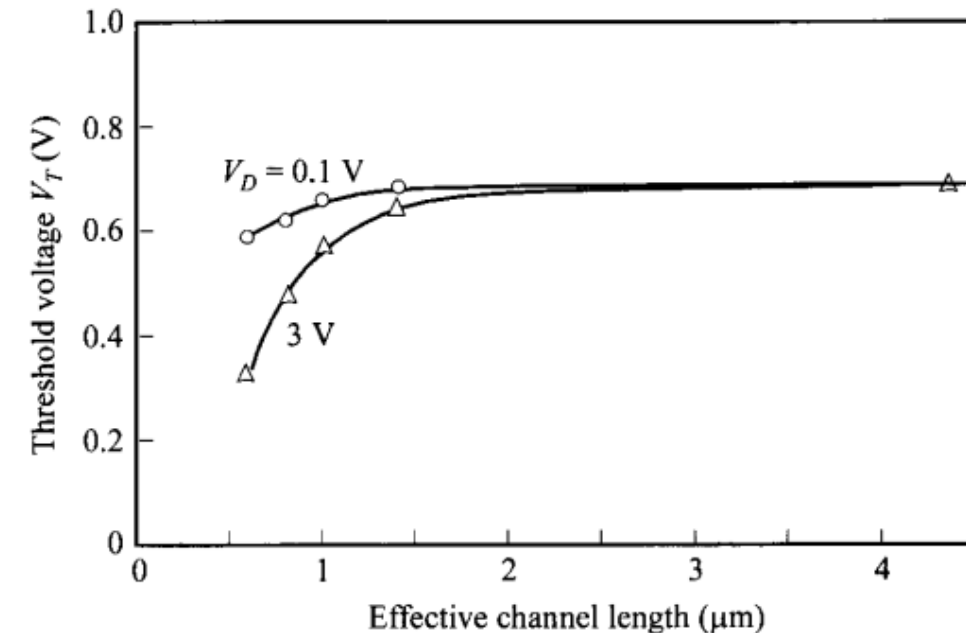
Hence $Q_D = qN_A W_{Dm}$ where W_{DM} is the width of the maximum depletion

For a very simple first order analysis:

The shift in threshold voltage to the length decreasing to L' is given by

$$\Delta V_T = -\frac{qN_A W_{Dm}}{C_{ox}} \left[1 - \frac{(L + L')}{2L} \right]$$

Since, $L + L' < 2L$, the threshold always reduces with drain bias



Channel Length Modulation

The effective channel length is reduced due to the drain depletion.

In a large channel $L \cong L'$ and hence the current remains the same.

However, in short channels, L is small and hence $L_{eff} = L' = L - y_s - y_D$

Since, there is drain dependence on the length, the current does not saturate!

The total current increases with the drain bias due to reducing effective channel length

Generally,

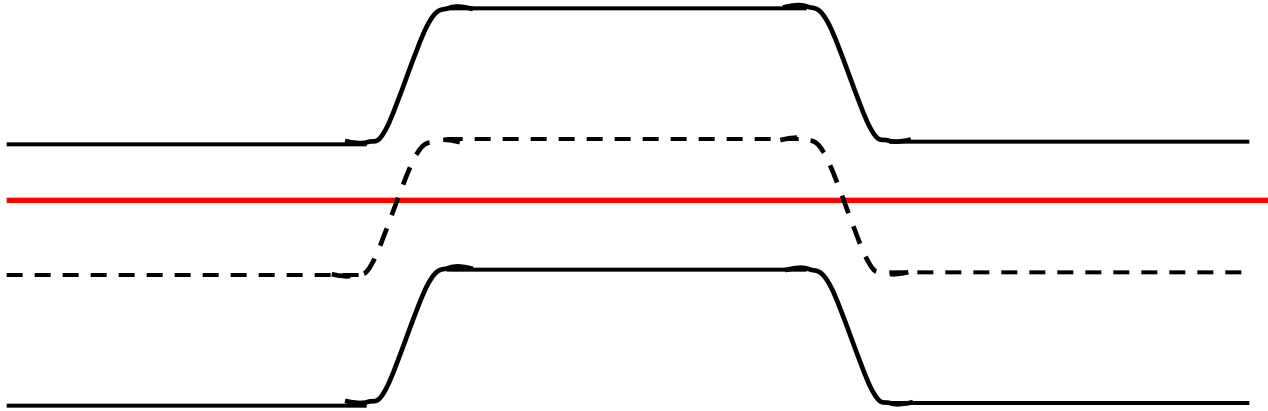
$$I_D \propto \frac{1}{L_{eff}} \propto \frac{1}{L - \Delta L} = \frac{1}{L} \left(1 + \frac{\Delta L}{L} \right)$$

Since, the dependence is on V_D , we write $\frac{\Delta L}{L} = \lambda V_D$

And the total current in saturation to be

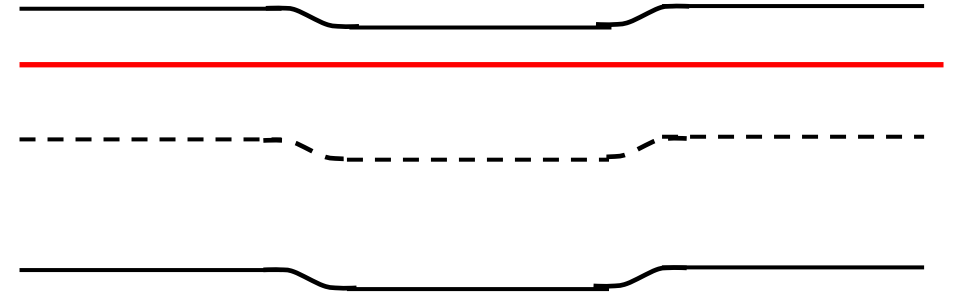
$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_G - V_T)^2 (1 + \lambda V_D)$$

Drain Induced Barrier Lowering



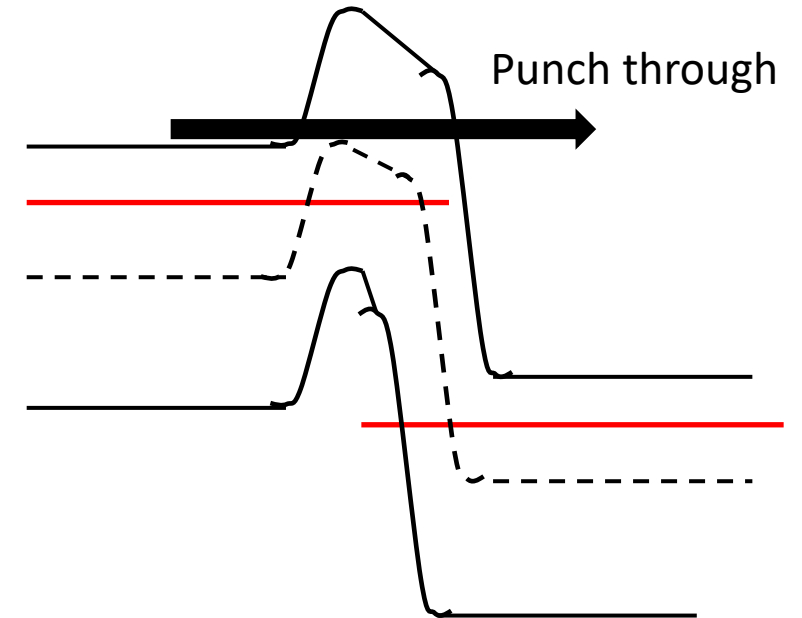
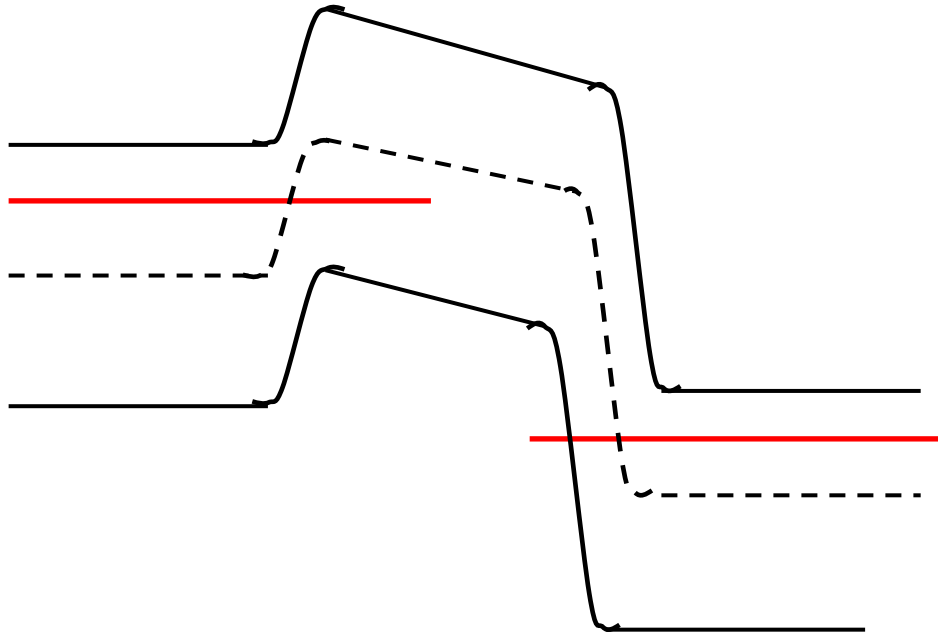
At Bulk

The bulk does not participate in the MOSFET conduction!



At surface

However, in the presence of drain bias, close to the drain diffusion



The barrier to source injection into the depletion width of the semiconductor is reduced due to drain bias

The punch through happens very close to the surface typically.

However, the substrate dopant concentration is sometimes observed to drop close to the edge of S/D diffusion

This causes the depletion width to the maximum around that region causing the punch through to happen in the bulk

Ways to reduce DIBL:

1. Source and drain diffusions should be scaled properly. Made shallow for shorter channels.
2. Channel doping must be made high to reduce the depletion width. However, this has other issues like changing the threshold voltage.
3. Sometimes, implants are made in localized regions near source/drain. These are called as Halo or pocket implants.

Multiplication and Oxide Reliability

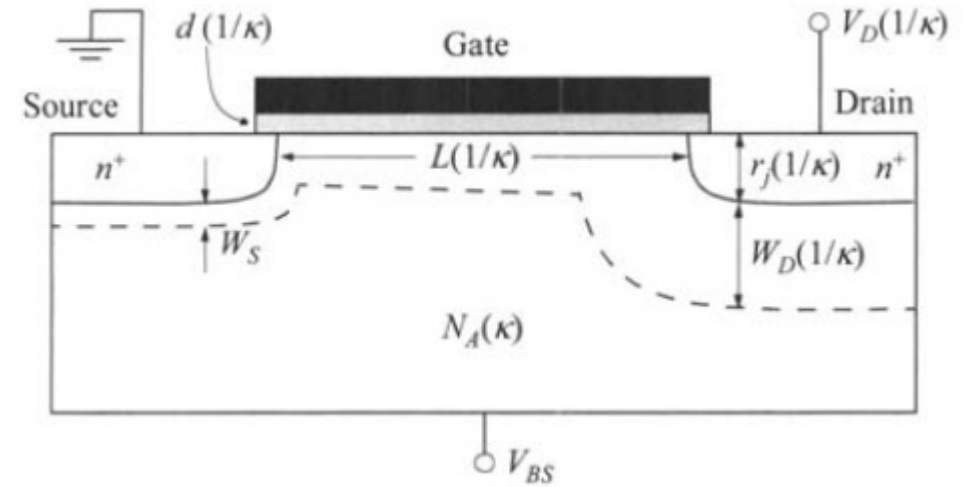
Due to nonideal device scaling, the electrons reach high field regions with excess energies (Hot carriers)

If an energy > 3.1 eV is obtained, then the electrons can cross the Si-SiO₂ barrier

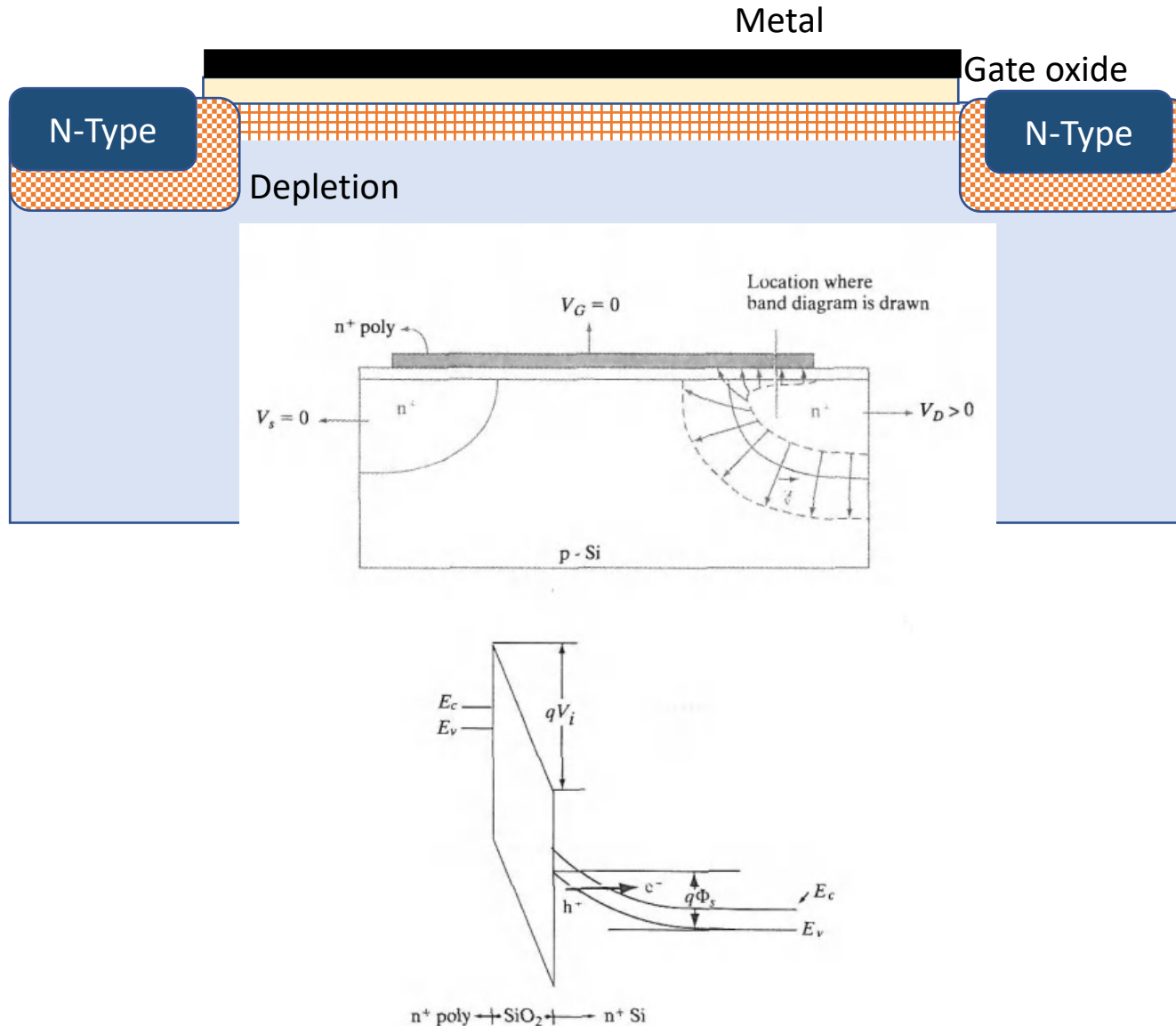
Extreme kinetic energy also leads to impact ionization – formation of e-h pairs

Electrons reach drain due to depletion field – contribute to current

Holes either reach the gate oxide/get sunk into the bulk
giving rise to I_{BS}



Gate Induced Drain Leakage



Ideal, However, never like this.

There is always a gate – drain overlap

This causes increasing drain current as the gate potential is reduced.

This is because, the Gate-Drain field is now very large.

This causes, the bands to bend significantly near the drain

This causes extra current through Gate-Drain insulator interface.

In short the short channel effects can be summarized as follows

1. Carrier velocity saturation
2. Drain induced barrier lowering
3. Gate leakage
4. Degradation of sub-threshold swing and threshold lowering
5. Punch-through
6. Hot carrier effects

Typically employed solutions:

1. Doping the channel material stronger
2. Strained Si channel for larger mobility
3. High-K dielectric for thicker effective oxide (same capacitance)
4. Use of polysilicon gate to have smaller flat band potential (for smaller V_T)

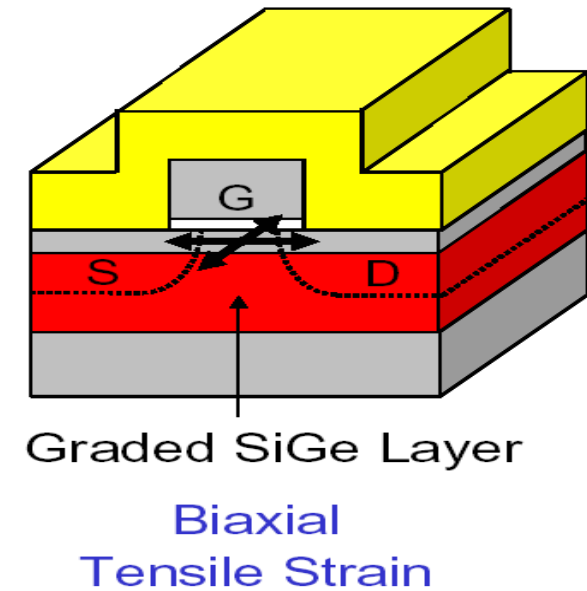
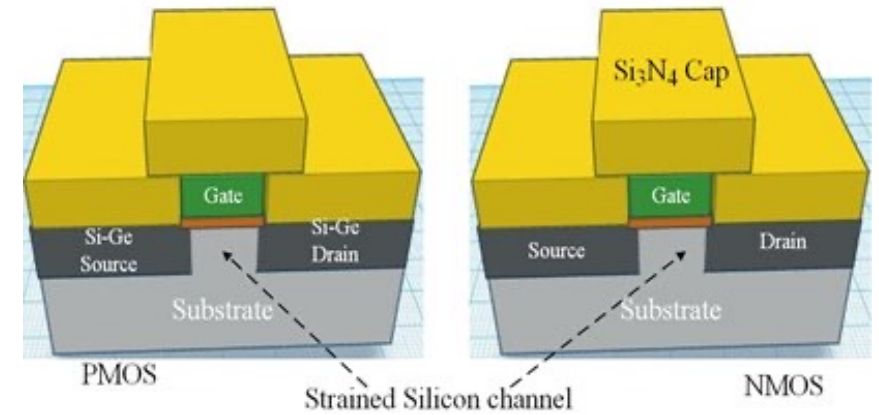
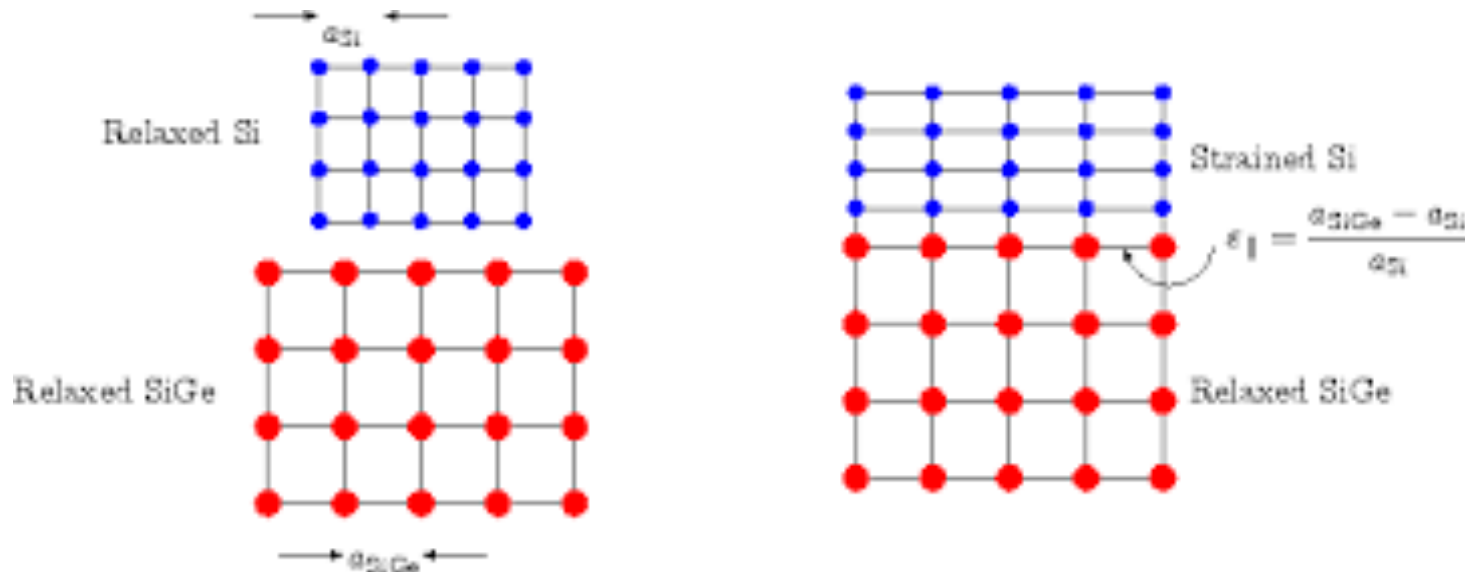
The bottom line is to improve the gate control on the channel
In other words, higher gate capacitance is required!

Germanium atom size is larger than Si.

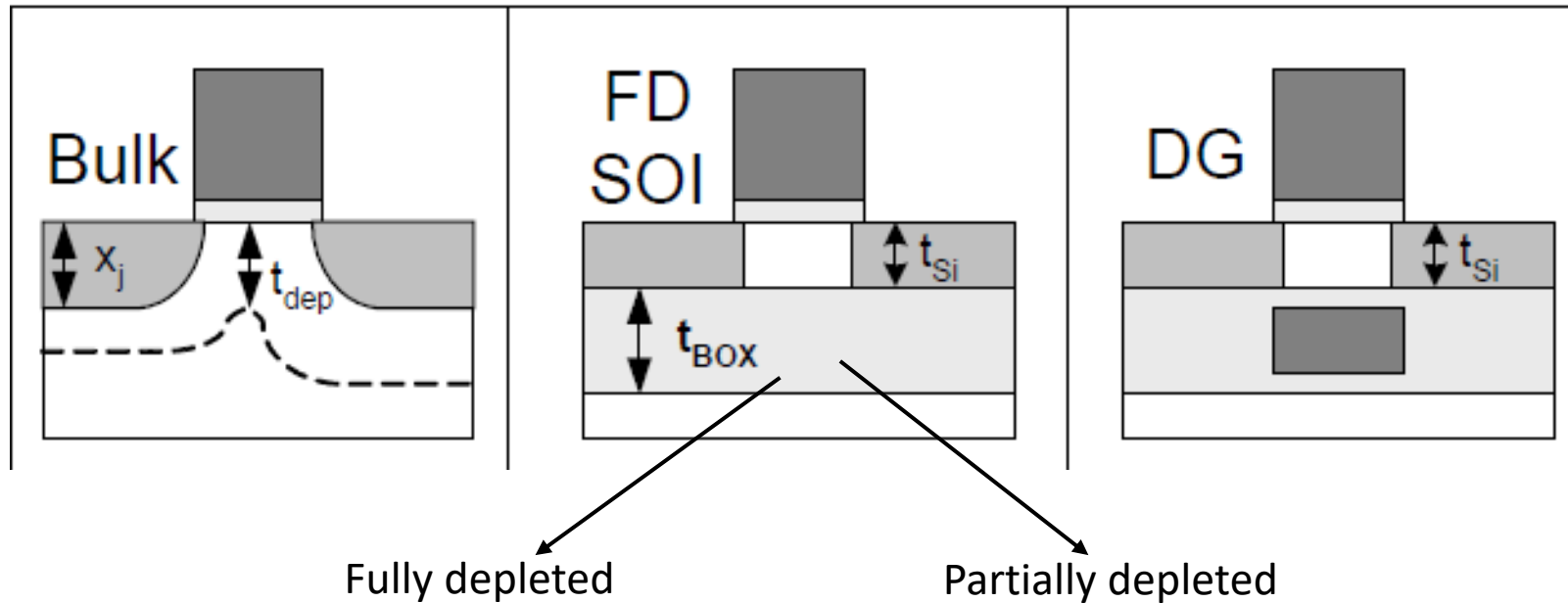
Introduction of Ge into Silicon lattice causes strain in the near-by atoms

Si-Ge (of about 20% Ge) on either sides of Si compressively strains the nearby layer

Si layer grown over Si-Ge layer makes it tensile strained.



How can we improve the gate coupling with the channel ?



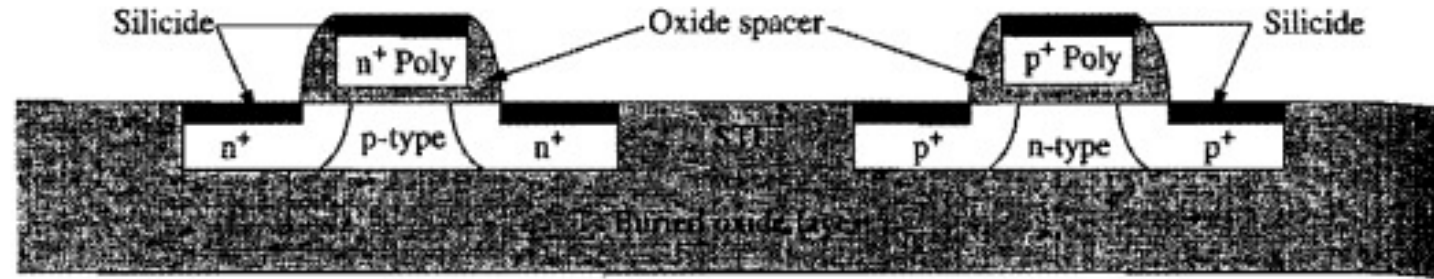
Double gate –
both gate tied
together
1989 Sekigawa
and Hayashi

Bottom gate
takes in the
effect of source
and drain

As the length of the device is reduced, to improve speed, power and packing density,
The gate control over the body becomes increasingly weak.

The source and drain effect on the body can only be reduced by decreasing the body thickness.

Silicon-on-Insulator (SOI) was introduced to improve gate coupling.



Inherent advantages of SOI over Bulk Si

1. Very low junction capacitance

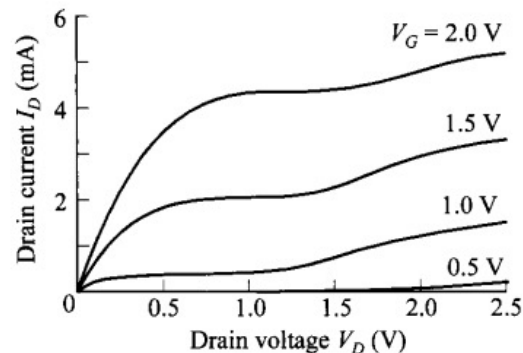
Source and drain capacitances are absent, Cap through buried oxide is too small

2. No body effect

Body is not grounded/tied to any potential. Body takes the potential of source, lesser depletion

3. Soft error immunity

The volume susceptible to ionizing radiations is small

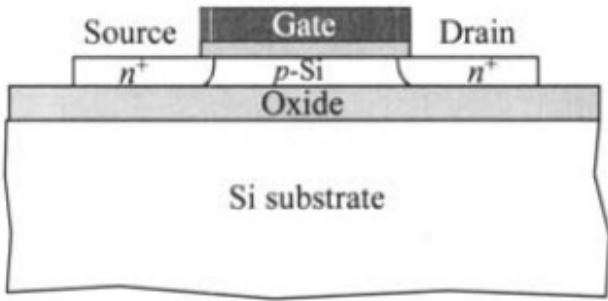


However, the floating body is known to have the Drain-Current overshoot: Body potential rising with the gate, causing V_T reduction

Floating body has history effects: How long the device has been on

Floating body also called as Kink effect due to the output characters

Fully Depleted SOI MOSFET



The body is lightly doped or truncated such that there are no neutral regions.

The body is fully depleted even before the onset of threshold.

Displays ideal sub-threshold swing (60 mV/Decade)

V_T can now be lower, lower capacitances allow faster speed of operation

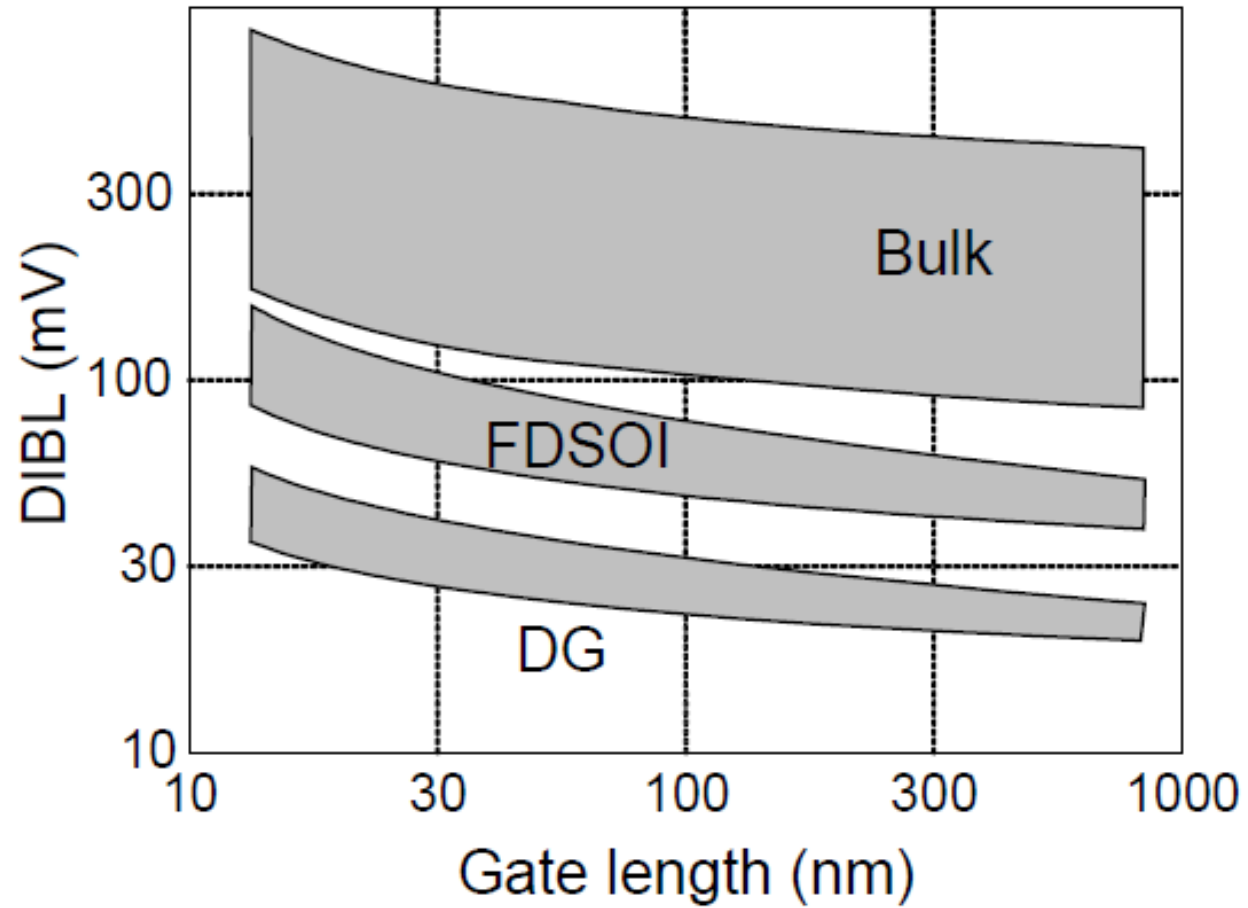
S is ideal for fully depleted MOS because,

$$I_{ds} \propto e^{\frac{q\psi_s}{KT}}$$
$$\psi_s = \frac{V_G}{1 + \frac{C_{si}}{C_{ox}}}$$

If $C_{si} \ll C_{ox}$ We get the almost purely exponential behavior with the Boltzmann factor (Ideal S)

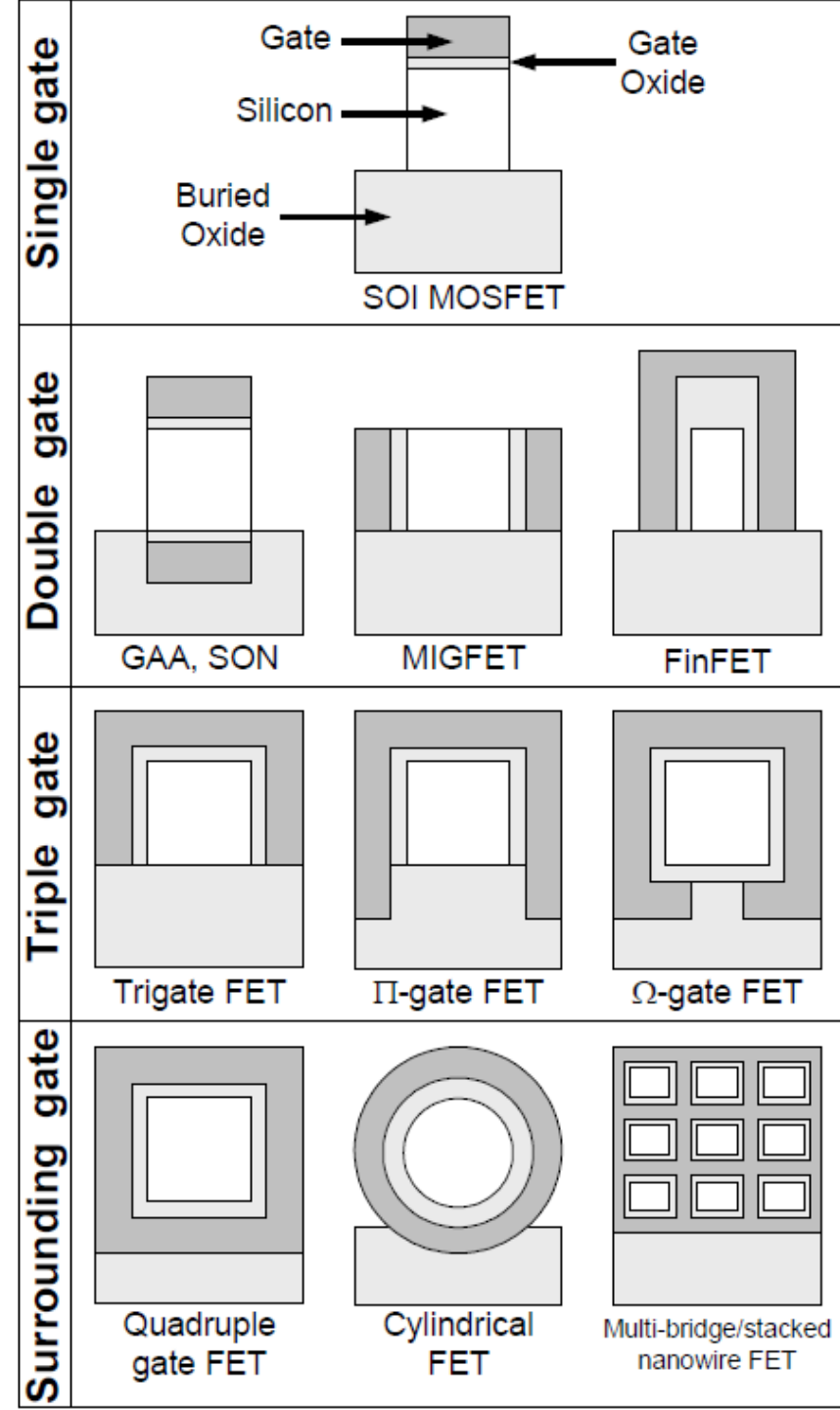
Downside: The depleted body gives you strong short channel effects. There is band bending in the body giving you DIBL

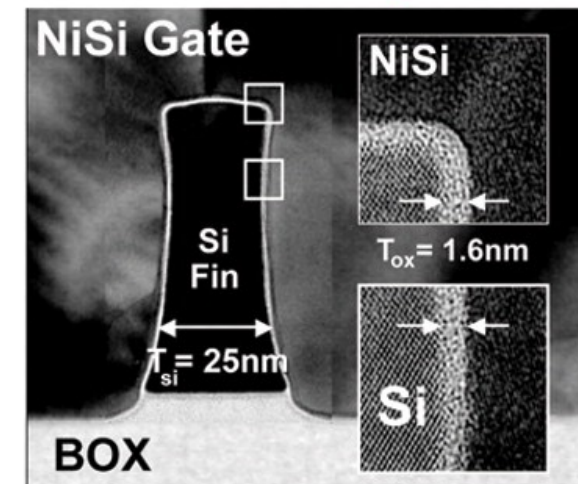
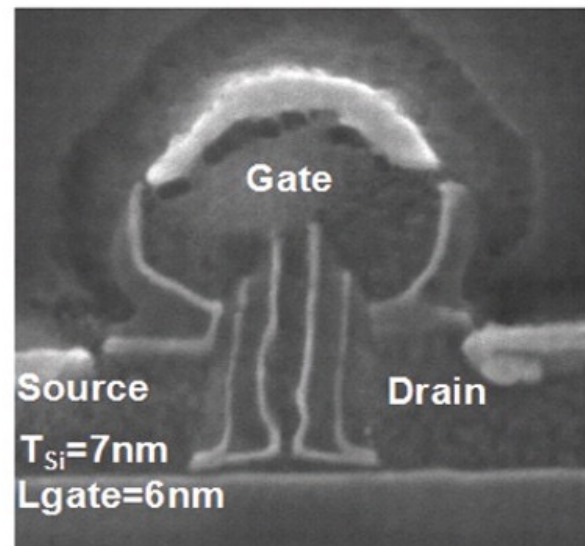
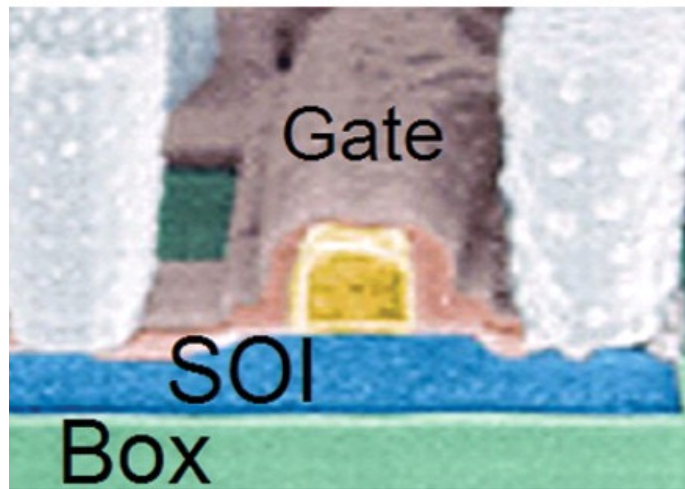
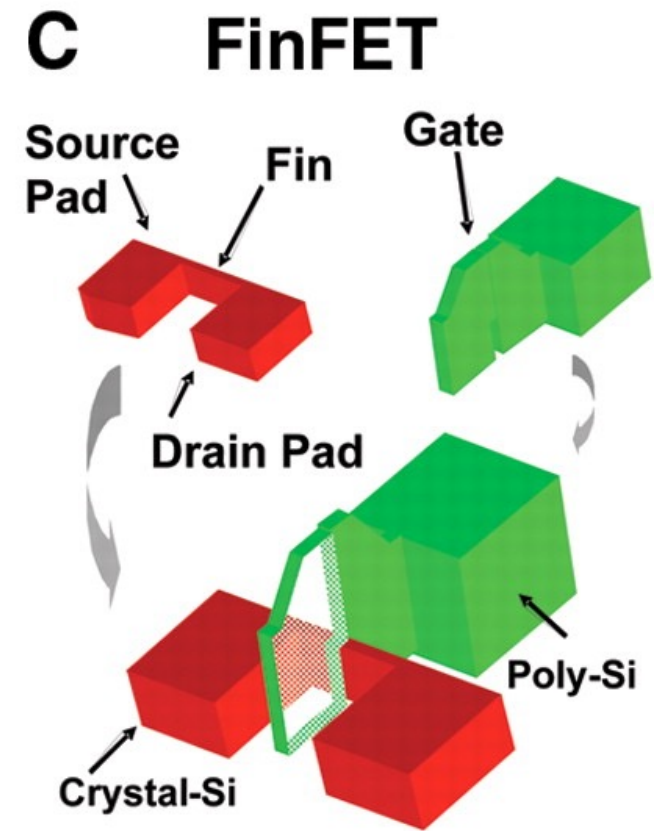
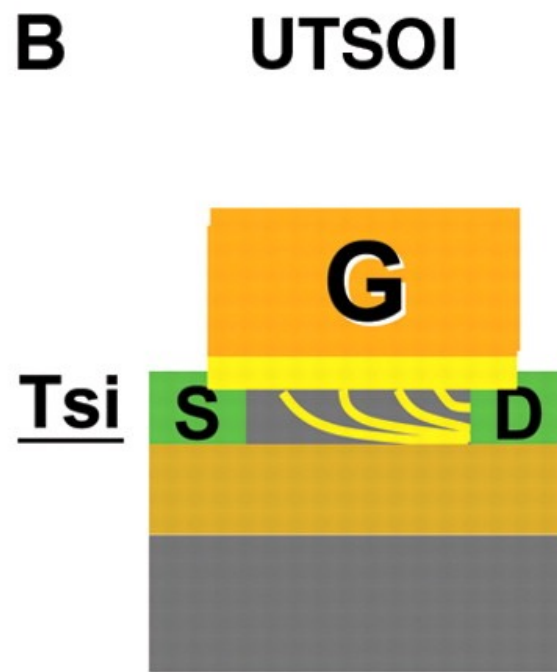
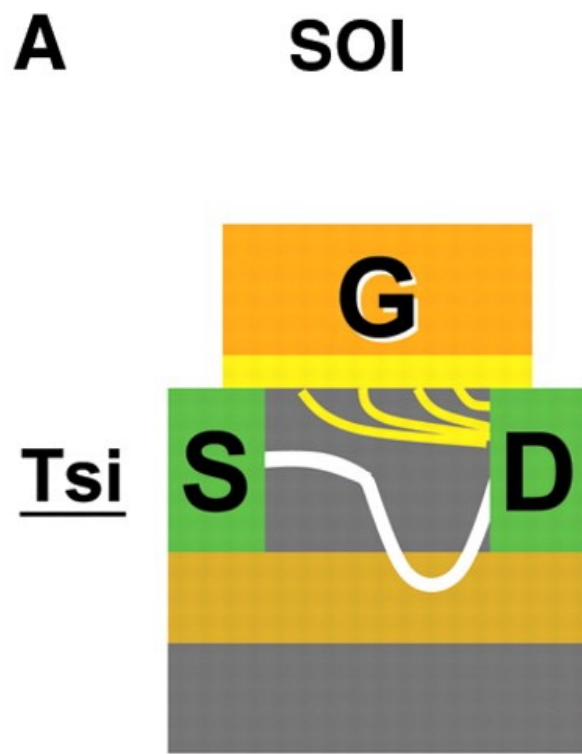
DIBL in various device architectures with the gate length



In FDSOI and in Double gate transistors, the Drain field gets terminated either by the ground planes below the buried oxide or the gate electrode. This makes the band bending in the channel to be small and thus reduce the DIBL effect.

Acronym	Also known as
MuGFET (Multiple-Gate FET)	Multi-gate FET, Multigate FET
MIGFET (Multiple Independent Gate FET)	Four-terminal (4T) FinFET
Triple-gate FET	Trigate FET
Quadruple-gate FET	Wrapped-Around Gate FET Gate-All-Around FET Surrounding-Gate FET
FinFET	DELTA (fully DEpleted Lean channel TrAnsistor)
FDSOI (Fully Depleted SOI)	Depleted Silicon Substrate
PDSOI (Partially depleted SOI)	Non-Fully Depleted SOI
Volume Inversion	Bulk Inversion
DTMOS (Dual Threshold Voltage MOS)	VTMOS (Varied Threshold MOS) MTCMOS (Multiple Threshold CMOS) VCBM (Voltage-Controlled Bipolar MOS) Hybrid Bipolar-MOS Device



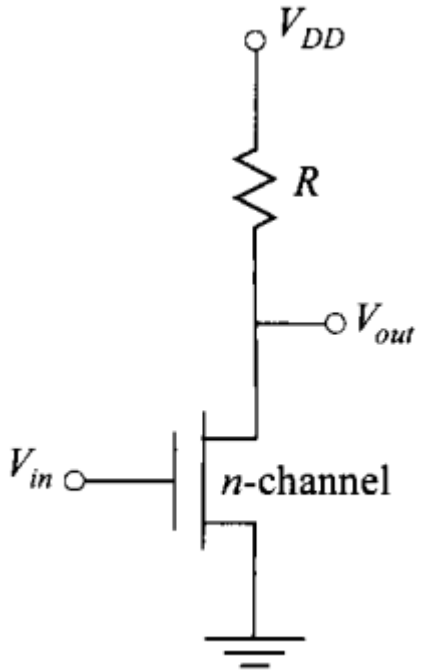


Circuits with MOSFET

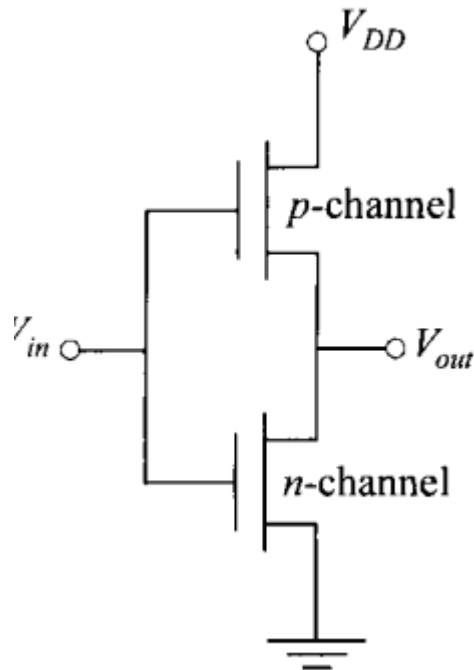
Lets look at an inverter-

Its like a switch, which you toggle: Turn on if its off, turn off if its on.

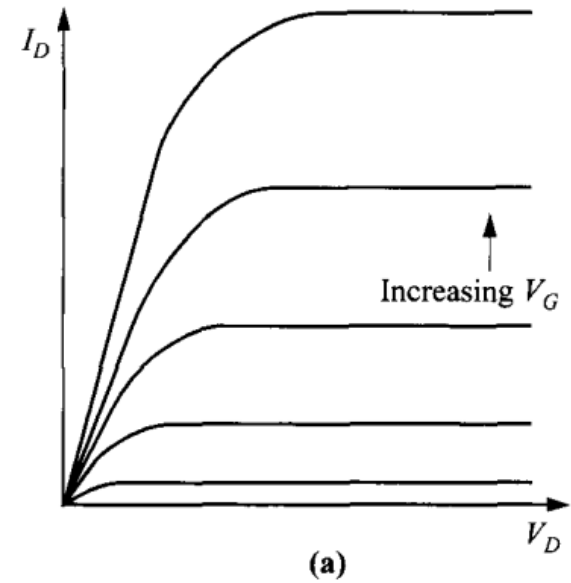
Many ways to implement it, but the most common ways are



N-MOS design



Complementary CMOS design

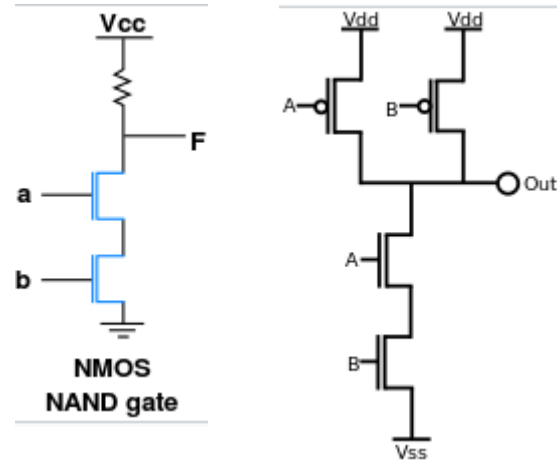


We take the input potential to be logic '1' if the potential is same as the supply potential V_{DD}

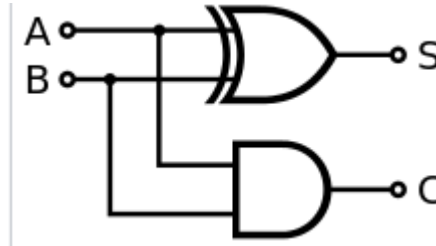
And logic '0' if the potential of any node is closer to ground.

This is the origin of binary logic, with which we do computation, communication and storage.

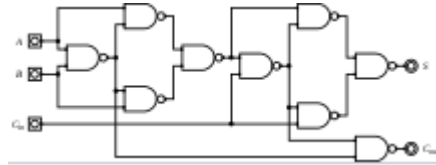
NAND Gate



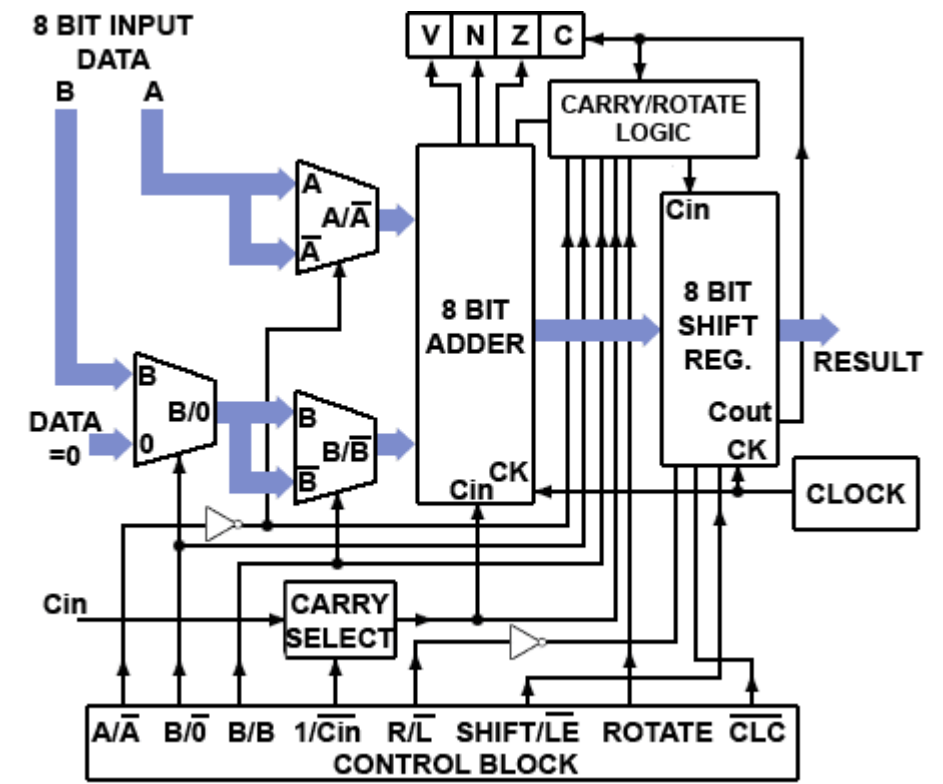
Half adder



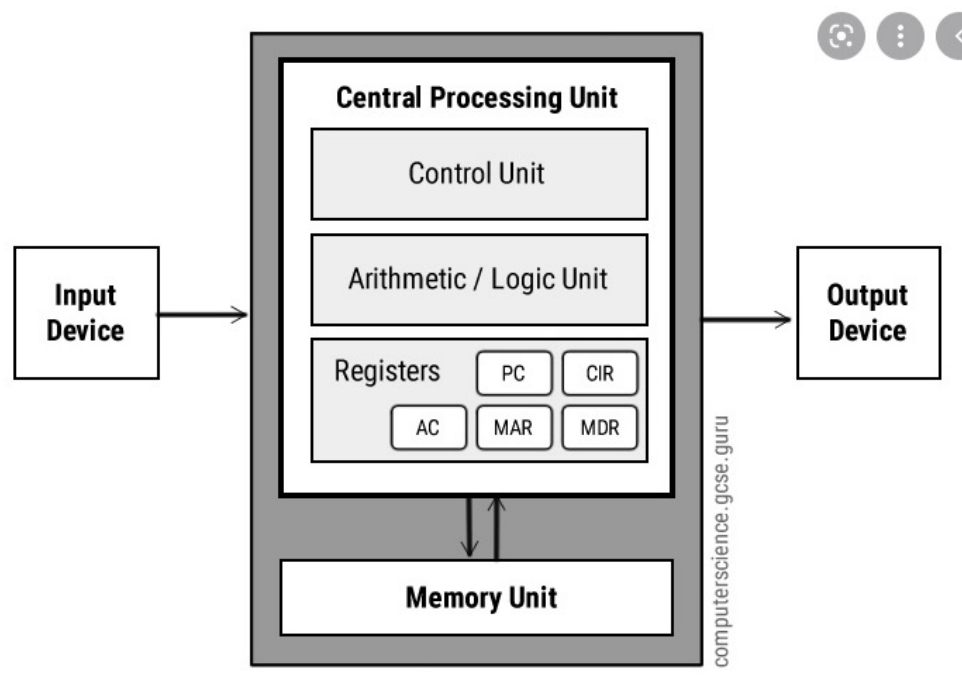
NAND Half Adder



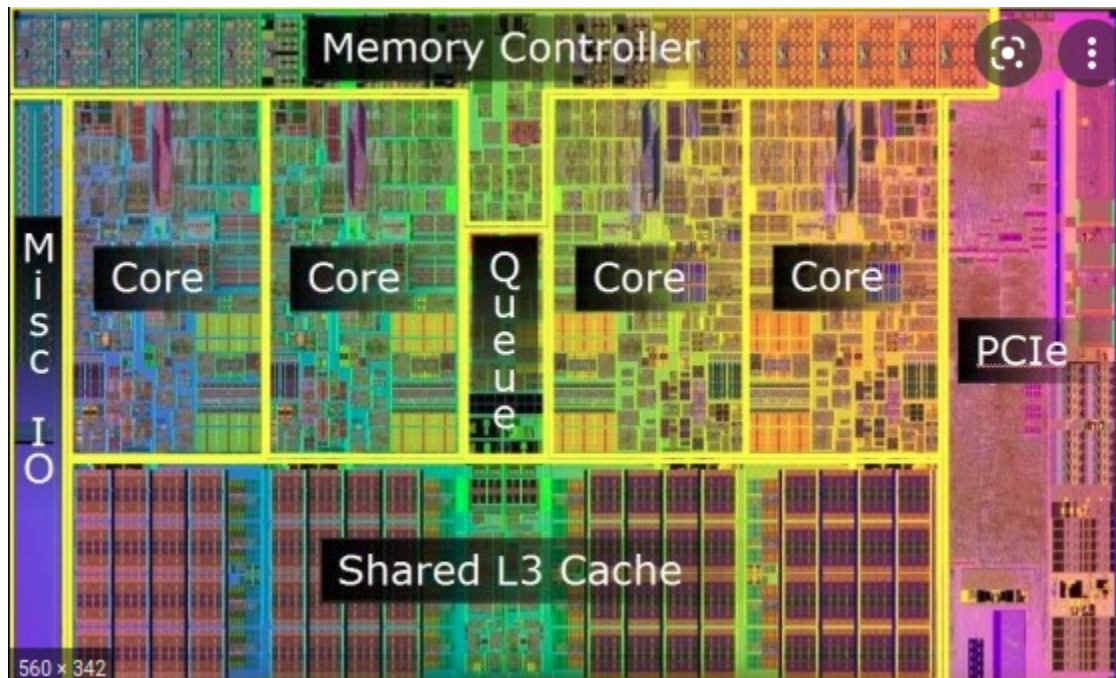
Example Arithmetic and Logic Unit



Simplified processor schematics



Intel I7 Quad Core



Apple M1

