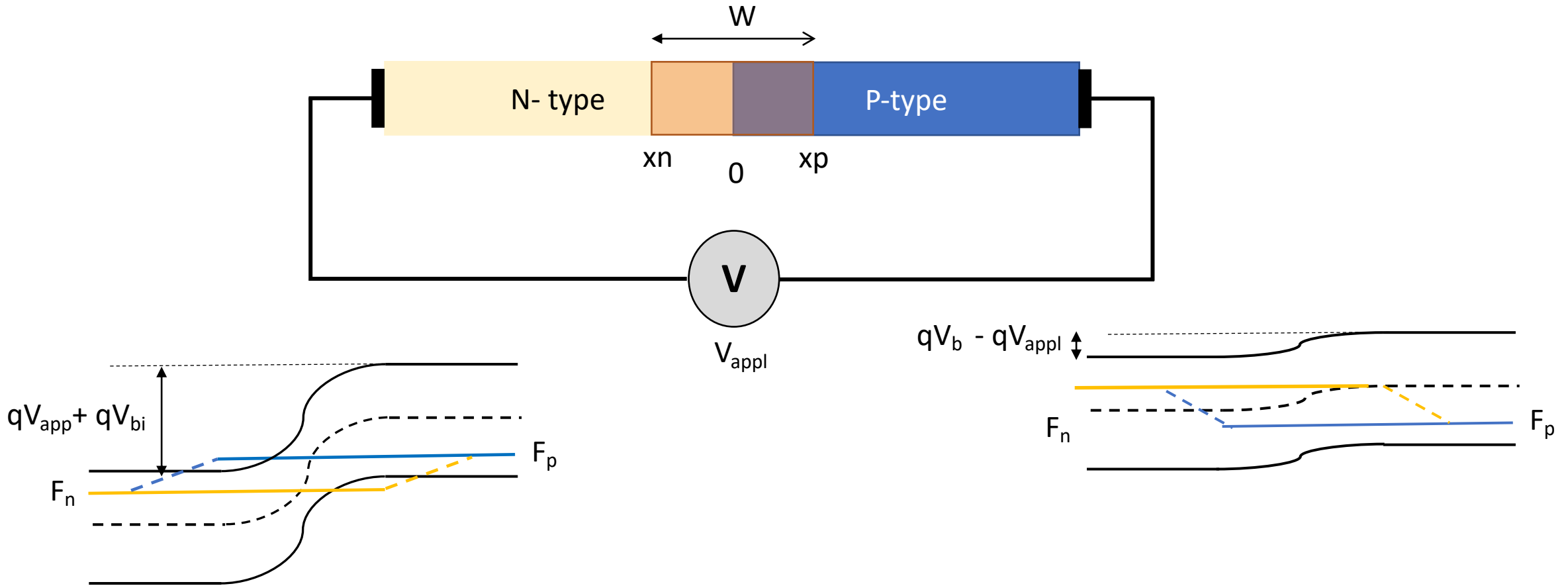


Assumption 1: There is no potential drop in the neutral regions, contacts

What happens in the presence of bias:

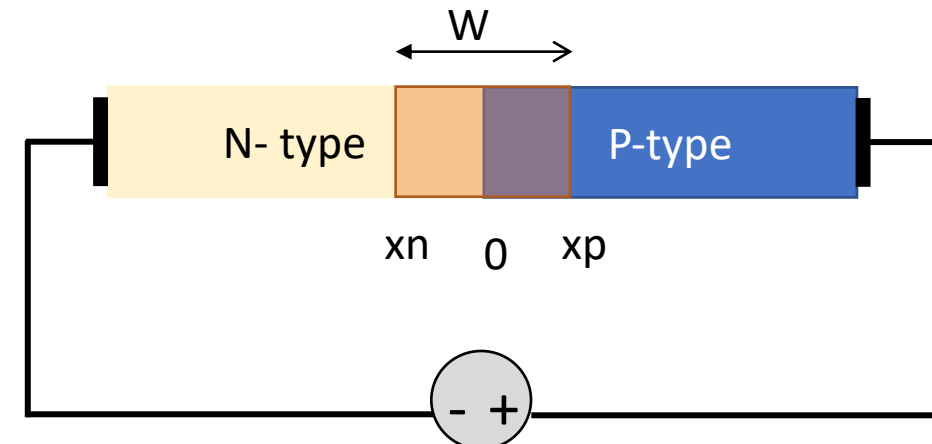
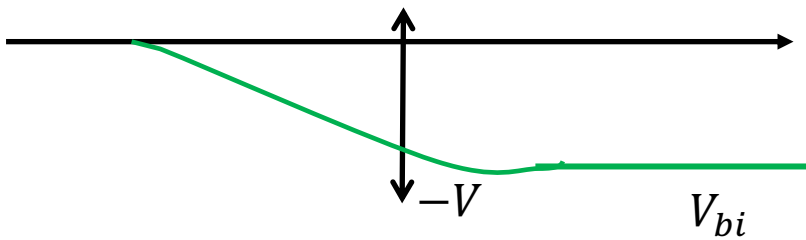
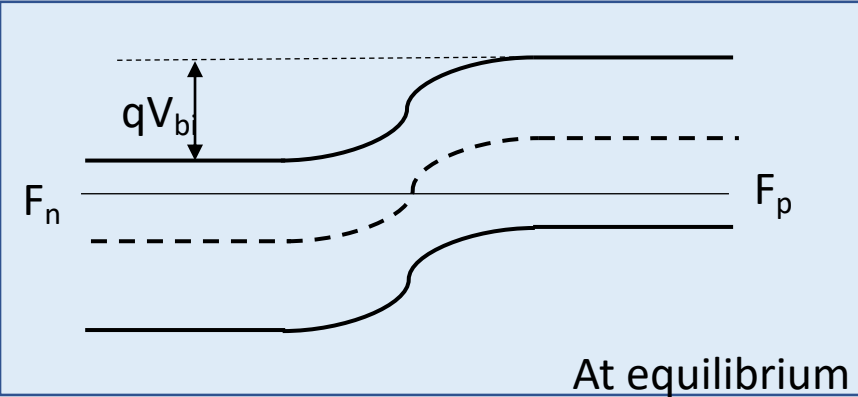


Remember at equilibrium, the drift and diffusion currents of electrons and holes are equal and opposite.

This leads to net zero current.

When a potential bias is applied, this balance is affected.

Connecting positive potential to P-Type

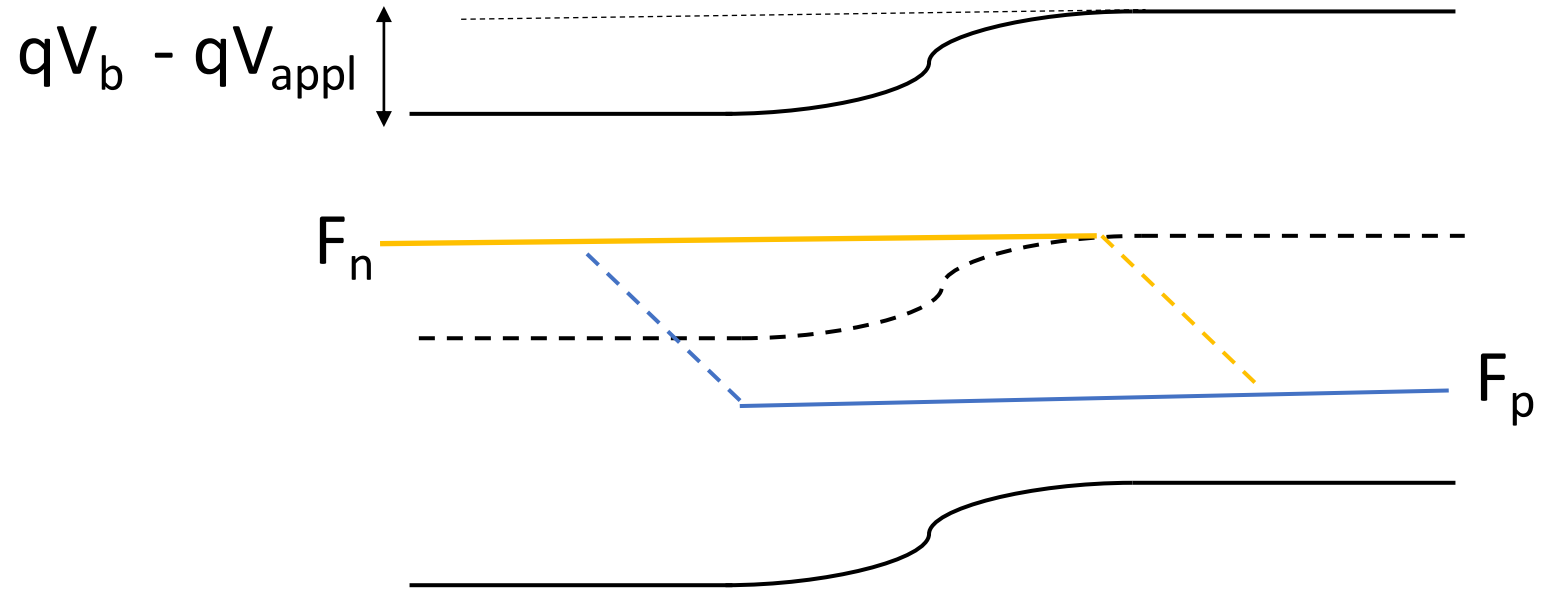


The built-in potential is such that the p-side is at a negative potential in comparison to n-type.

If positive potential terminal is connected to P type, The potential is set to off-set the built-in bias potential.

The potential barrier to the carrier transport is reduced!!

The Drift current, which compensated the diffusion is reduced. This leads to a net-diffusion current in a forward biased PN junction.



Diffusion under bias

Looking at holes:

Density of holes in the ptype: $p_p = n_i e^{(E_i - F_p)/KT}$

Density of holes in the ntype: $p_n = n_i e^{(E_i - F_n)/KT}$

$$\frac{p_p}{p_n} = e^{\frac{F_p - F_n}{KT}} = e^{q(V_{bi} - V_{appl})/KT}$$

At equilibrium

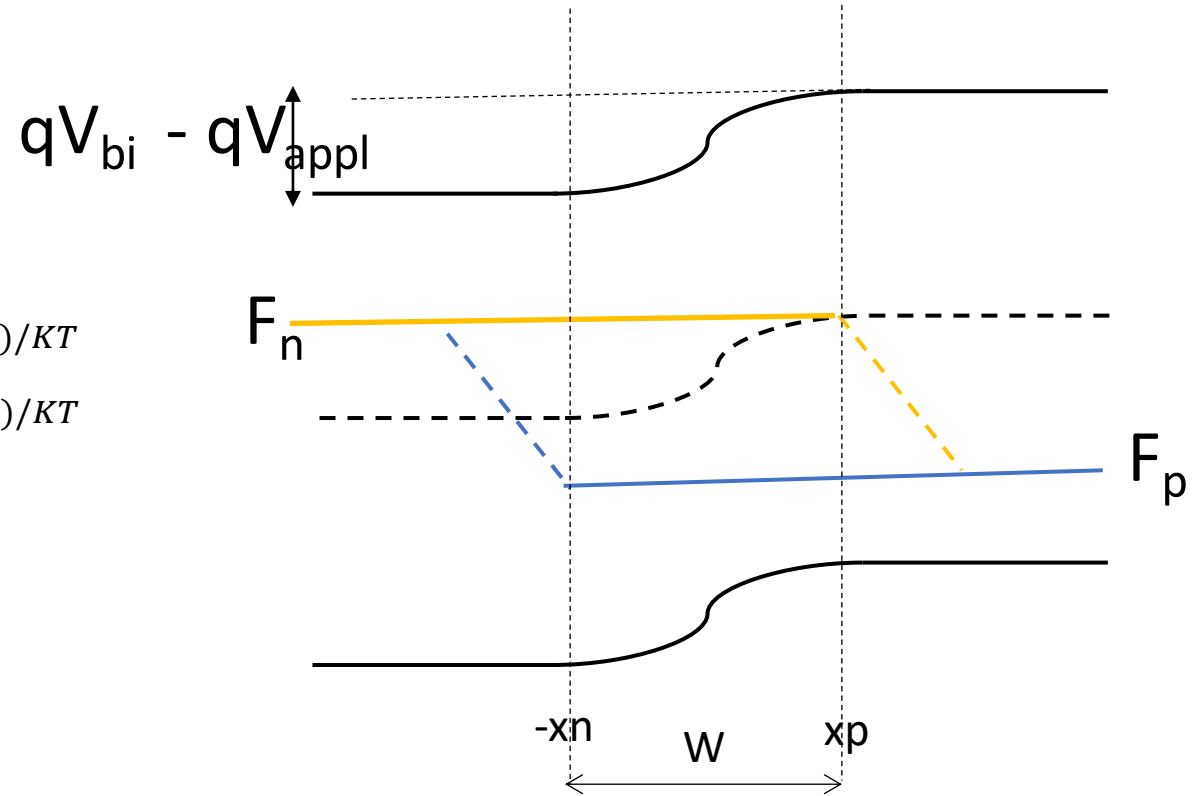
$$\frac{p_p^0}{p_n^0} = e^{q(V_{bi})/KT}$$

The Fermi level, intrinsic levels do not change till the edge of the depletion width

We assume the majority carriers do not change significantly: $p_p^0 = p_p$

$$\frac{p_n^0 e^{q(V_{bi})/KT}}{p_{(-xn)}} = e^{q(V_{bi} - V_{appl})/KT}$$

$$\frac{p_{(-xn)}}{p_n^0} = e^{qV_{appl}/KT}$$



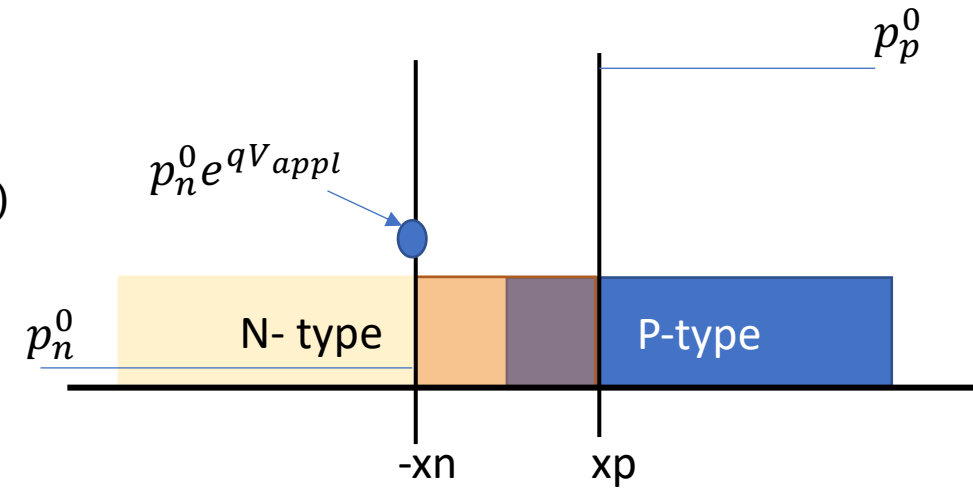
Excess carrier density at the edge of the depletion width is exponential of applied bias

Excess holes at the edge of n-type:

$$\Delta p(-x_n) = p_n(-x_n) - p_n^0 = p_n^0(e^{qV_{appl}} - 1)$$

Excess electrons at the edge of p-type:

$$\Delta n(x_p) = n_p(x_p) - n_p^0 = n_p^0(e^{qV_{appl}} - 1)$$

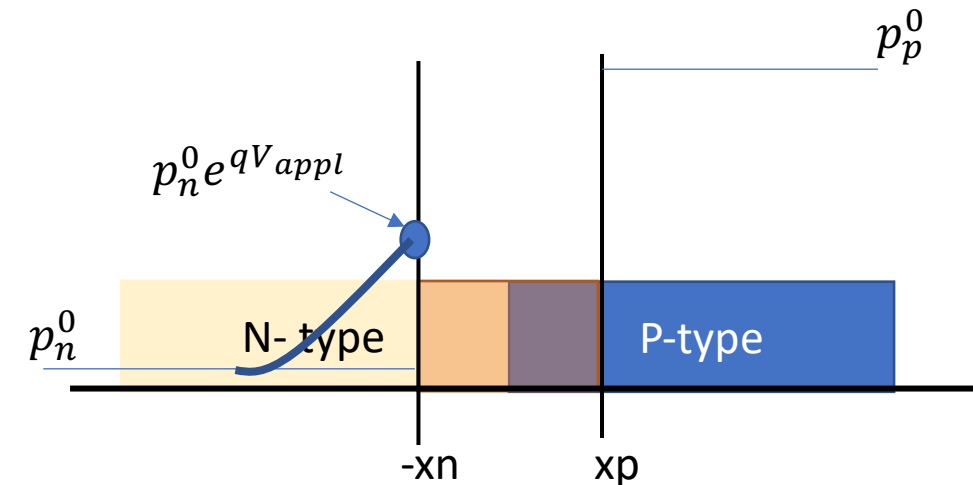


Once, we know the steady state injection rate of the minority carriers, we know the distribution shape.

$$\Delta p(x) = p_n^0(e^{qV_{appl}} - 1)e^{-\frac{x+x_n}{L_p}}$$

Where L_p is the diffusion length of holes in N-type

$$\text{Hole current } J_p = -qD_p \frac{dp_n}{dx} \Big|_{-x_n} = \frac{qD_p p_n^0}{L_p} \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$



On similar lines,

$$\text{Electron current } J_n(x) = qD_n \frac{dn_p(x)}{dx} \Big|_{xp} = \frac{qD_n n_p^0}{L_n} \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$

The individual current components are spatially variable.

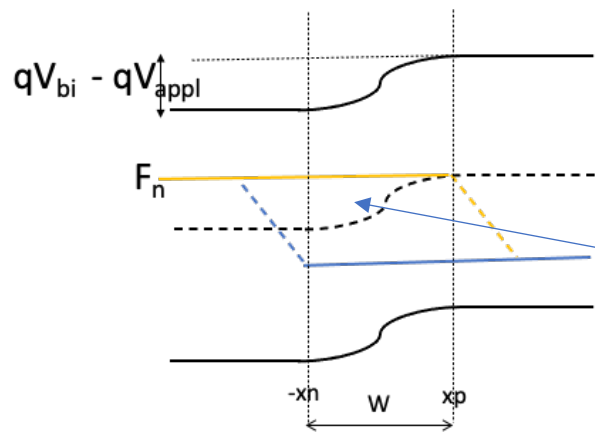
Total current is the summation of both the currents

Shockley Equation
Ideal diode equation

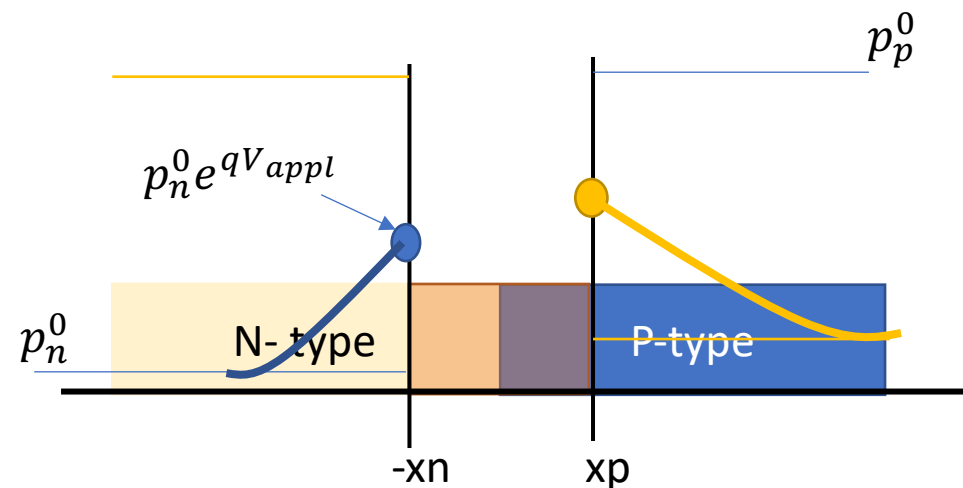
$$J = J_n + J_p = J_0 \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$

$$\text{Where, } J_0 = \frac{qD_p p_n^0}{L_p} + \frac{qD_n n_p^0}{L_n}$$

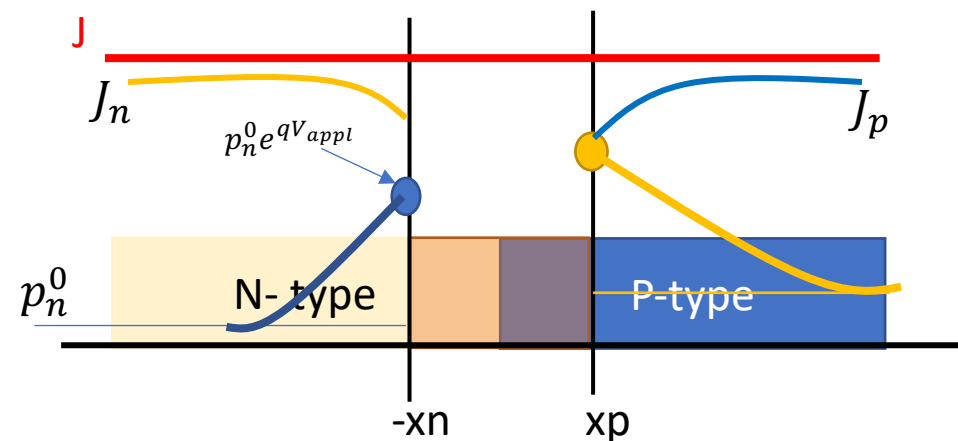
The total current has no spatial dependence



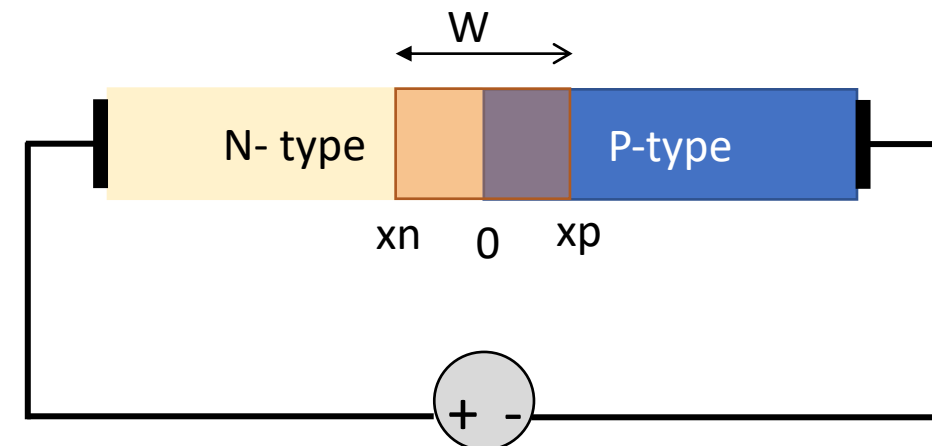
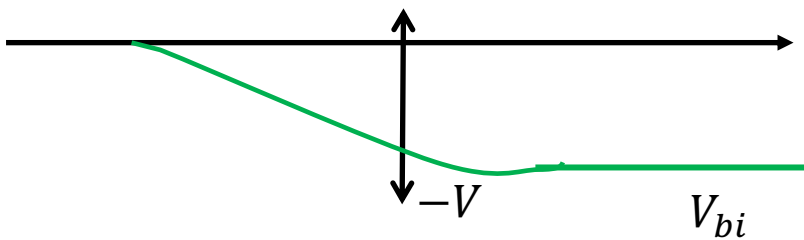
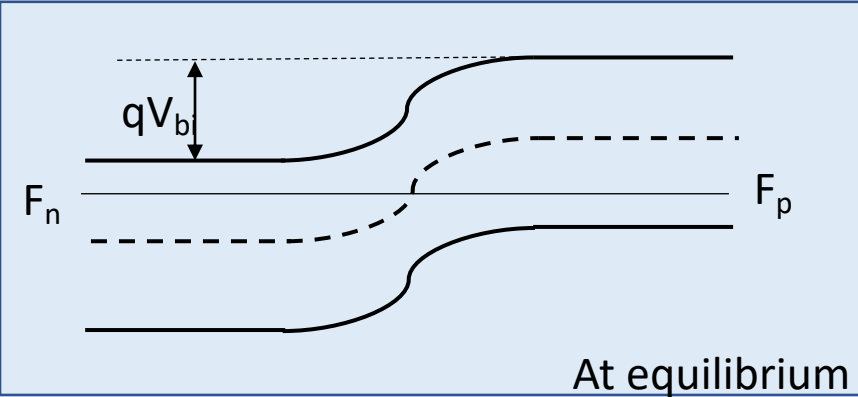
Why is the Quasi-Fermi levels flat in the depletion width ?



Current contributions



So what happens when you connect P-side to negative potential



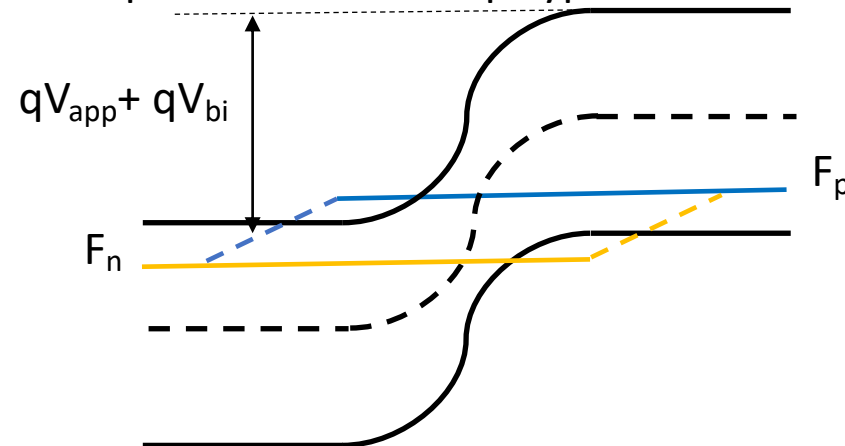
The built-in potential is such that the p-side is at a negative potential in comparison to n-type.

If negative potential terminal is connected to P type, The applied potential adds on to the built-in potential.

The potential barrier to the carrier transport is enhanced!!

The diffusion current, which compensated the drift is reduced. This leads to a net-drift current in a reverse biased PN junction.

However, the drift current is very small because of lack of carriers. No electrons are present in the the p-type material to be drifted.



The equations are sign insensitive.

$$\text{Electron current } J_n(x) = qD_n \frac{dn_p(x)}{dx} \Big|_{xp} = \frac{qD_n n_p^0}{L_n} \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$

The individual current components are spatially variable.

Total current is the summation of both the currents

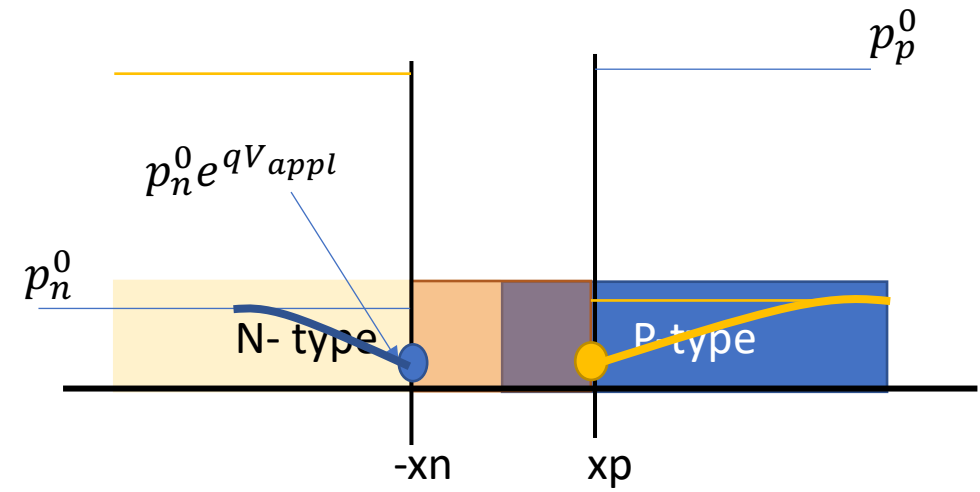
$$J = J_n + J_p = J_0 \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$

$$\text{Where, } J_0 = \frac{qD_p p_n^0}{L_p} + \frac{qD_n n_p^0}{L_n}$$

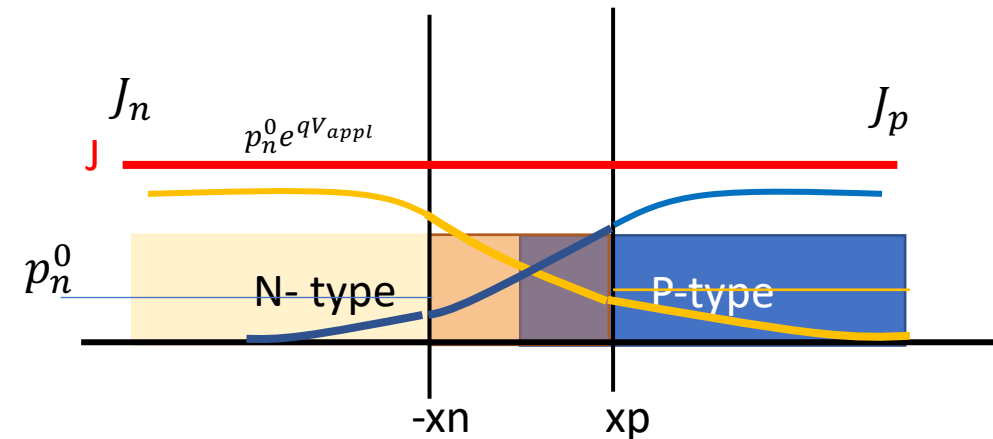
Current is mostly taken by the drift component

Drift is strongly controlled by the field and the density. There is excess field in the region, but the charge density is the bottle neck.

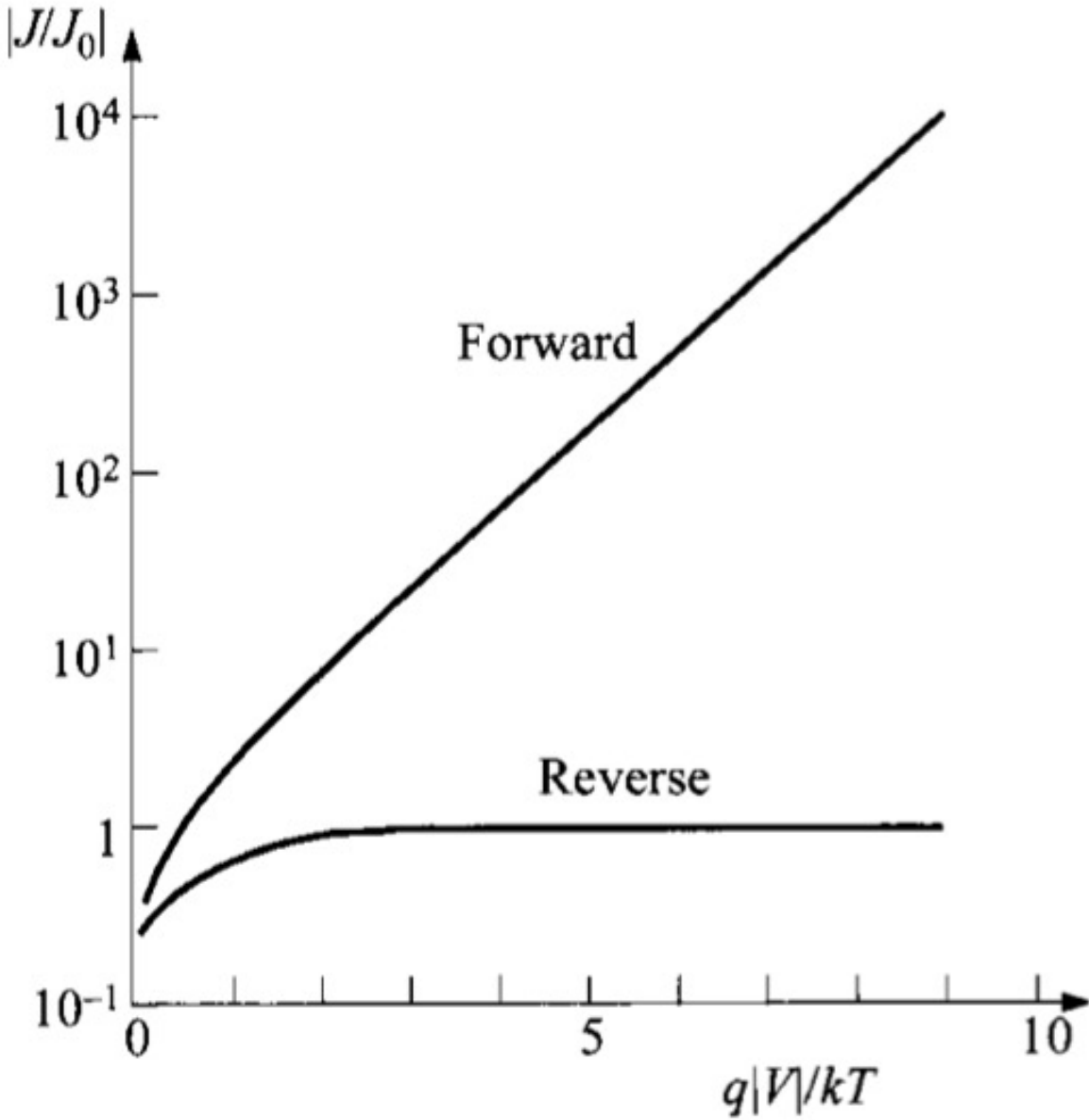
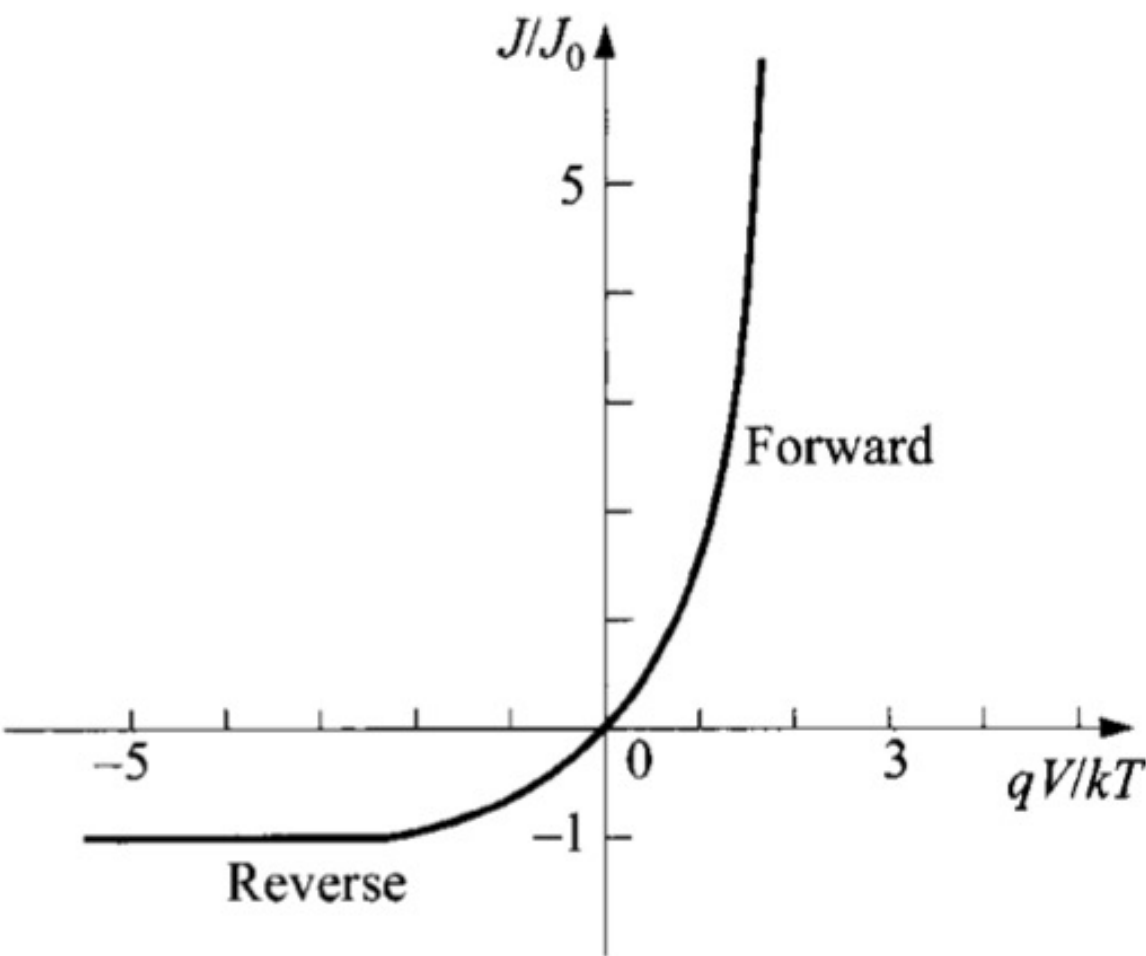
Thermally generated carriers control the reverse bias current density.



Current contributions



Ideal Diode characteristics



Diode currents

In the forward direction, the current rises constantly at about 60 mv/decade at 300 K. (Boltzmann tyranny)

On the reverse side, the current saturates at J_0 also called as reverse saturation current

$$J = \left[\frac{qD_p p_n^0}{L_p} + \frac{qD_n n_p^0}{L_n} \right] \left[e^{\frac{qV_{appl}}{KT}} - 1 \right]$$

Lets take an example of a diode with heavy P-doping in comparison with N-doping.
Such as diode is called as P⁺-N diode.

For such a diode, $p_n^0 \gg n_p^0$

$$\text{Therefore } J_0 \cong \frac{qD_p p_n^0}{L_p} = q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} \cong T^{\frac{\gamma}{2}} [T^3 e^{-\frac{E_G}{KT}}]$$

Non Idealities

Shockley equations describes well a Ge diode IV characteristics, but not much Si and GaAs diodes. This is because of non ideal characteristics

What were ignored:

1. Generation and recombination in the depletion width
2. The majority carriers were shown to be close to equilibrium – ignoring high injection
3. No potential drop in the neutral region
4. Tunneling between the bands
5. Surface effects.
6. Junction breakdown

Generation and Recombination

Consider the reverse bias situation.

The carrier density in the depletion width is far from the equilibrium condition.

$$np \ll n_i^2$$

This will lead to generation of carriers in the depletion width.

A generation rate U is given by

$$U = \frac{n_i}{\tau_g}$$

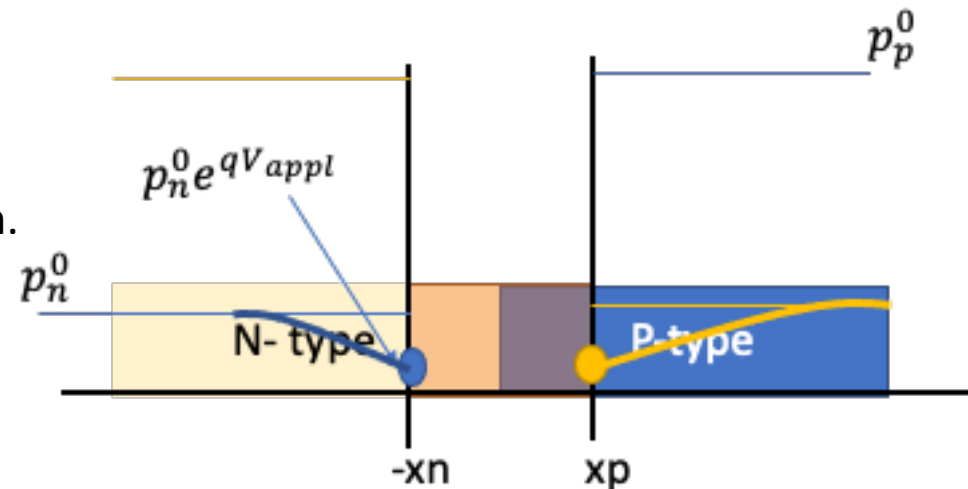
In the units of per cm³ per second.

The net additional current due to the generation is given by

$$J_R = \int_{-x_n}^{x_p} qUdx = \frac{qn_iW}{\tau_g}$$

Thus additional current is observed in reverse bias due to generation.

$$J_0 = q \sqrt{\frac{D_p}{\tau_p} \frac{n_i^2}{N_D}} + \frac{qn_iW}{\tau_g}$$



For materials like Ge with large n_i , generation do not contribute strongly.

For other materials, the generation current alters the response from the ideal diode behavior

In forward bias:

In addition to the diffusion current, there is recombination in the depletion width.

This is because, $n * p \gg n_i^2$ in the depletion width.

Similar to the previous case, a recombination rate is proportional to excess

$$U \propto (np - n_i^2)$$

On the p side, in forward bias $n_p = n_p^0 + \Delta n_p$

$$U \propto \Delta n_p \propto n_i e^{\frac{qV_{appl}}{2KT}}$$

$$\text{The forward current } J_{FR} = \int_{-x_n}^{x_p} qU dx = e^{\frac{qV_{appl}}{2KT}}$$

$$\text{Total current } J_F = J_0 \left[e^{\frac{qV_{appl}}{\eta KT}} - 1 \right]$$

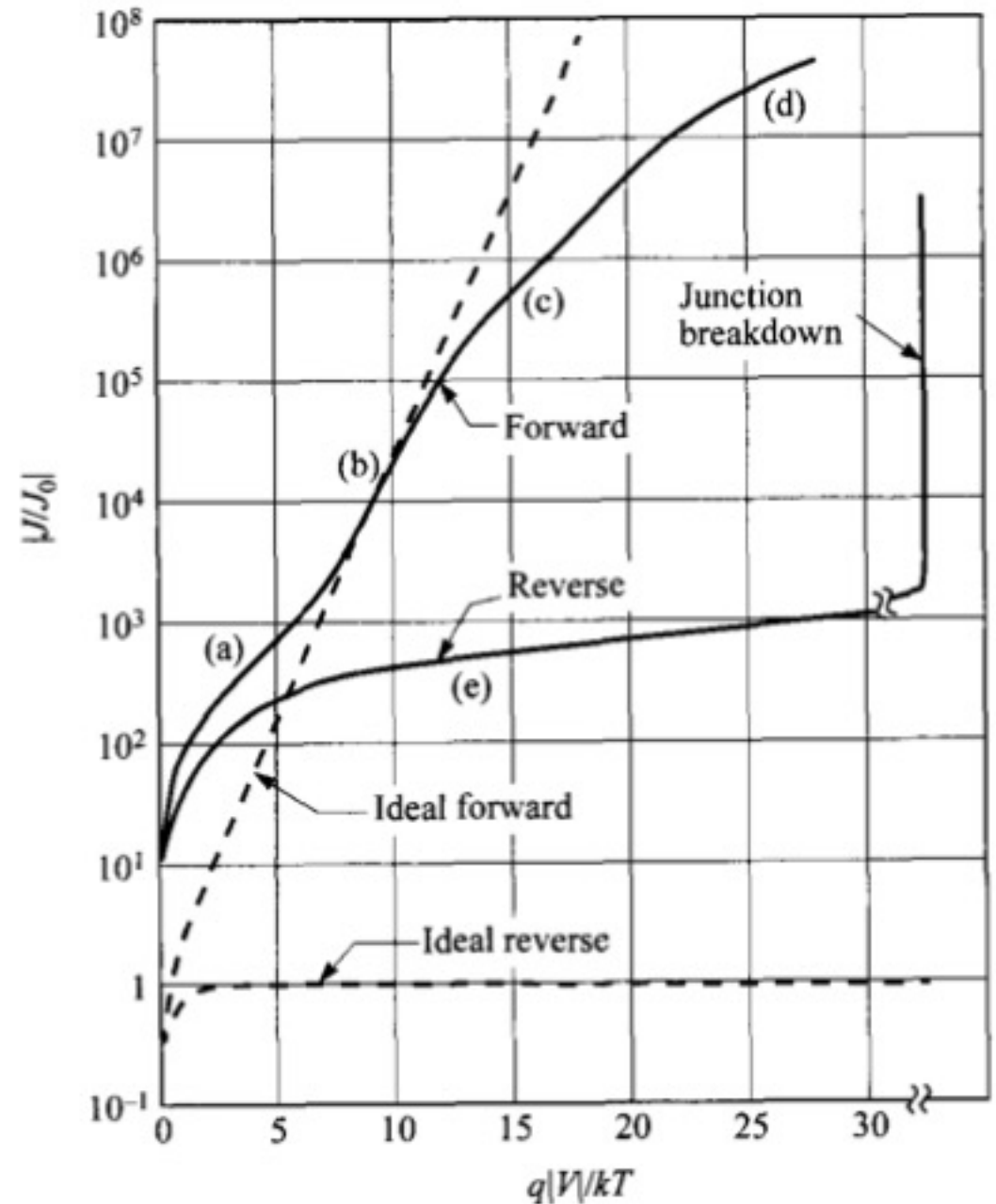
η close to 1 is ideal diode

η close to 2 has lot of recombination

Additional currents are observed in the forward direction due to the recombination of the electron-hole pair in the depletion regions.

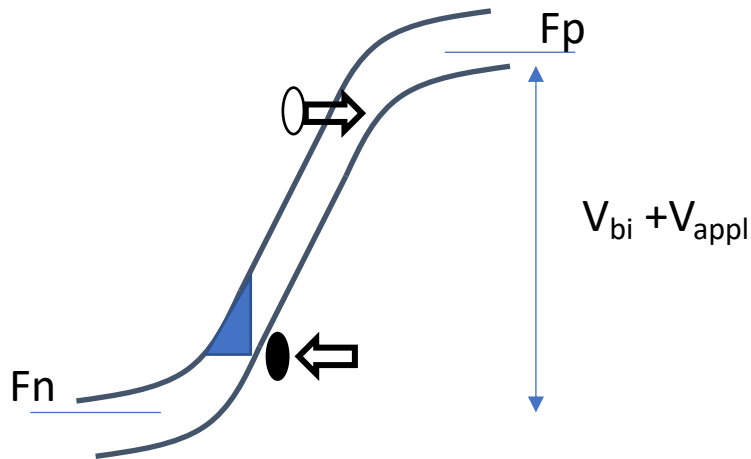
High injection:

1. Typically observed in the one-sided junction.
2. At high injection, the minority carrier injection is very close to the majority carrier density
3. Such high current density leads to ohmic potential drops, so the bands are not flat in the neutral region.
4. The net diode current in the high injection case is lower than that of ideal diodes due to series resistance drops.



Diode Breakdown

Tunneling breakdown

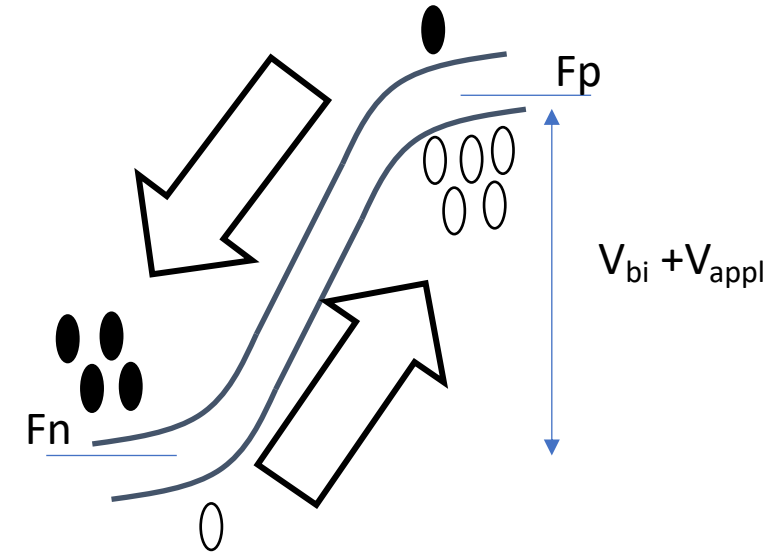


Band to Band tunneling through a narrow triangular barrier.

Band are narrower when the doping density is higher, the depletion width is smaller!

In situations, where The band-band tunneling has not yet happened and you still increase the reverse bias

Avalanche Breakdown



The carrier velocities are so large that, they create electron-hole pairs.

These are once again swept by the high field and this continues till the junction breaks down. This is called avalanche multiplication

Capacitances in a diode

Depletion capacitance / Junction capacitance

Due to the formation of di-poles at the interface, the total charge density Q in the junction varies with applied potential

The capacitance $C = \frac{dQ}{dV}$

How does the charge vary with the applied bias ?

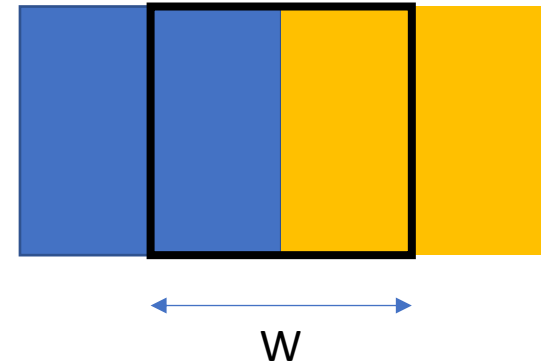
At equilibrium, we showed that the depletion width W is given by

$$W = \left[\frac{2\epsilon V_{bi}}{q} \frac{N_A + N_D}{N_A N_D} \right]^{\frac{1}{2}}$$

If an external potential is applied,

$$W = \left[\frac{2\epsilon (V_{bi} - V_{appl})}{q} \frac{N_A + N_D}{N_A N_D} \right]^{\frac{1}{2}}$$

In parallel plate approximation $C_D = \frac{\epsilon}{W}$



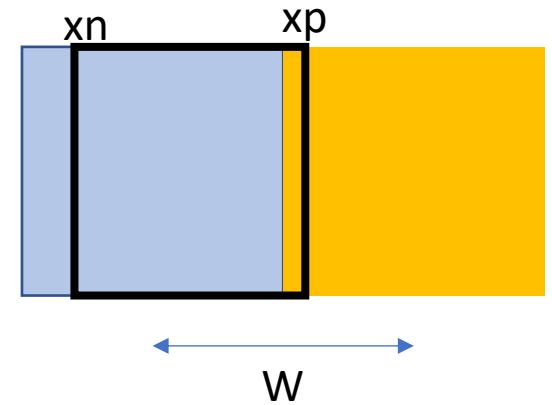
Let us consider a one-sided junction: For example a P⁺ - N

The depletion width is such that $|x_n| \gg |x_p|$

The width $W = x_n + x_p \cong x_n$

The capacitance equation now becomes

$$C_D = \frac{\epsilon}{W} = \sqrt{\frac{q\epsilon N_A}{2}} \left[V_{bi} - V_{appl} - \frac{2KT}{q} \right]^{-1/2}$$



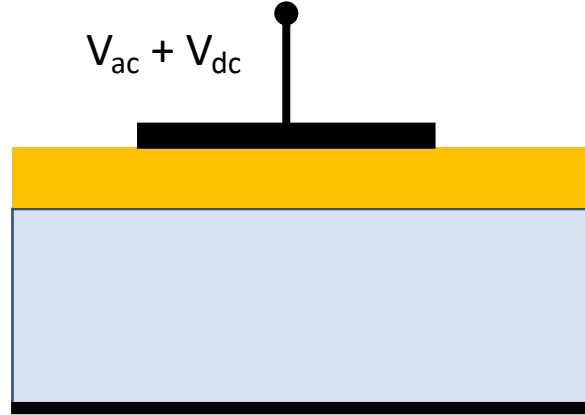
Therefore, the capacitance is dominated by the applied bias and the doping density of the weakly doped side.

$$\frac{1}{C_D^2} = \frac{2}{q\epsilon N_A} \left[V_{bi} - V_{appl} - \frac{2KT}{q} \right]$$

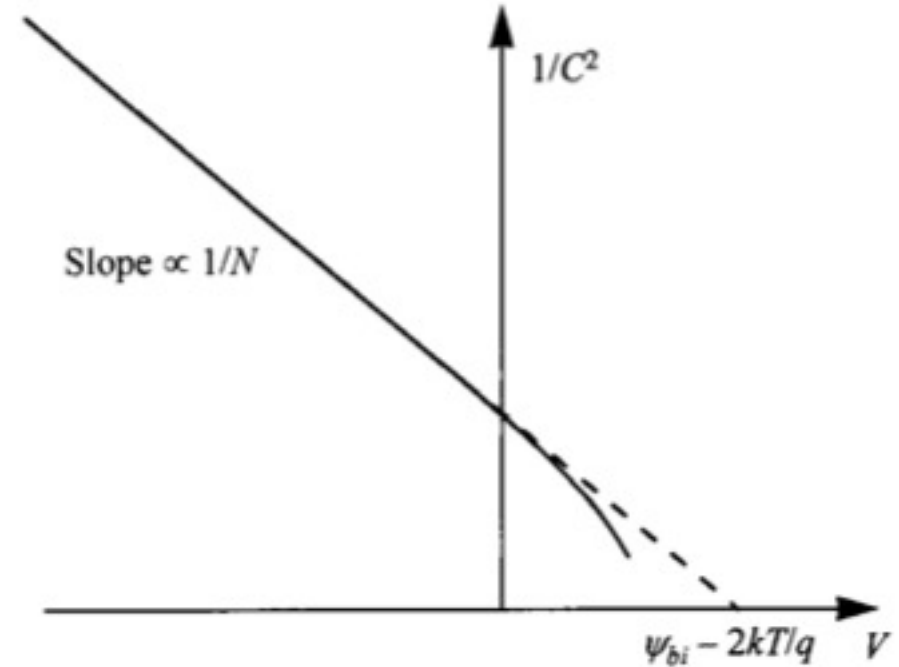
$$\frac{d\left(\frac{1}{C_D^2}\right)}{dV} = -\frac{2}{q\epsilon N_A}$$

Capacitance – voltage profiling

Take a PN junction device



- The slope of the curve gives the doping density.
- The depth at which the doping density is obtained is $x_D = \frac{\epsilon A}{C_D}$
- The built-in potential is obtained from x-intercept



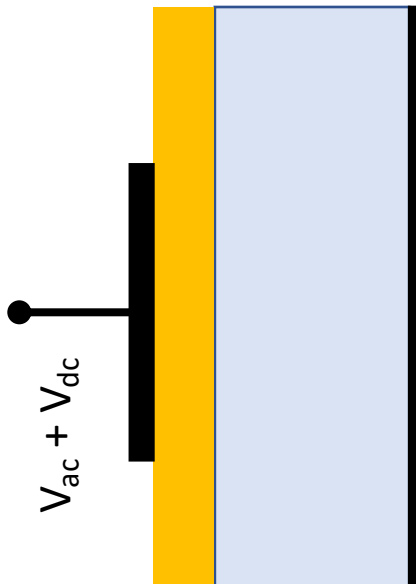
Caveats: Area and dielectric constant appears in square.

Diffusion capacitance

In reverse bias, the depletion capacitance/ junction capacitance dominate the total capacitance.

However, in the forward bias, there is an additional component to the device capacitance

Diffusion capacitance: When the forward biased device is abruptly changed to reverse bias, can the minority charge carriers change also abruptly ?



Let us consider a P⁺-N device

We were at steady state forward bias and then abruptly change the bias to reverse.

Time dynamics is governed by the continuity equation in the N type.

$$-\frac{\partial J_p(x, t)}{\partial x} = \frac{q \partial p(x, t)}{\tau_p} + q \frac{\partial p(x, t)}{\partial t}$$

$$-\frac{\partial J_p(x, t)}{\partial x} = \frac{q \partial p(x, t)}{\tau_p} + q \frac{\partial p(x, t)}{\partial t}$$

Lets integrate the equation in x-dimension

$$J_p(0) - J_p(x) = \frac{q}{\tau_p} \int_0^x \partial p(x, t) + q \int_0^x \frac{\partial p(x, t)}{\partial t}$$

If we take a long diode, $x \rightarrow \infty$

$$I_p = \frac{Aq}{\tau_p} \int_0^x \partial p(x, t) + qA \int_0^x \frac{\partial p(x, t)}{\partial t}$$

$$I_p(t) = \frac{Q_p(t)}{\tau_p} + qA \frac{\partial Q_p(t)}{\partial t}$$

Therefore, the total current in the diode, is due to the general recombination of the excess minority carriers, and a second time dependence of stored charge density

We know the charge spatial dependence

$$Q_p(t) = \int_0^x \Delta p_n(t) e^{-x/L_p} dx = qAL_p \Delta p_n(t)$$

The injected excess density is given by $\Delta p_n(t) = p_n^0 \left(e^{\frac{qv(t)}{KT}} - 1 \right)$

Finally

$$Q_p(t) = qAL_p p_n^0 \left(e^{\frac{qv(t)}{KT}} - 1 \right)$$

The diffusion capacitance can be estimated from

$$C_d = \frac{dQ_p(t)}{dv(t)}$$

Relatively slower response of the injected minority carries in the neutral region is responsible for a 'reverse recovery' time, And hence a limitation in the operational frequency of the diode switch.

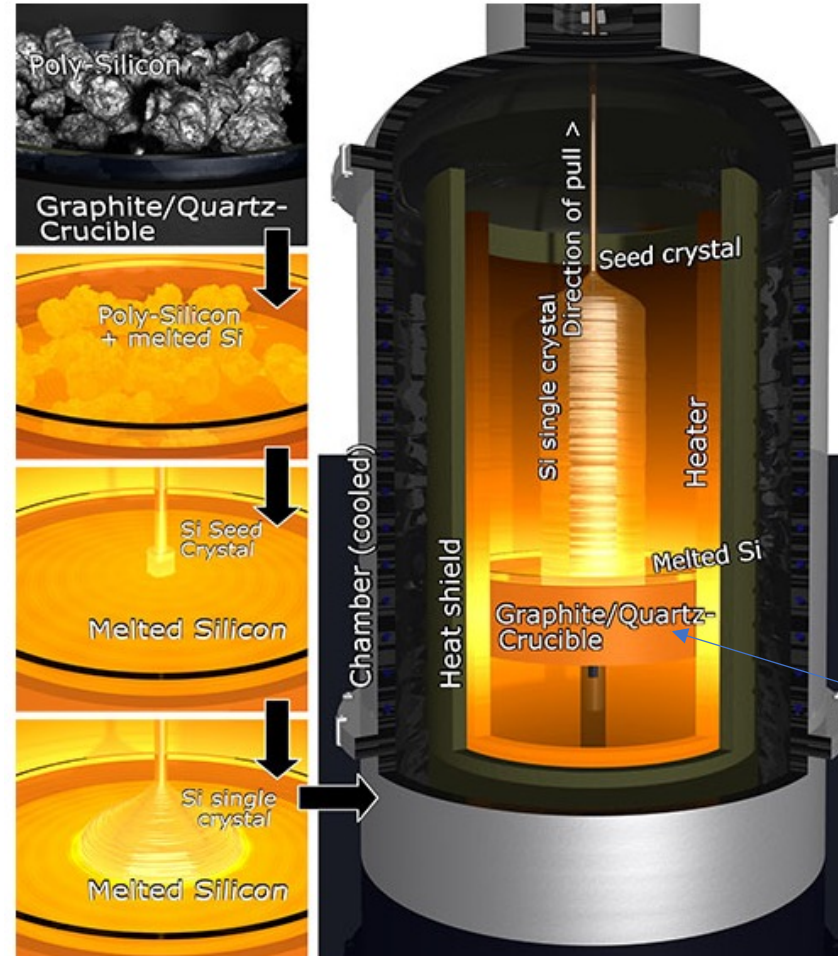
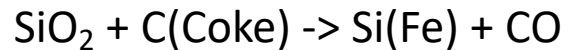
This is also true for other devices based on minority carrier injection: namely the BJT.

Semiconductor Growth and Doping Techniques

Example 1: 3D Crystal Growth from Seed:



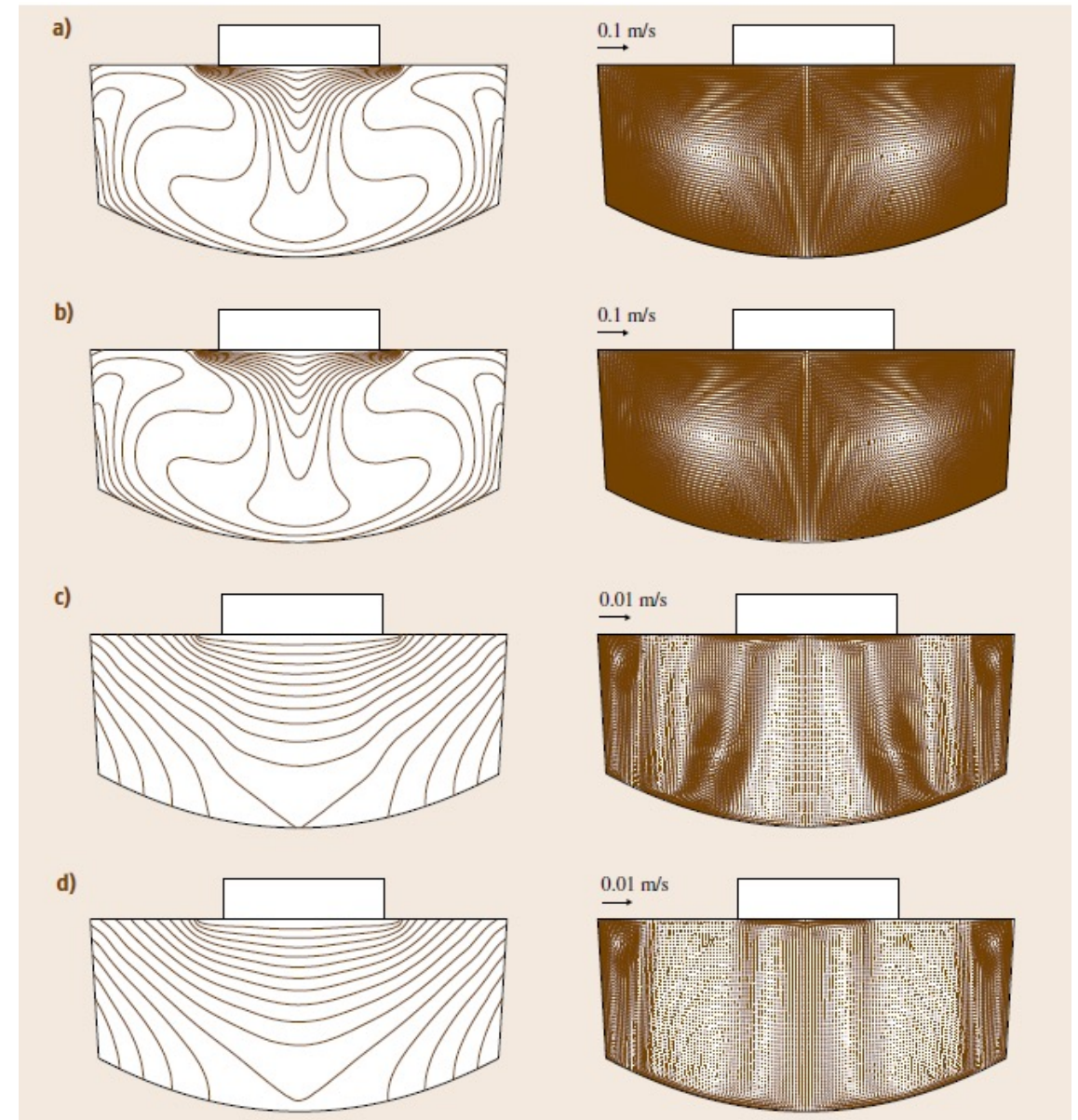
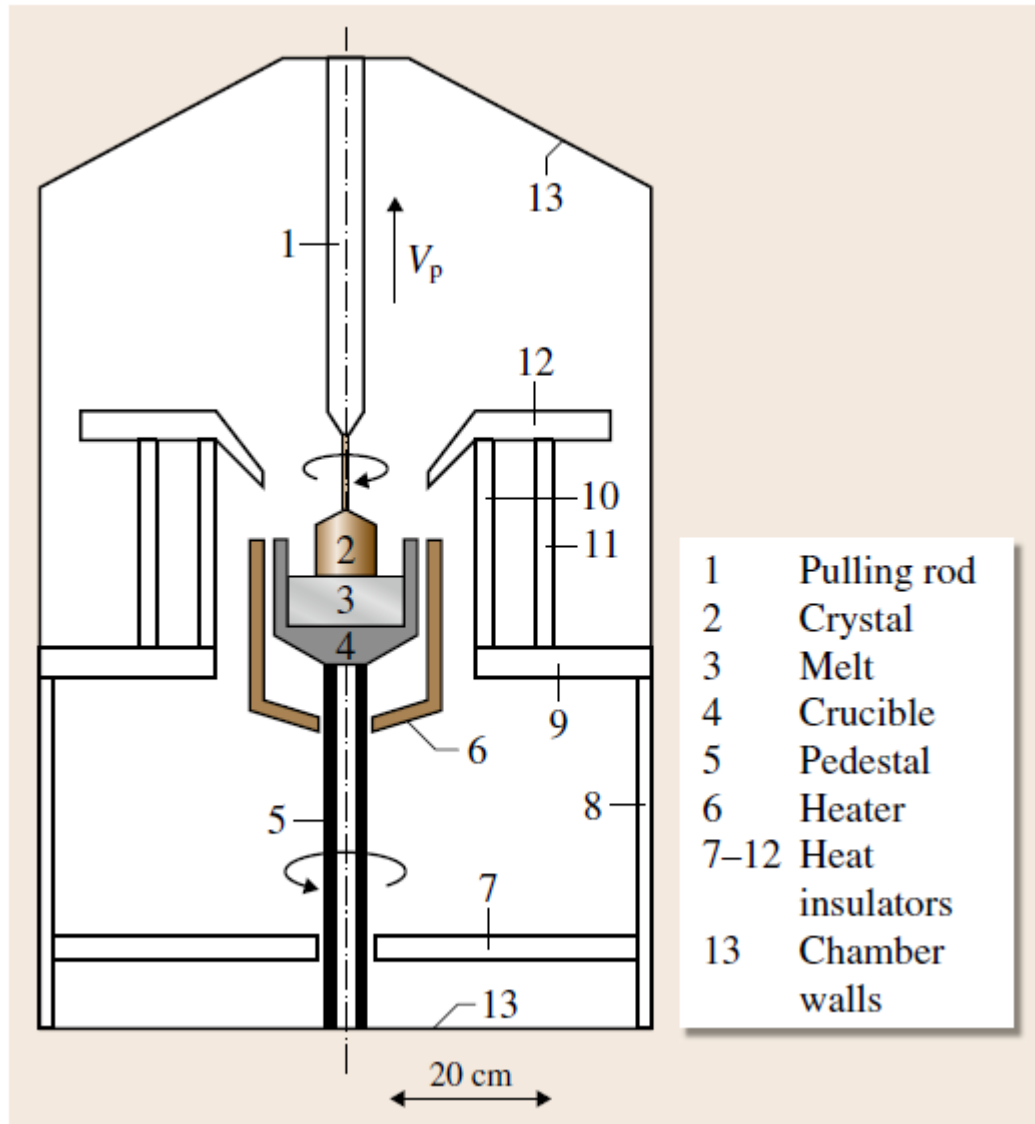
They say sand, but to get electronic grade Si, you need 99.999999999% pure Si powder



Si in the liquid phase gets attracted to the seed crystal
Due to surface tension.

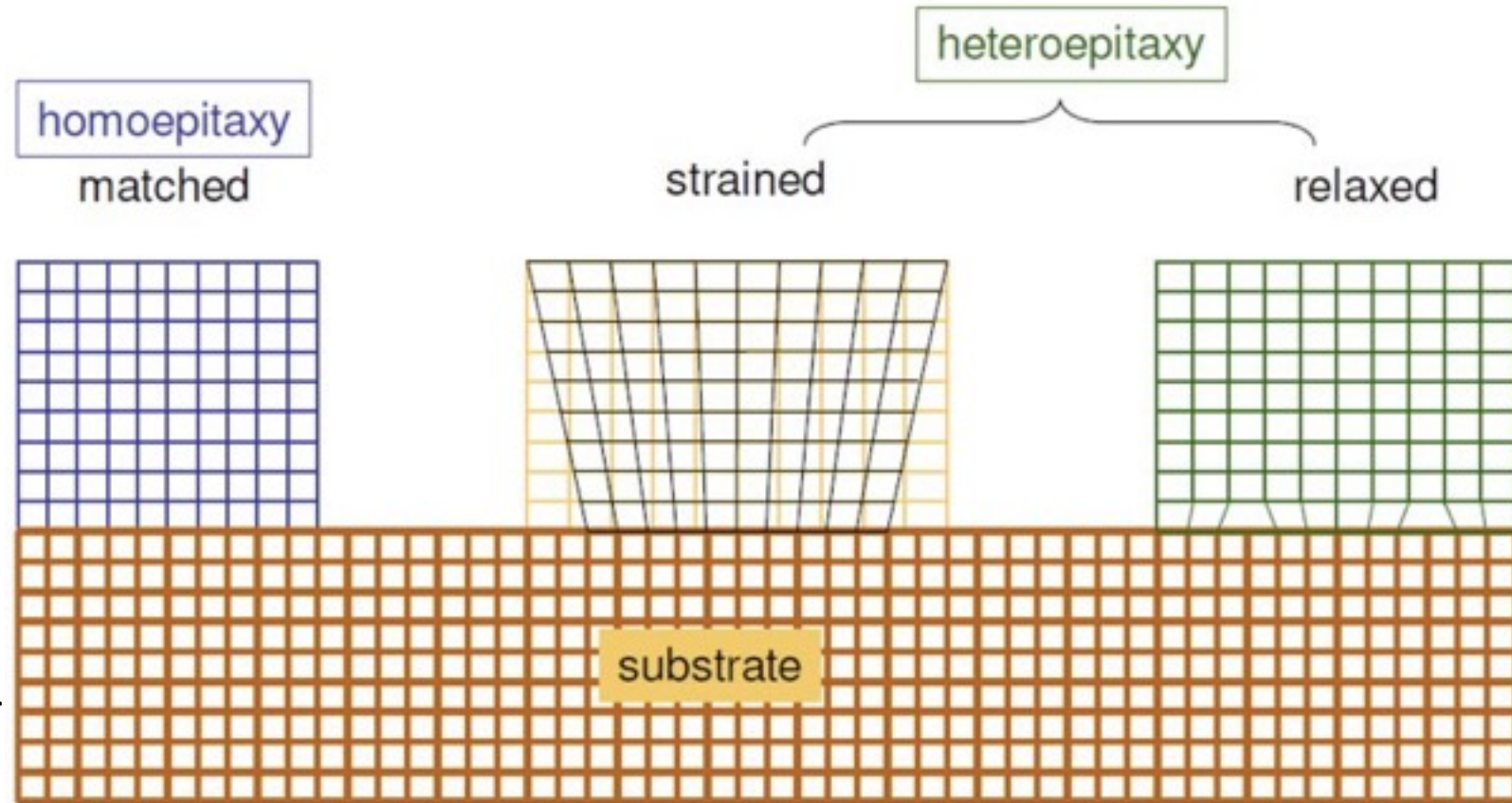
1500 C crucible

Czochralski process

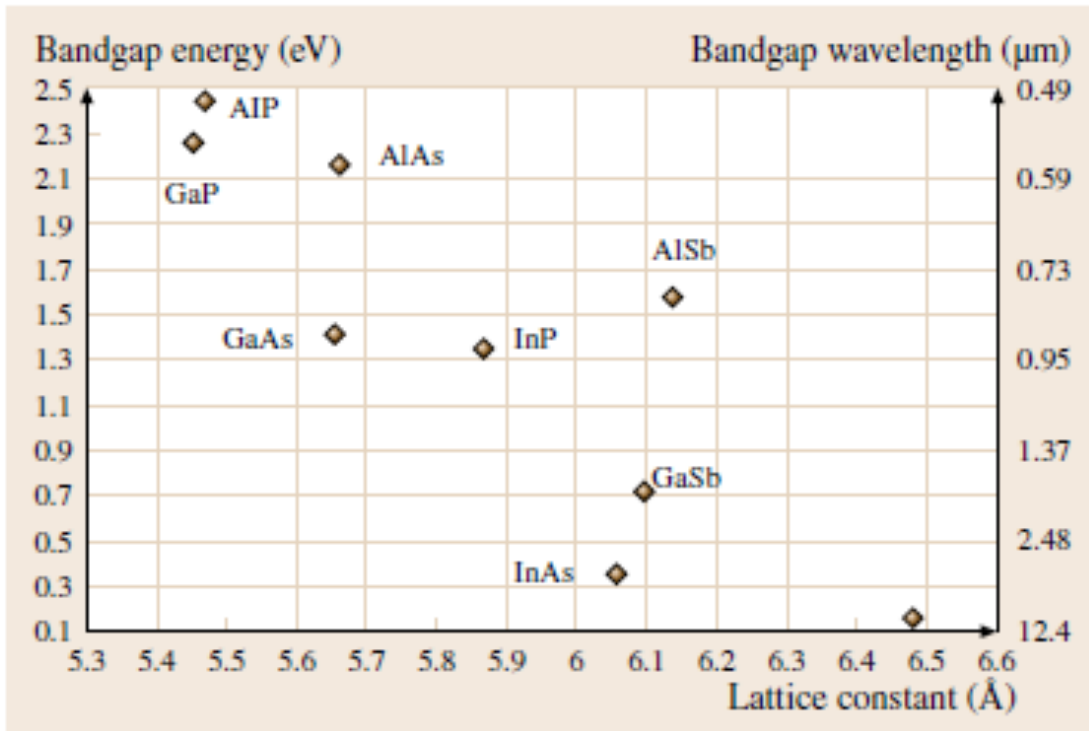


Epitaxy

- Epitaxy is growth of ordered layer over another pre-existing substrate.
- In conventional semiconductor industry, it is used to grow crystalline layers of a semiconductor over a large area wafer.
- If the second layer is the same as the first layer, it is called as homoepitaxy and if the second layer is different, it is called as heteroepitaxy.

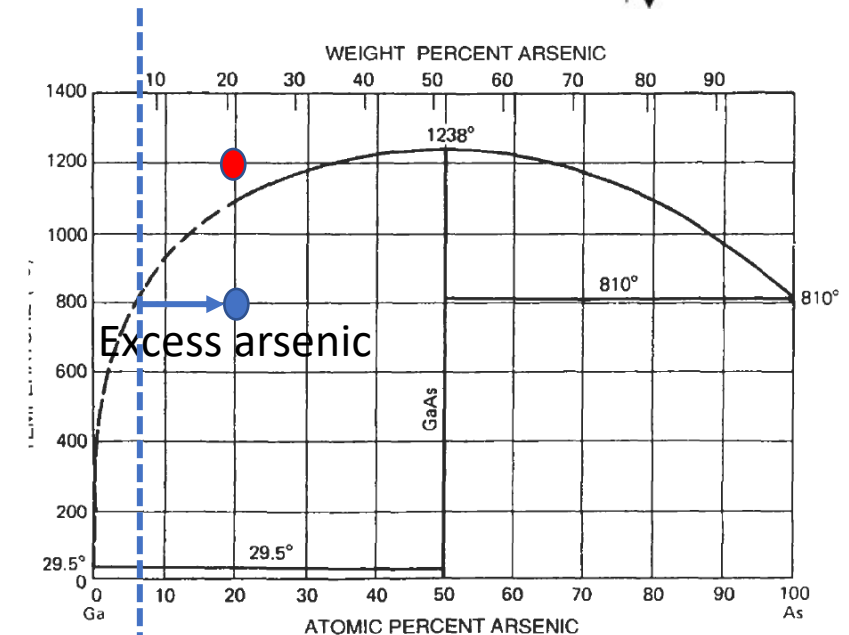
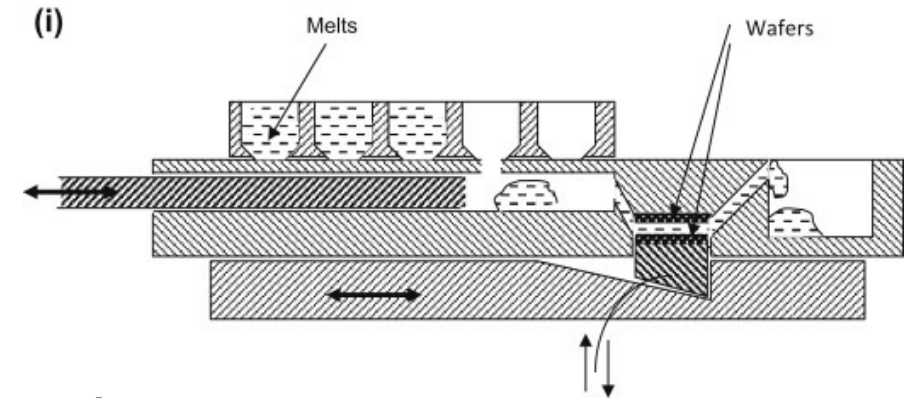


Liquid Phase epitaxy



- Low cost & controllable composition
 - Take a 10% As GaAs and heat it to 90%. It forms a nice alloy (Red dot)
 - Now cool it below the liquidus line, there is excess As in the phase
 - This will be ejected out as GaAs and this will grow heterogeneously! (blue dot)
- Rough surfaces and poor uniformity

Epitaxy – Known crystallographic relation between the substrate and device layer



Danaraj et. al., Hand book of crystal growth, © Springer
Mauk, Hand Book of crystal growth, ©Science Direct

Vapor phase epitaxy

Eg: $\text{TMGa} + \text{AsH}_3 \rightarrow \text{GaAs}$ at about 650 – 700C

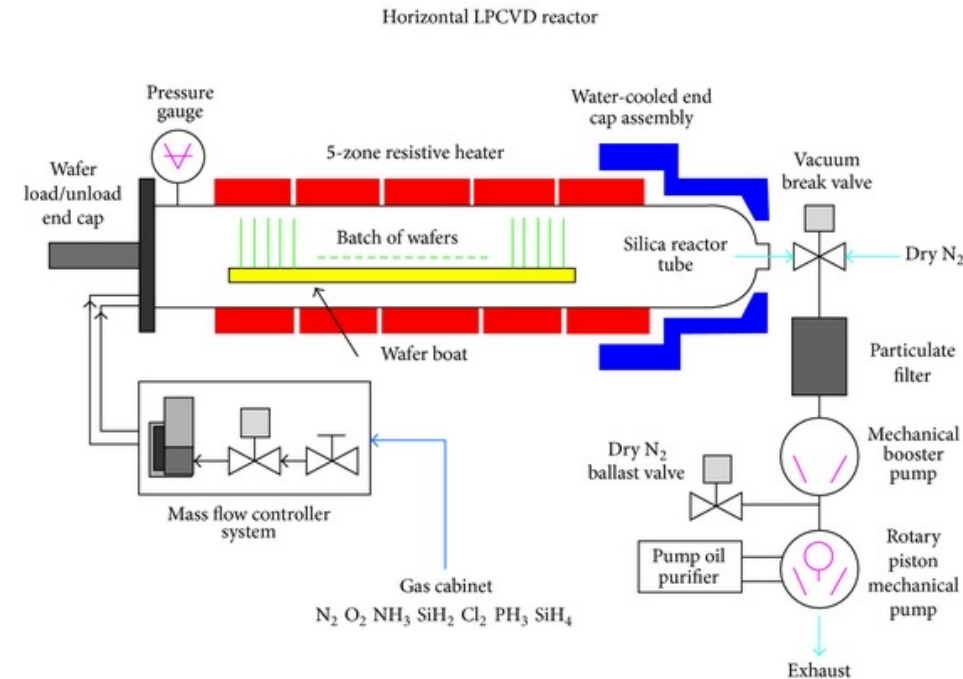
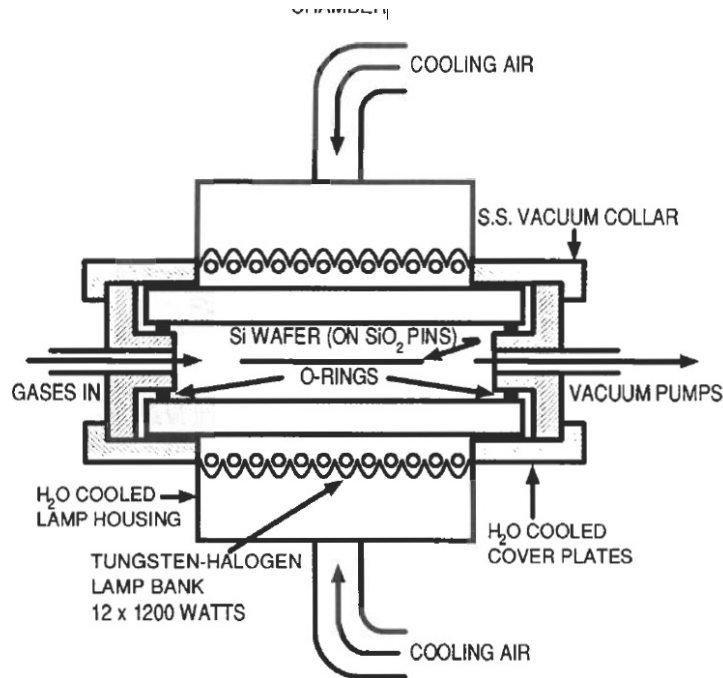


Figure 7-19. (Top) Schematic of VLE process; (bottom) schematic of RTCVD process. (Courtesy of M. L. Green, AT&T Bell Laboratories.)

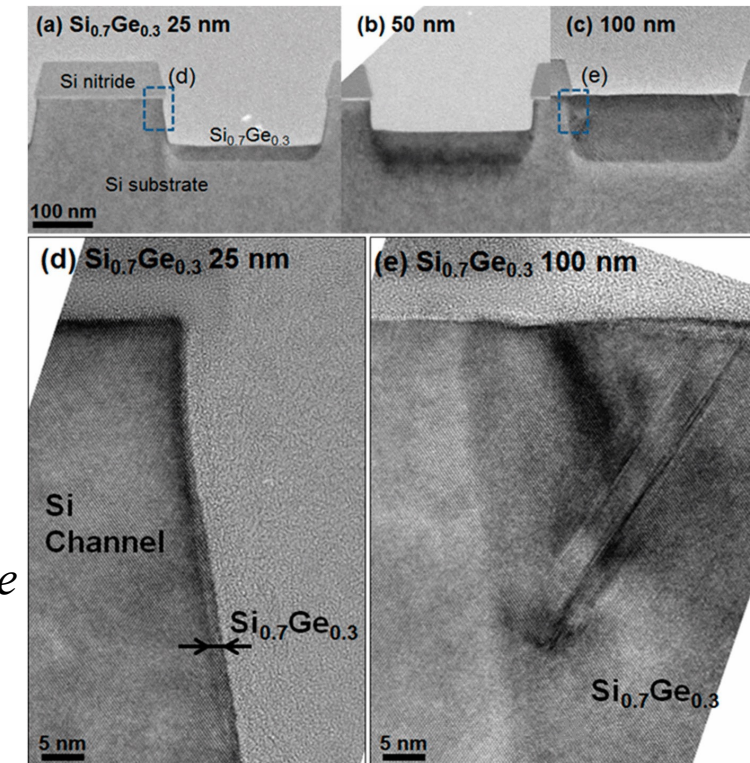
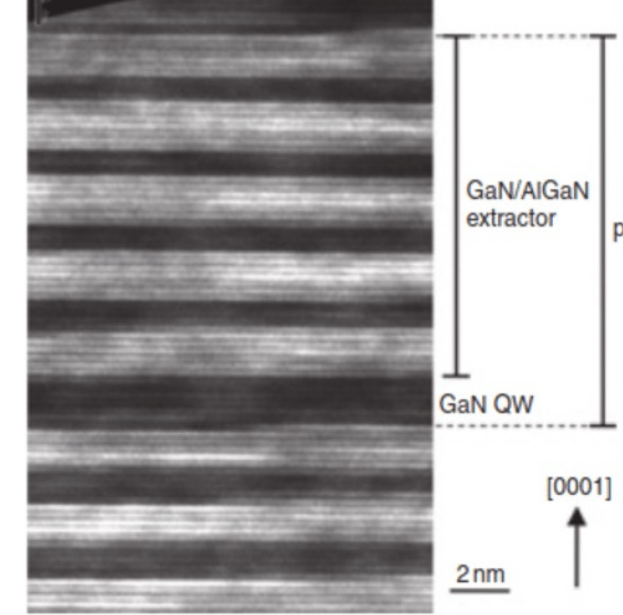
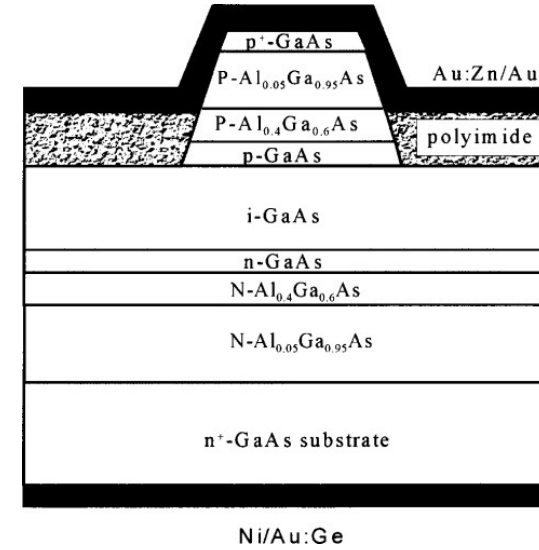
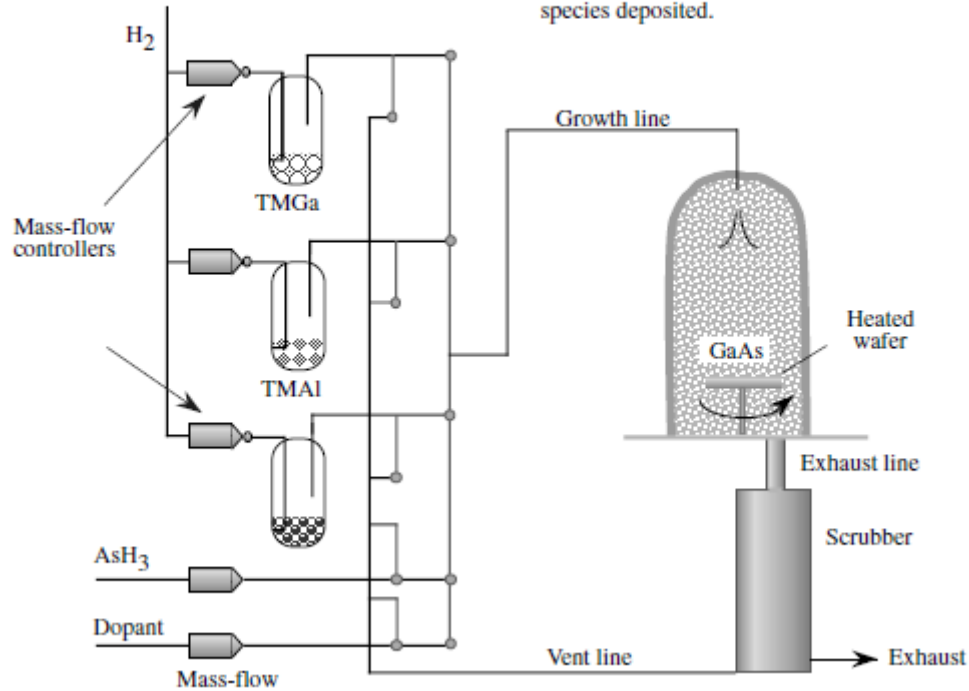
© University of Michigan

- No physical contact between substrate and reactor
- Thin layers are possible
- Sharp transition can be produced between multi-layer stacks
- Scale up is feasible

2D Nanostructures

An example by MOCVD growth

Chemical reaction at the heated substrate deposits GaAs or AlAs. Mass flow controllers control the species deposited.



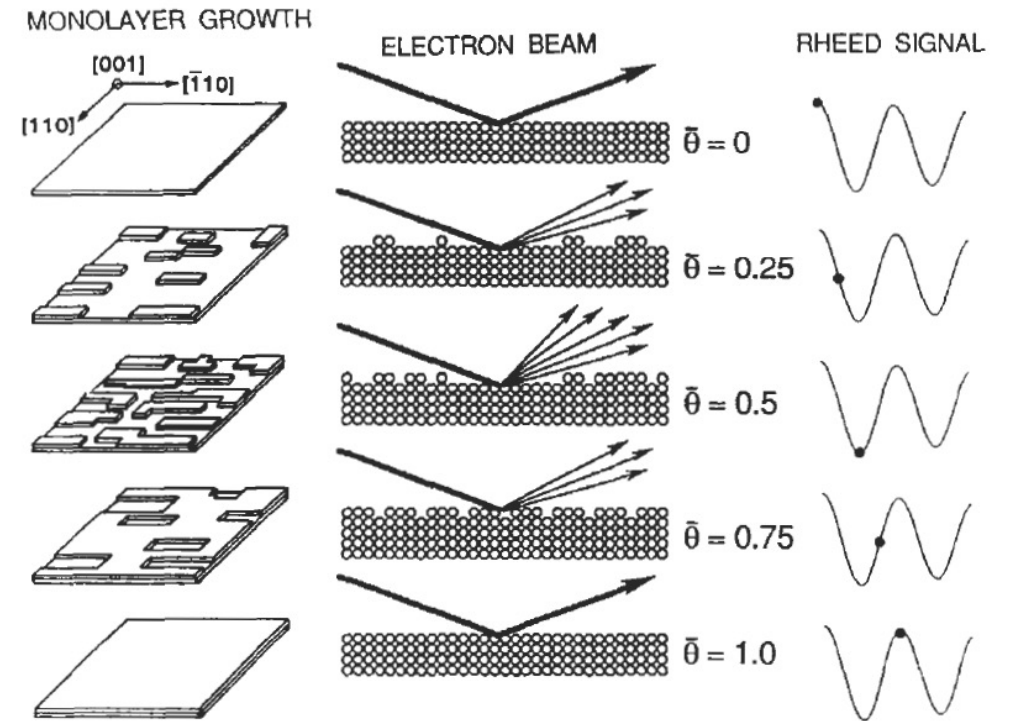
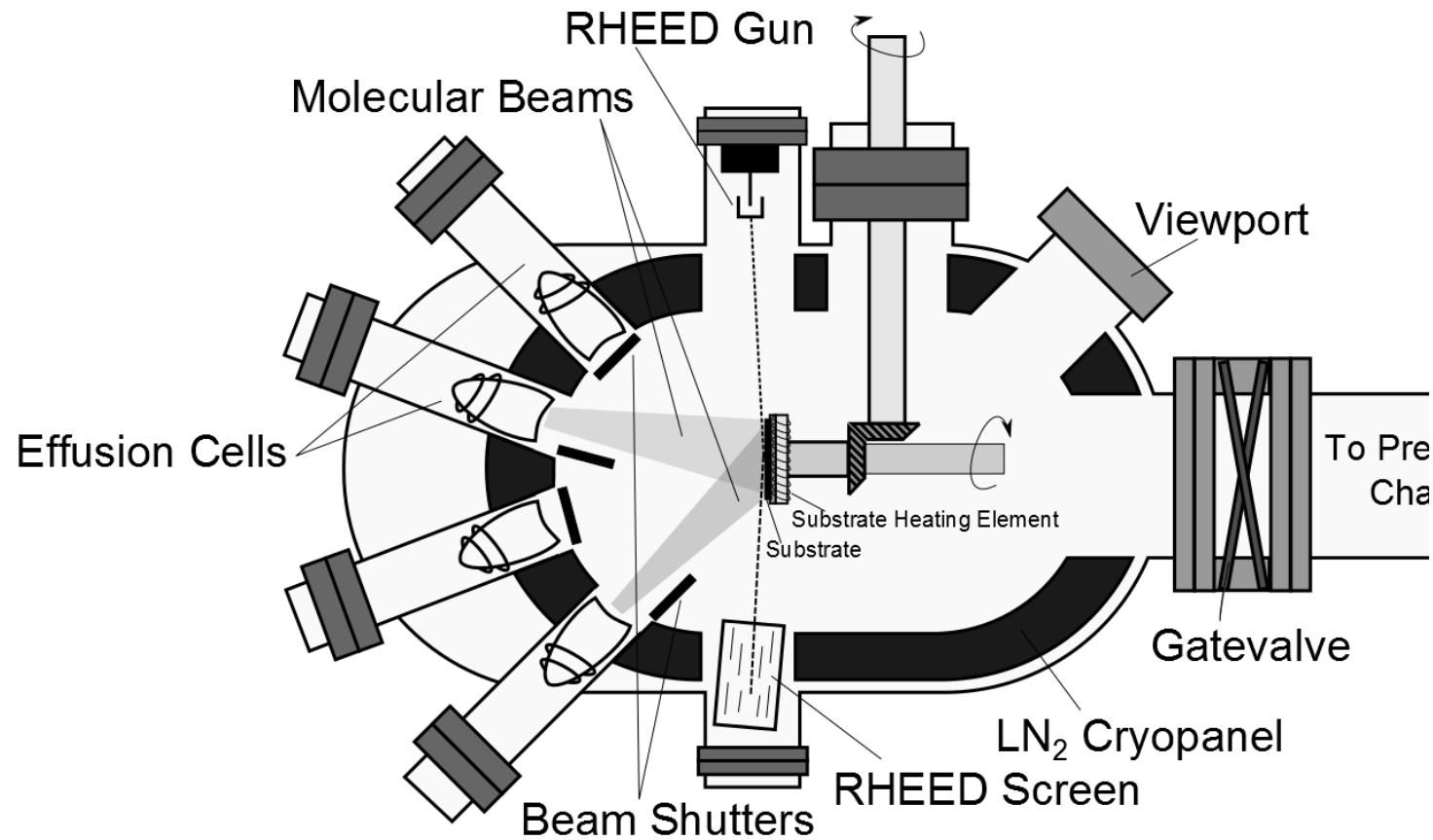
J. Singh, *Electronic and Optoelectronic Properties of Semiconductor Structures*, Cambridge Appl. Opt. **37**, 496-501 (1998)

[Acta Physica Slovaca](#) 65(2):65-U89

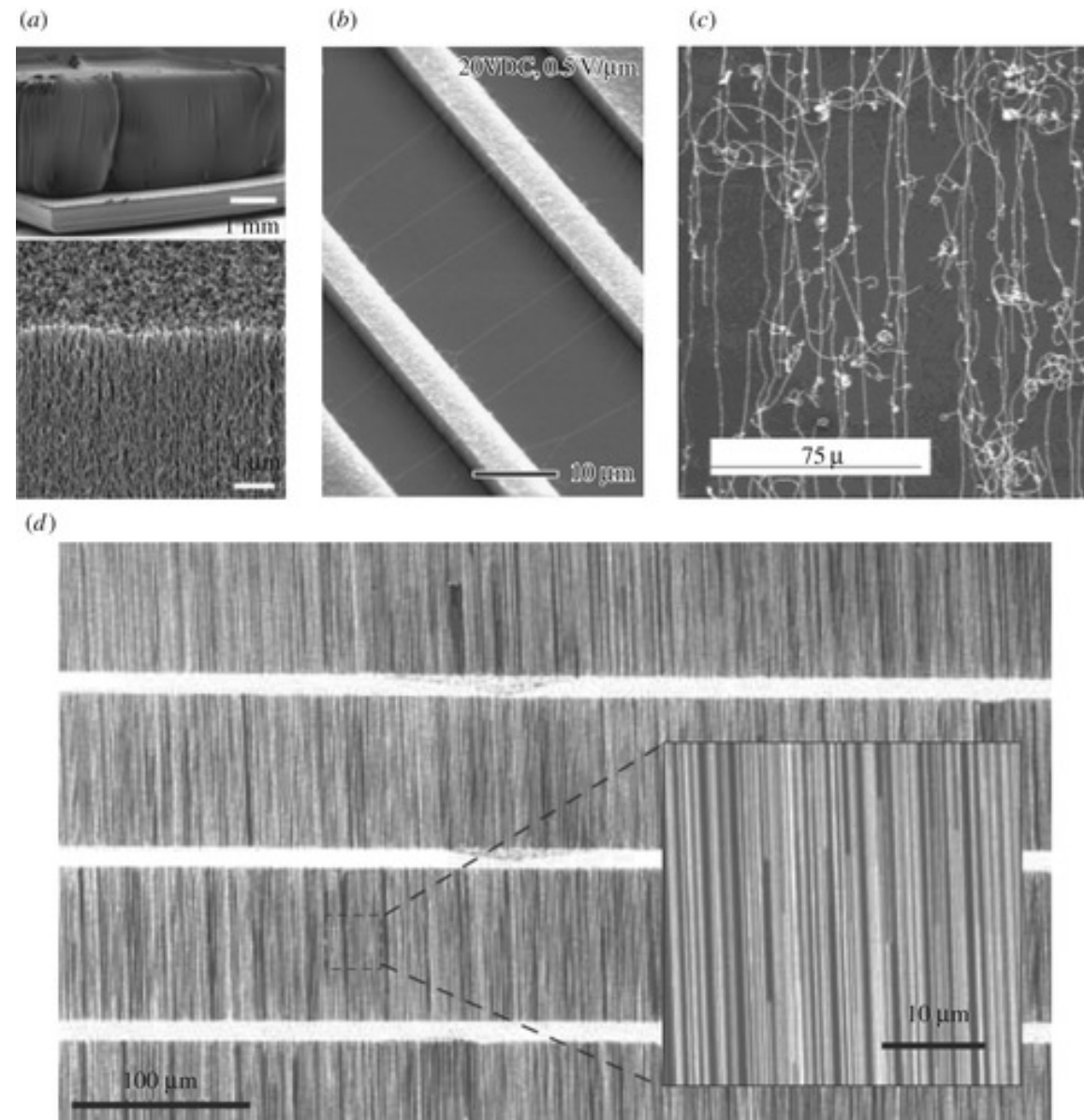
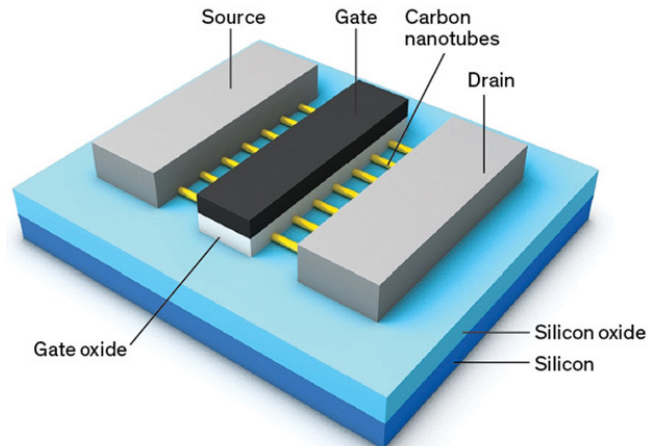
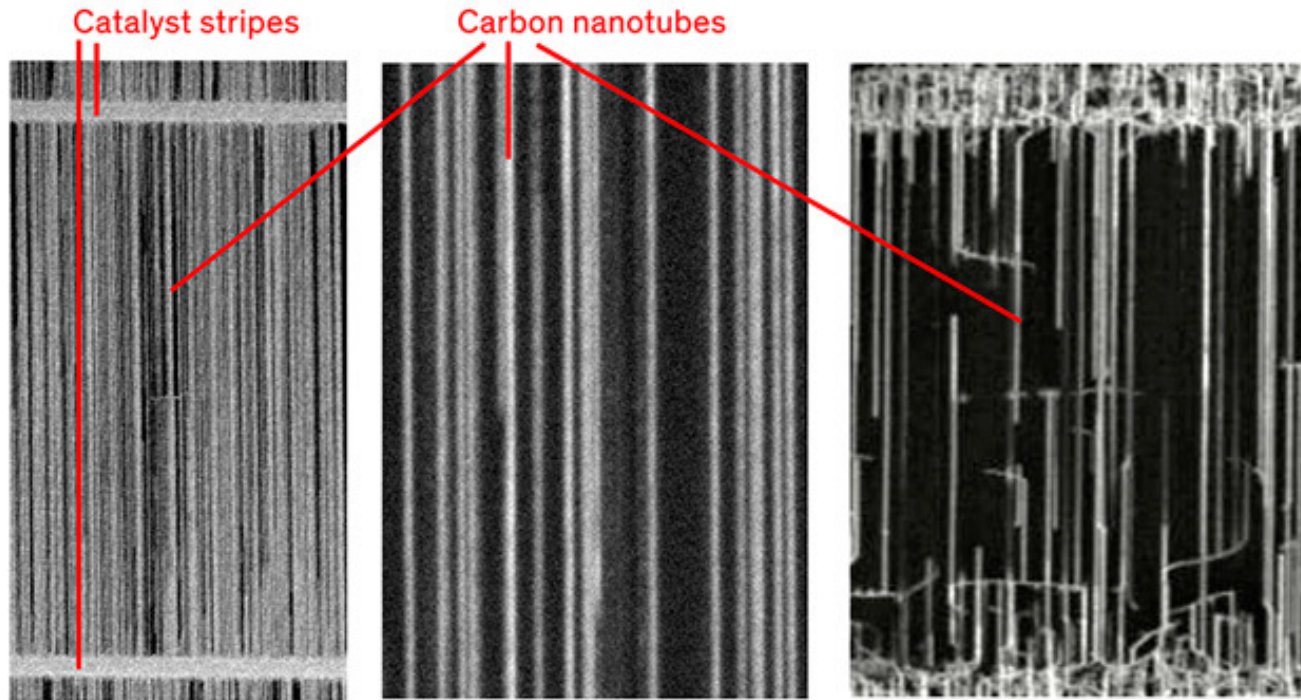
AIP Advances **6**, 095114 (2016);

Molecular Beam Epitaxy

1. High vacuum technique – 10^{-11} torr
2. Approximately 1 monolayer per sec.
3. Several monitoring tools.
4. Walls cooled by liquid N_2
5. One or more molecular beams are directed towards the substrate
6. Extreme material purity, doping control and thickness of layers

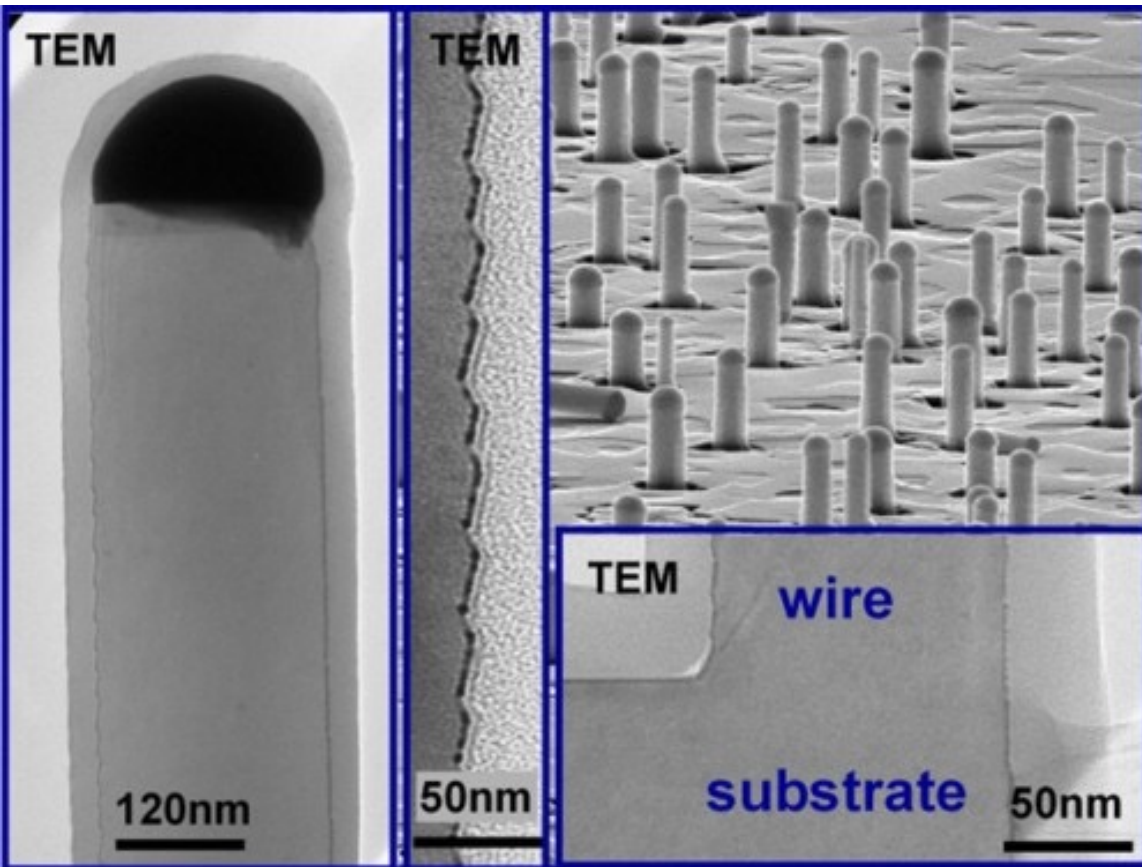


1D nanostructures

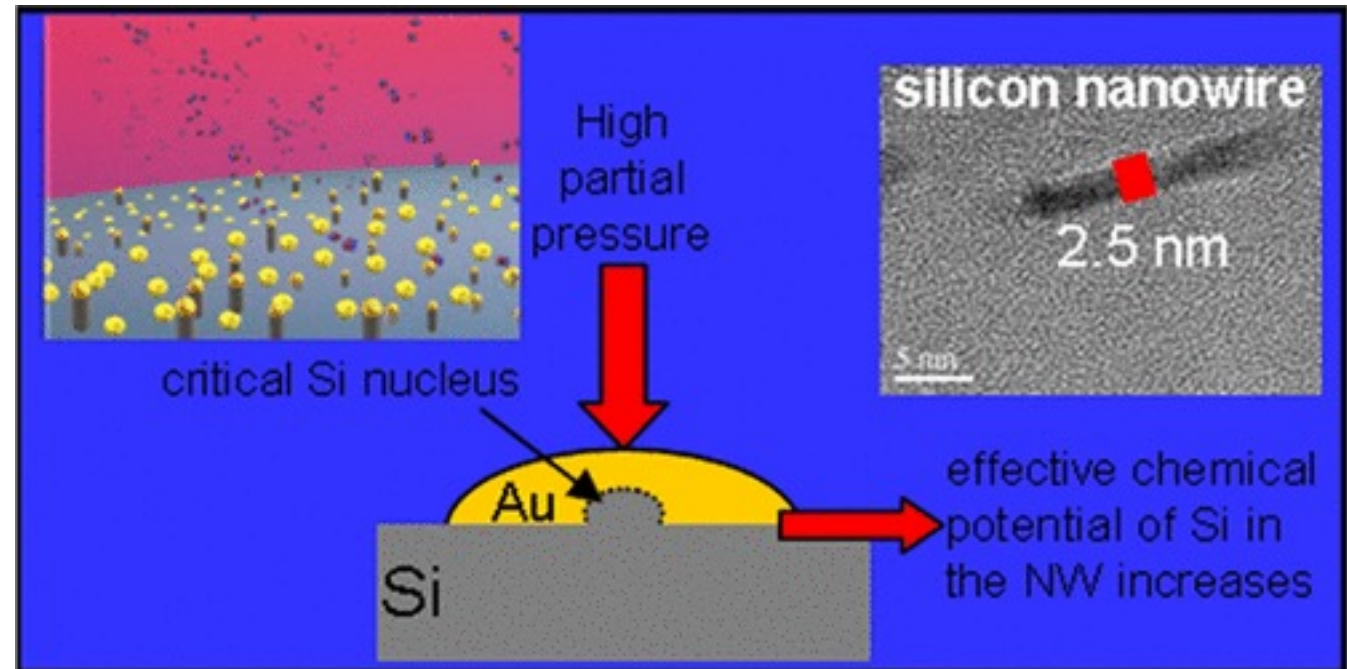


Growth by epitaxial CVD

Si Nanowires



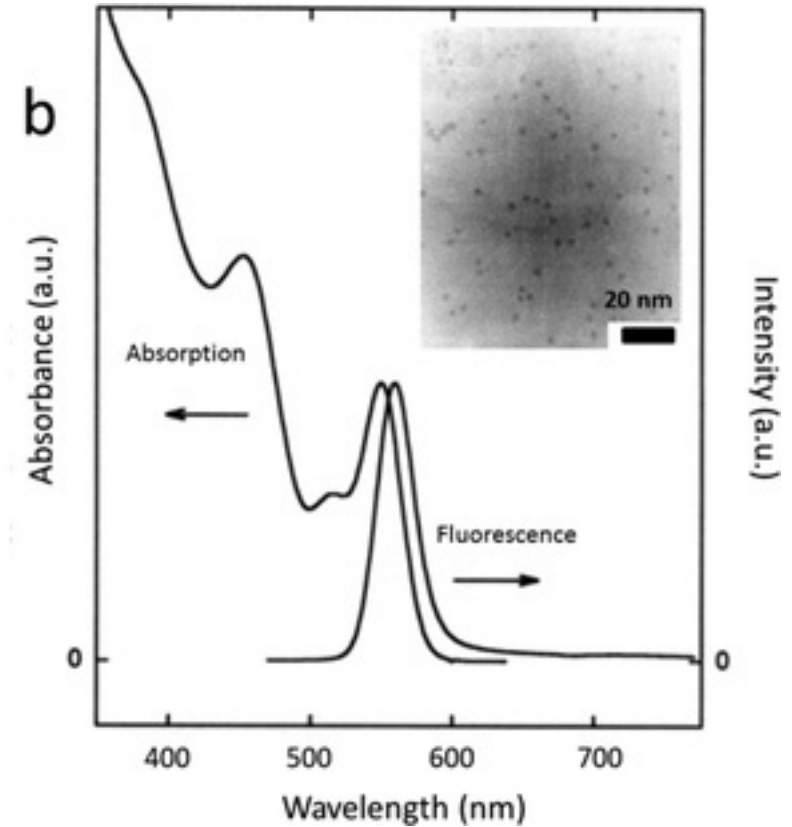
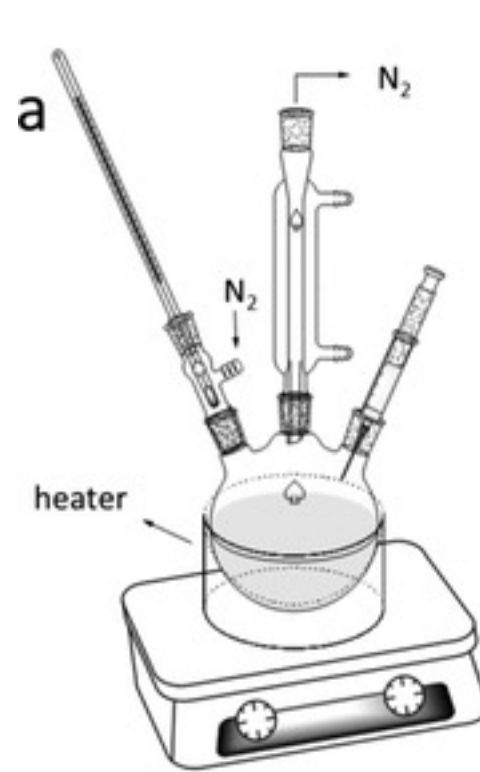
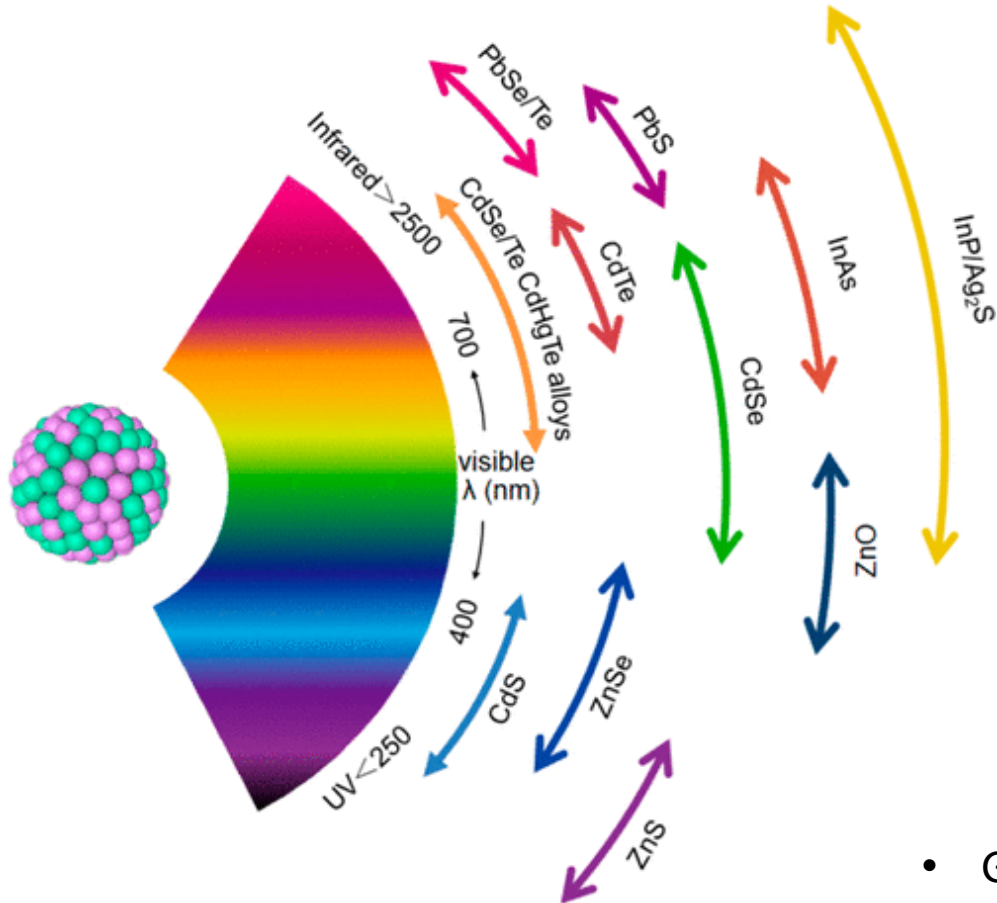
Vapor – Liquid – Solid Method



ACS Omega 2019, 4, 19, 17967–17971

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0-D nanostructures – Lateral sizes (10 – 100 nm)

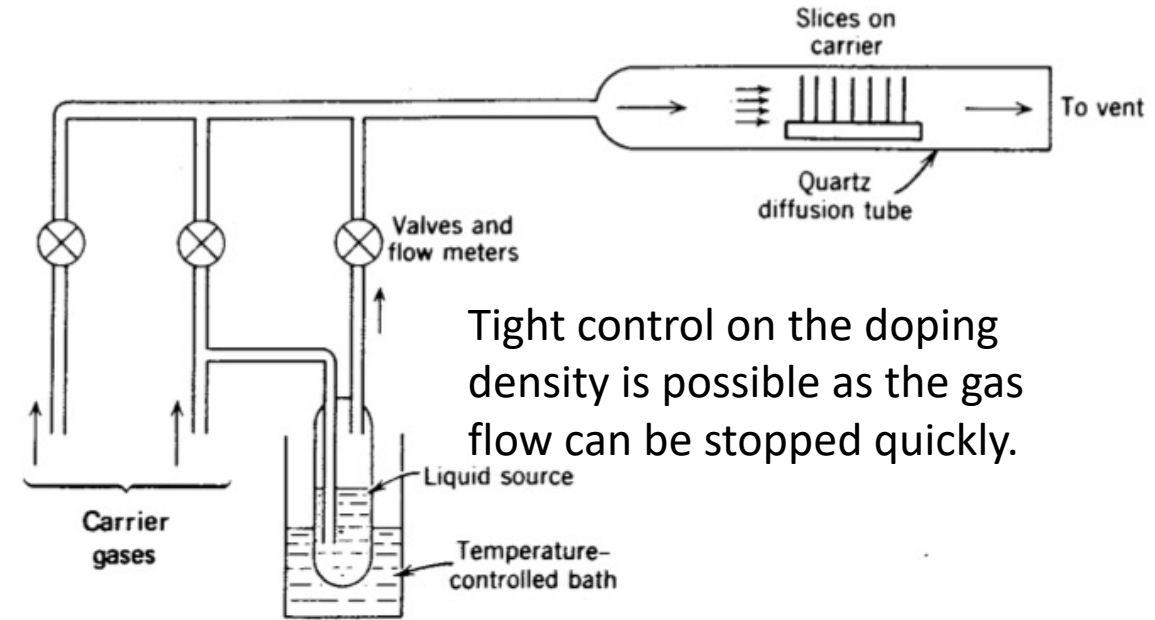
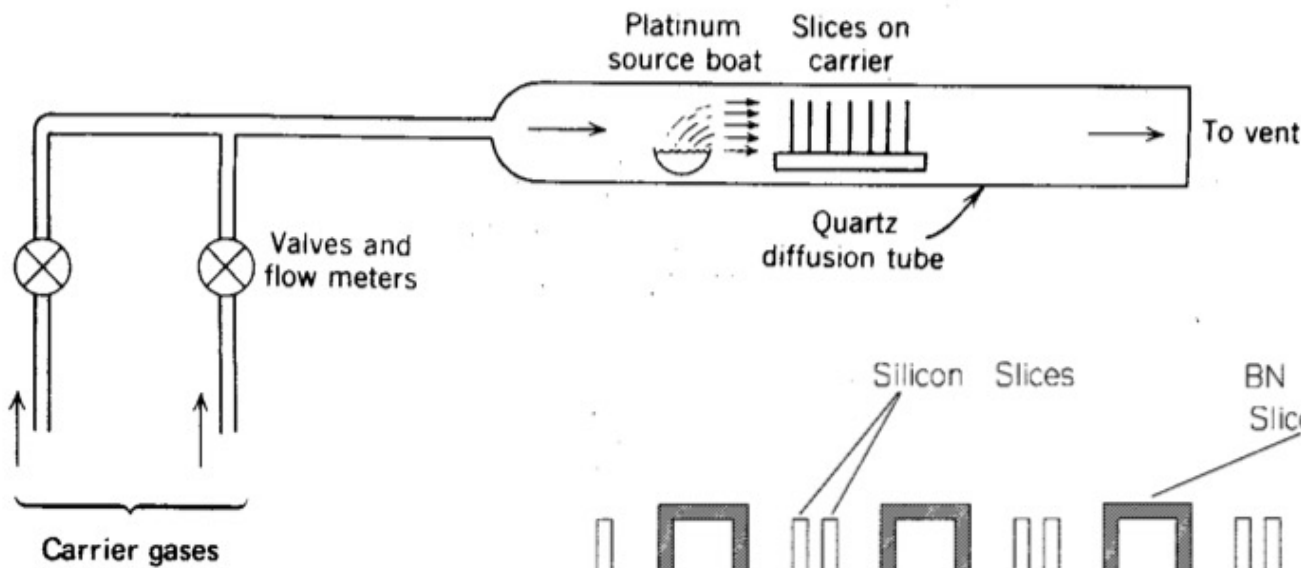


- Growth by wet- chemical means
- Homogeneous nucleation of nano particles
- Encapsulation of nucleated particles to prevent further growth

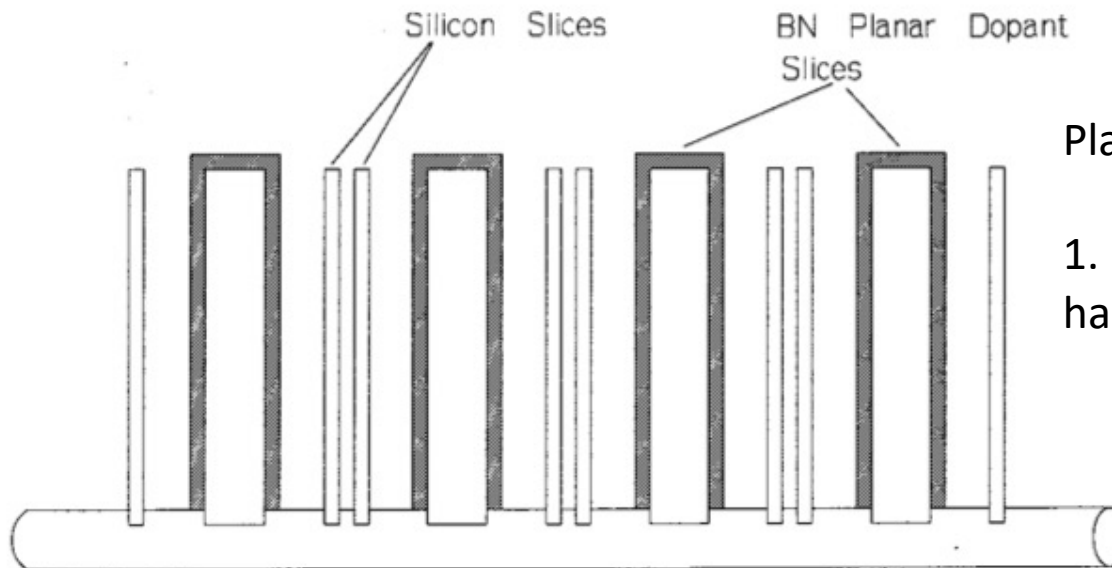
Doping Strategies

Liquid and Gaseous source diffusion

Solid Source diffusion



Tight control on the doping density is possible as the gas flow can be stopped quickly.



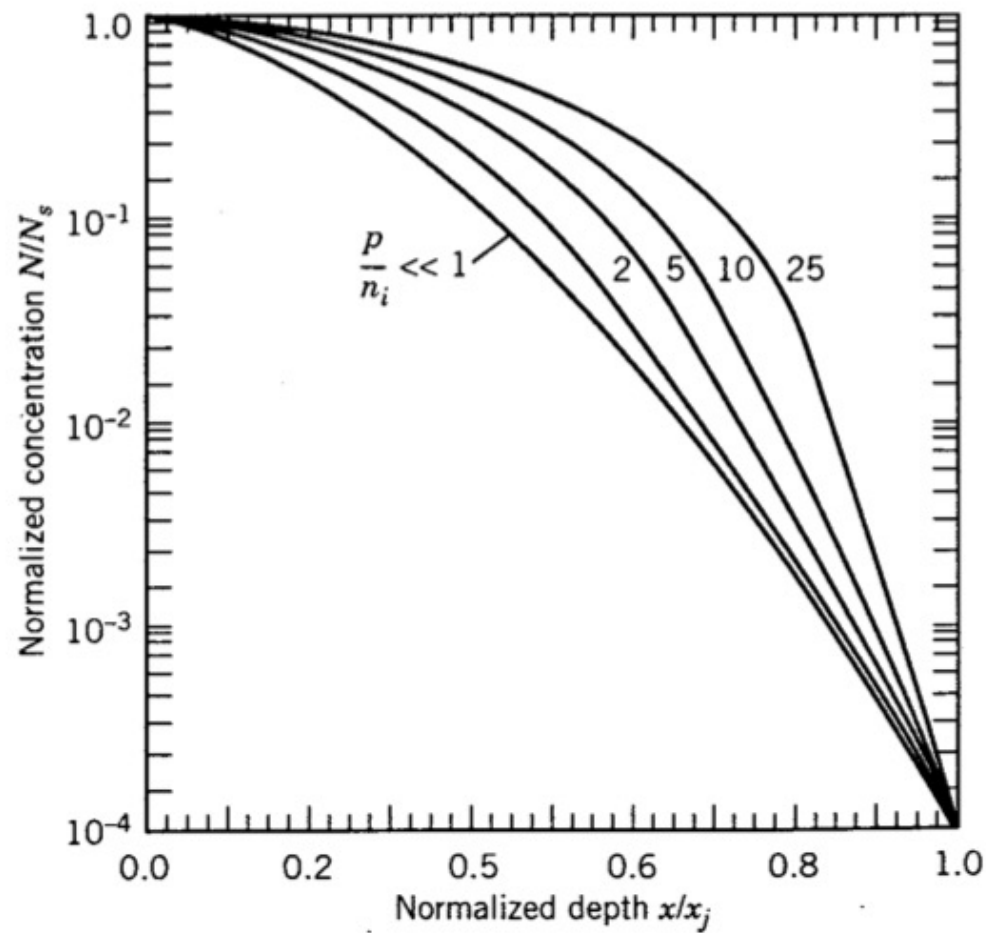
Planar source arrangement

1. Does not require any gas flows, simple handling

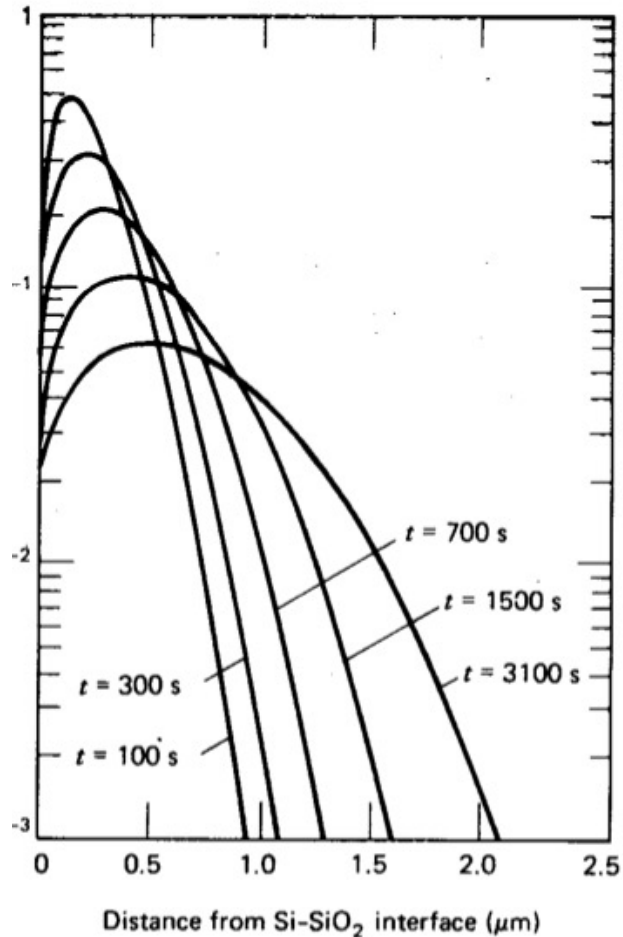
Dopant Profiles

In typical microfabrication processes, the diffusion is made through an opening in the SiO₂ layer.

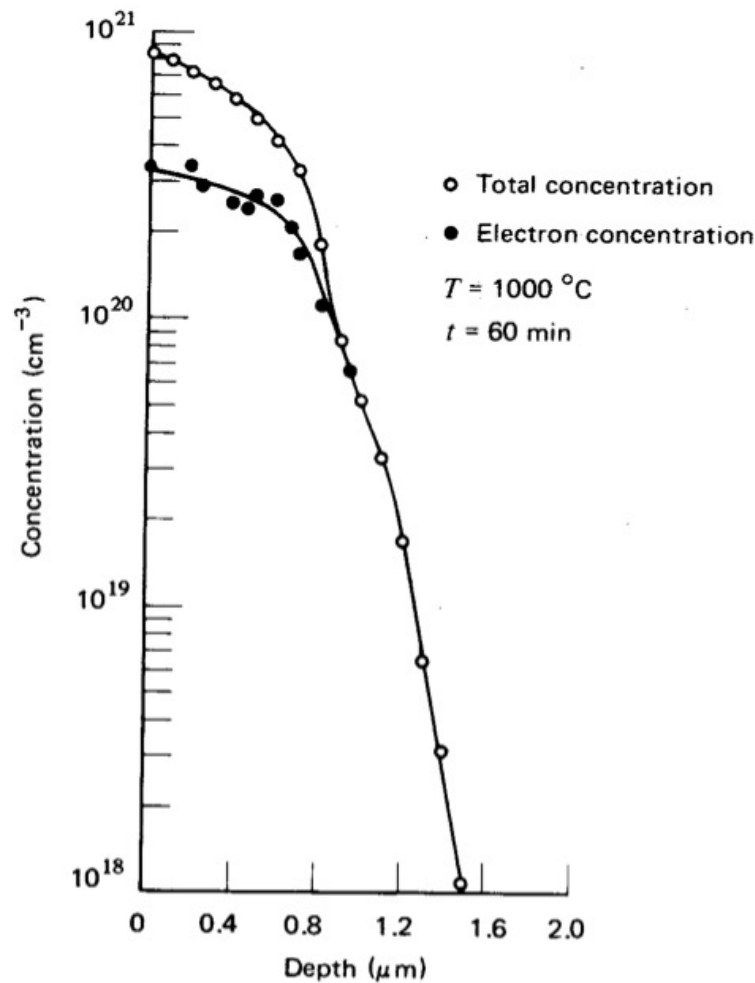
Boron dopant profile



Boron with redistribution effects

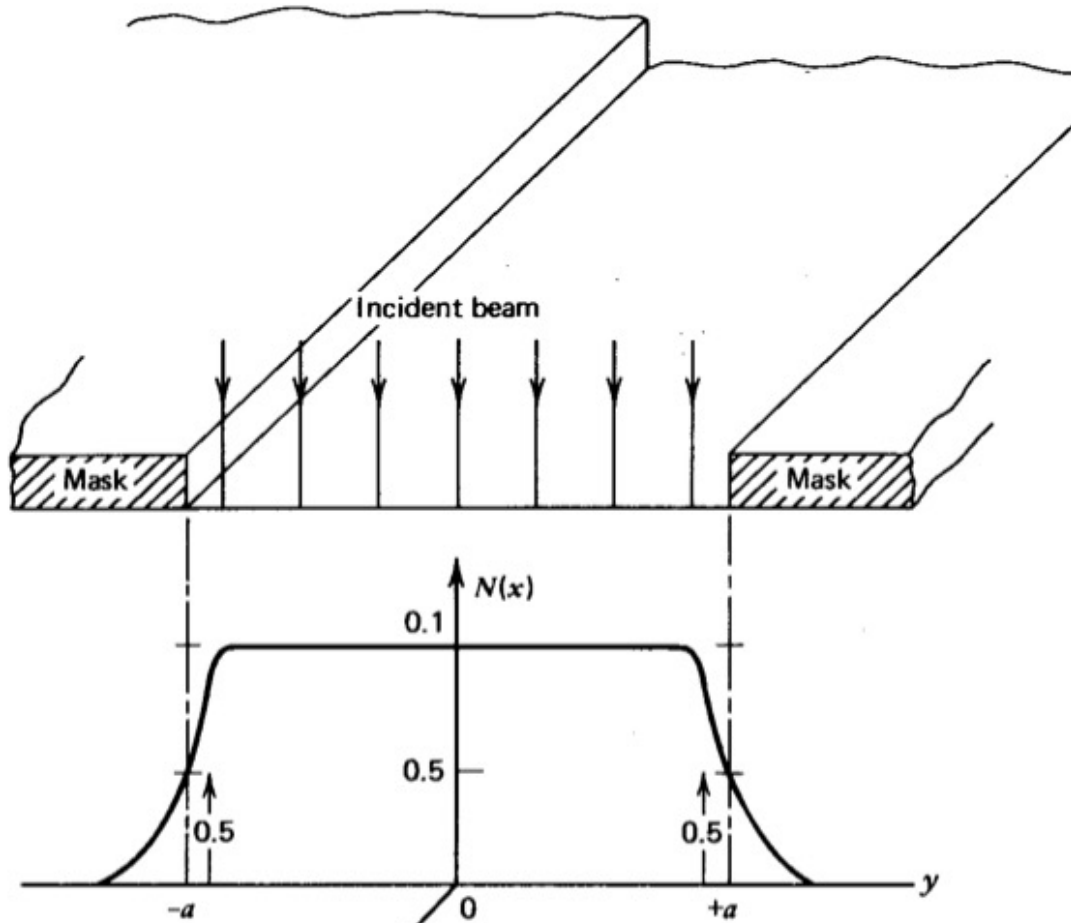


Phosphorus doping example



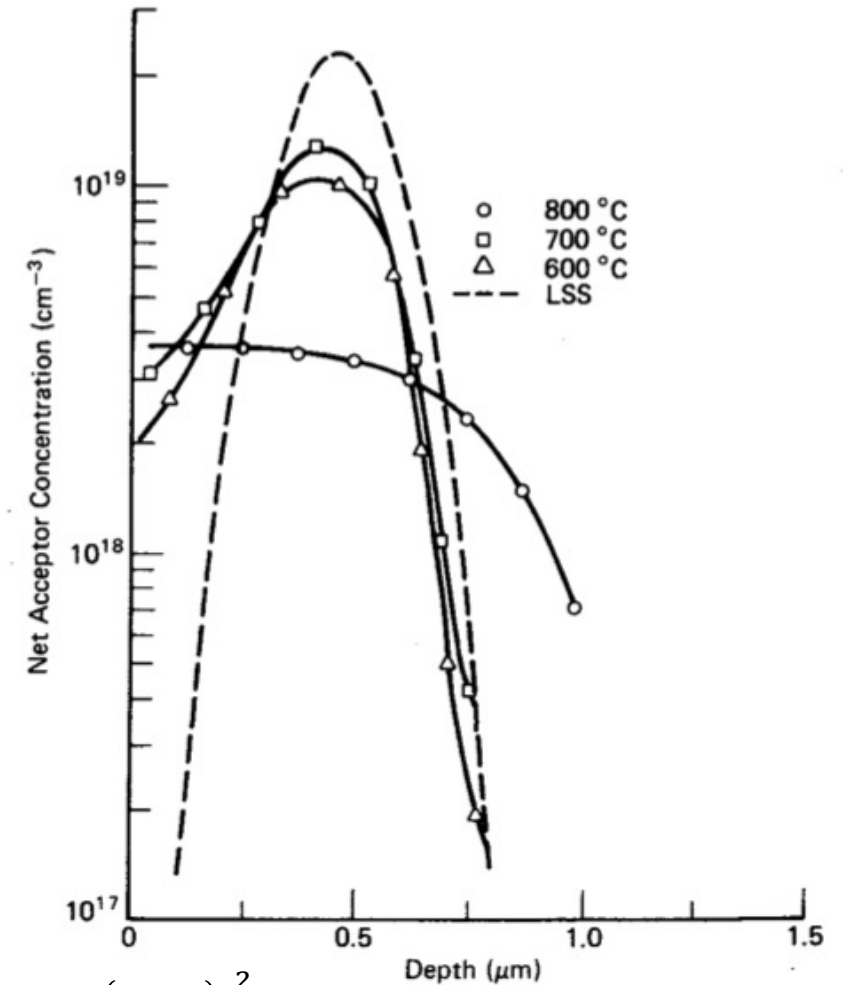
Ion implantation

Beryllium implants in Gallium Arsenide.



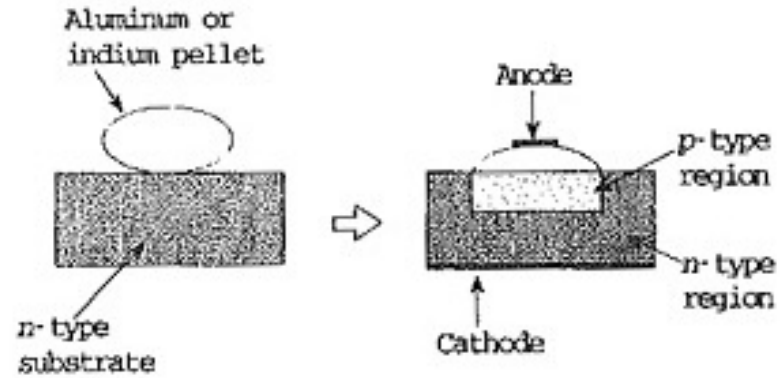
Implanted dose is ϕ ions/cm²

Implanted dose is largely a Gaussian $N(x) = \frac{\phi}{\sqrt{2\pi} \Delta R_p} e^{-\frac{1}{2} \left(\frac{x - R_p}{\Delta R_p} \right)^2}$

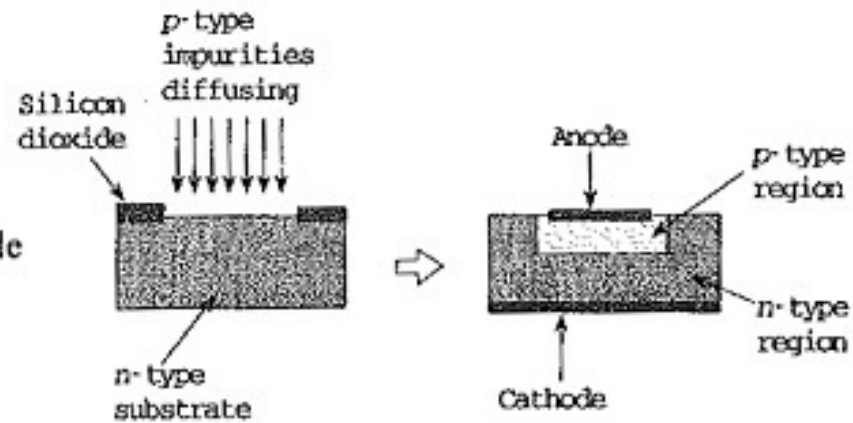


A practical PN junction diode fabrication

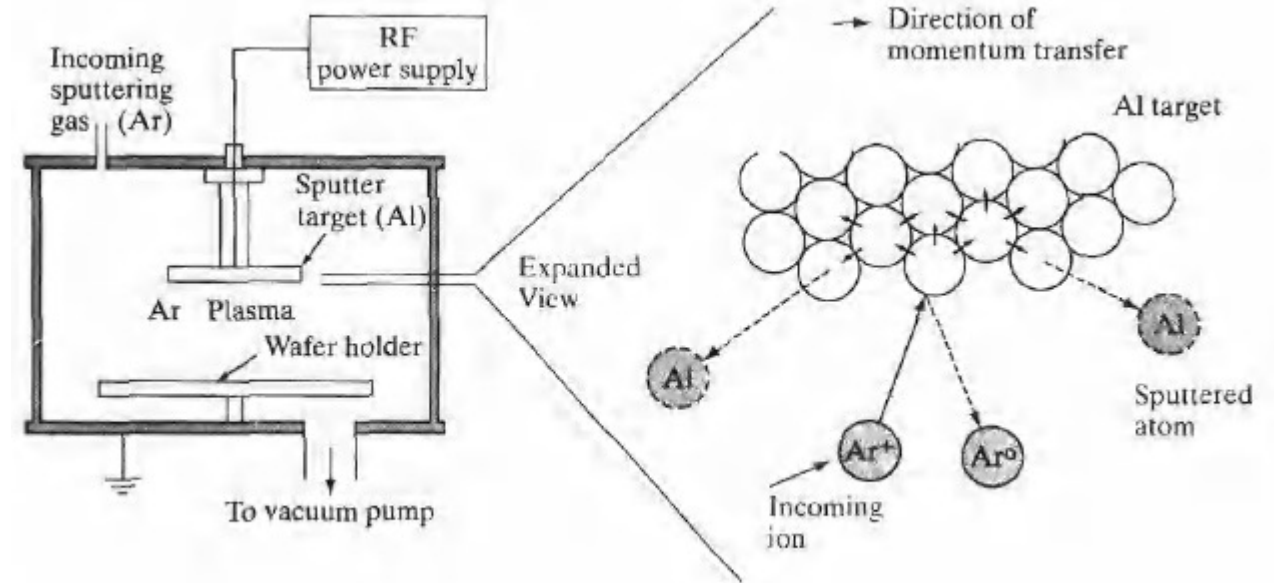
Alloy diode fabrication



Diffused diode fabrication



Metallization Technique



A metal semiconductor junction is crucial part of any semiconductor device