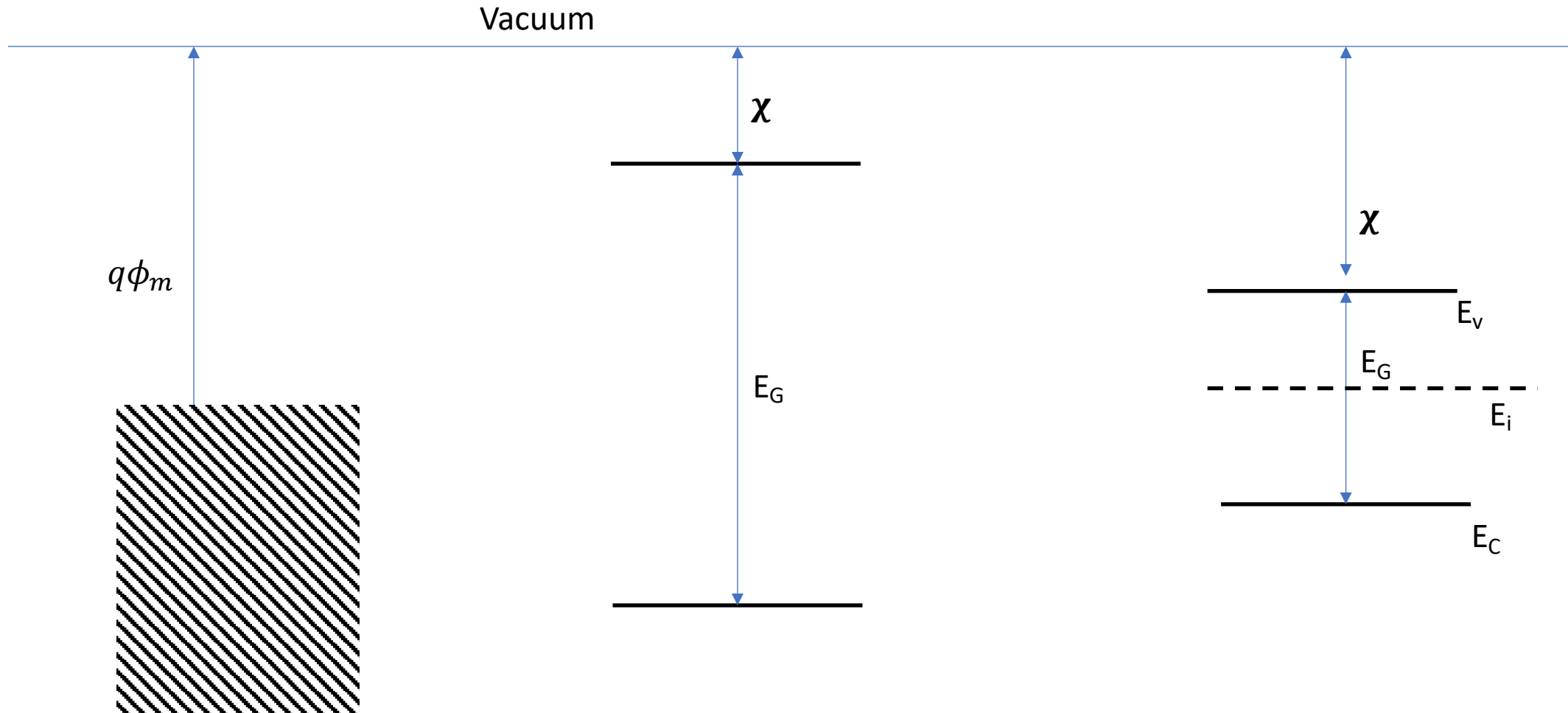


Metal – Insulator - Semiconductors

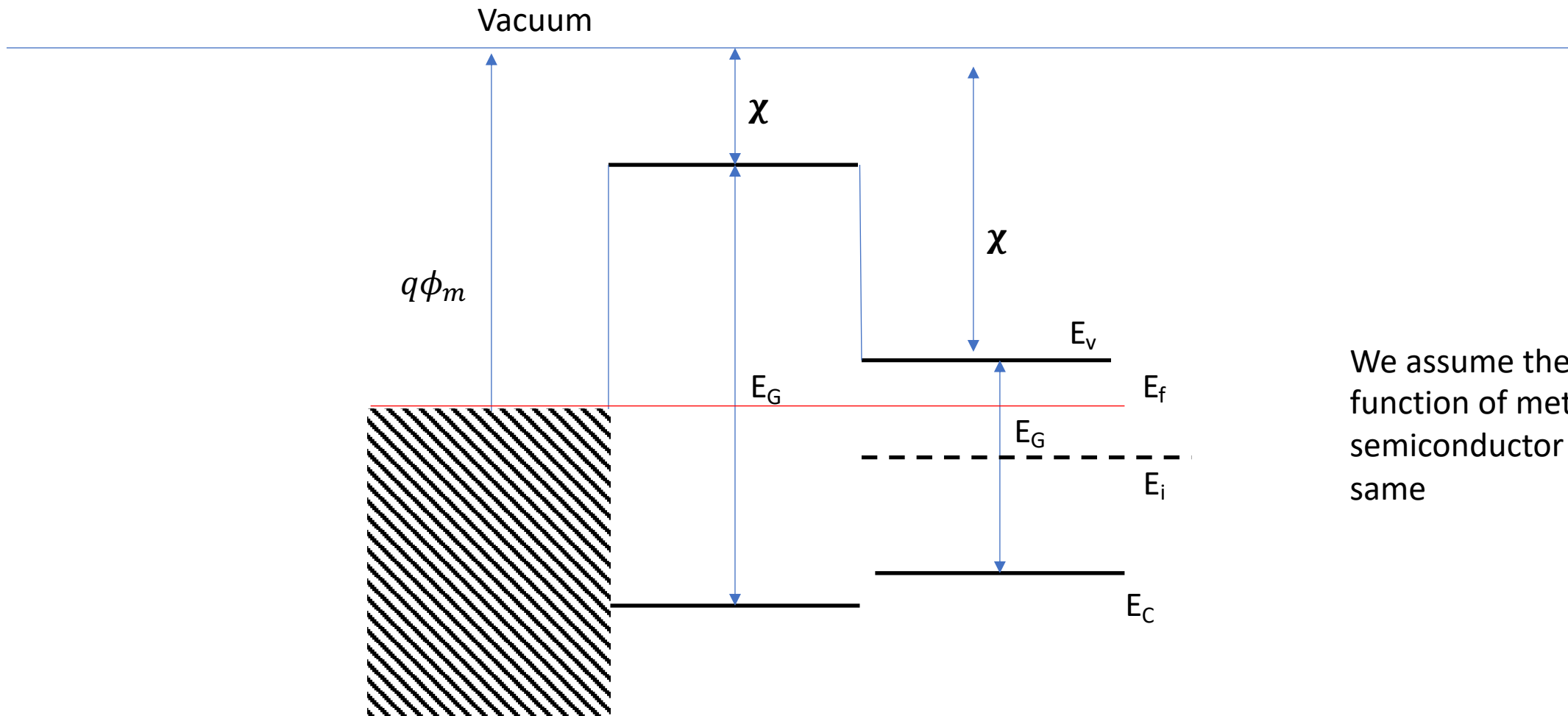
So what happens when we have a large insulator between metal and semiconductor ?



Three materials each have different electronic properties and energy levels

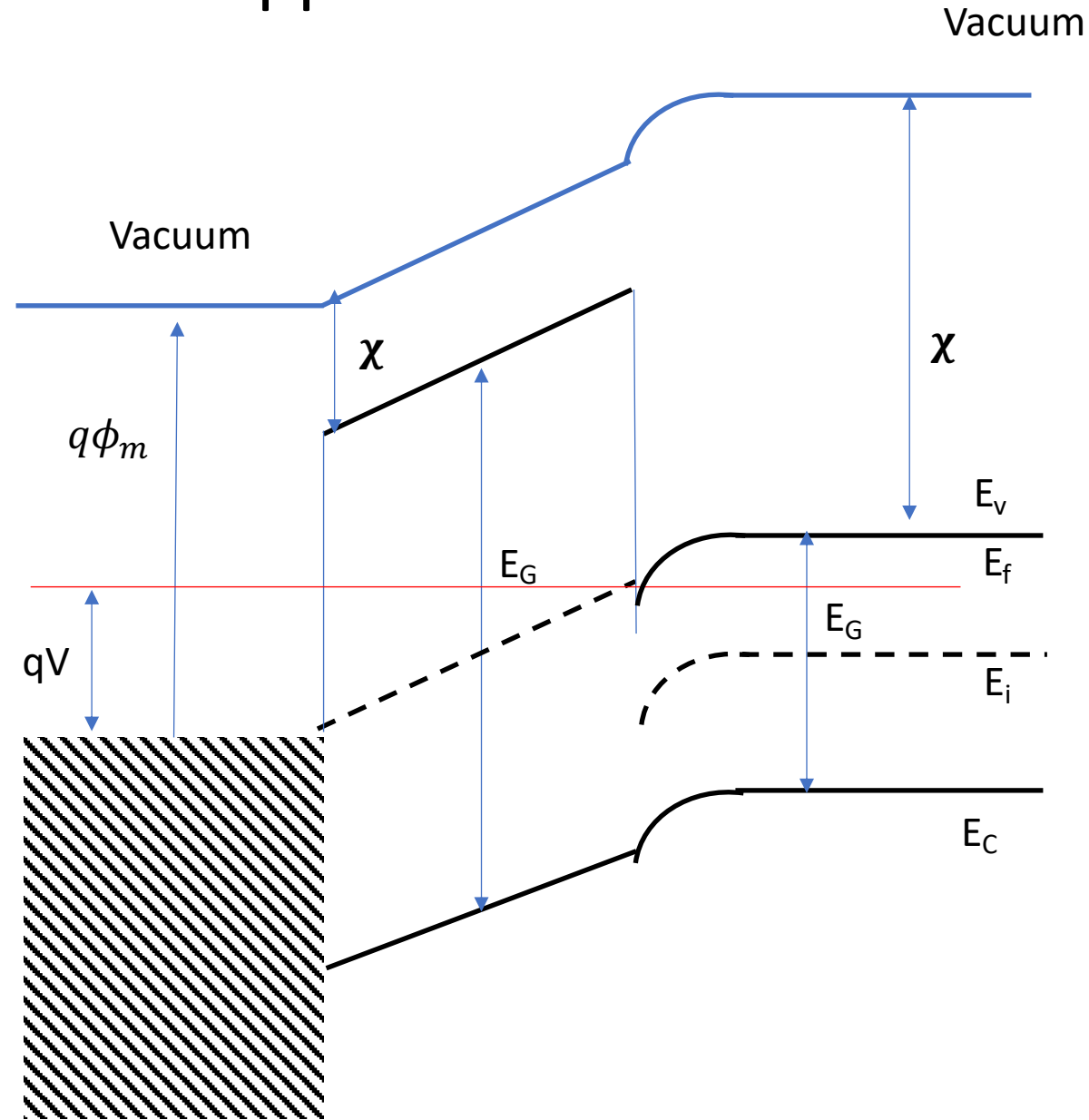
What happens when they are joined ?

The insulator does not allow any current to pass. , So the material is still at thermal equilibrium.



We assume the work function of metal and semiconductor are the same

When a positive bias is applied to the metal:

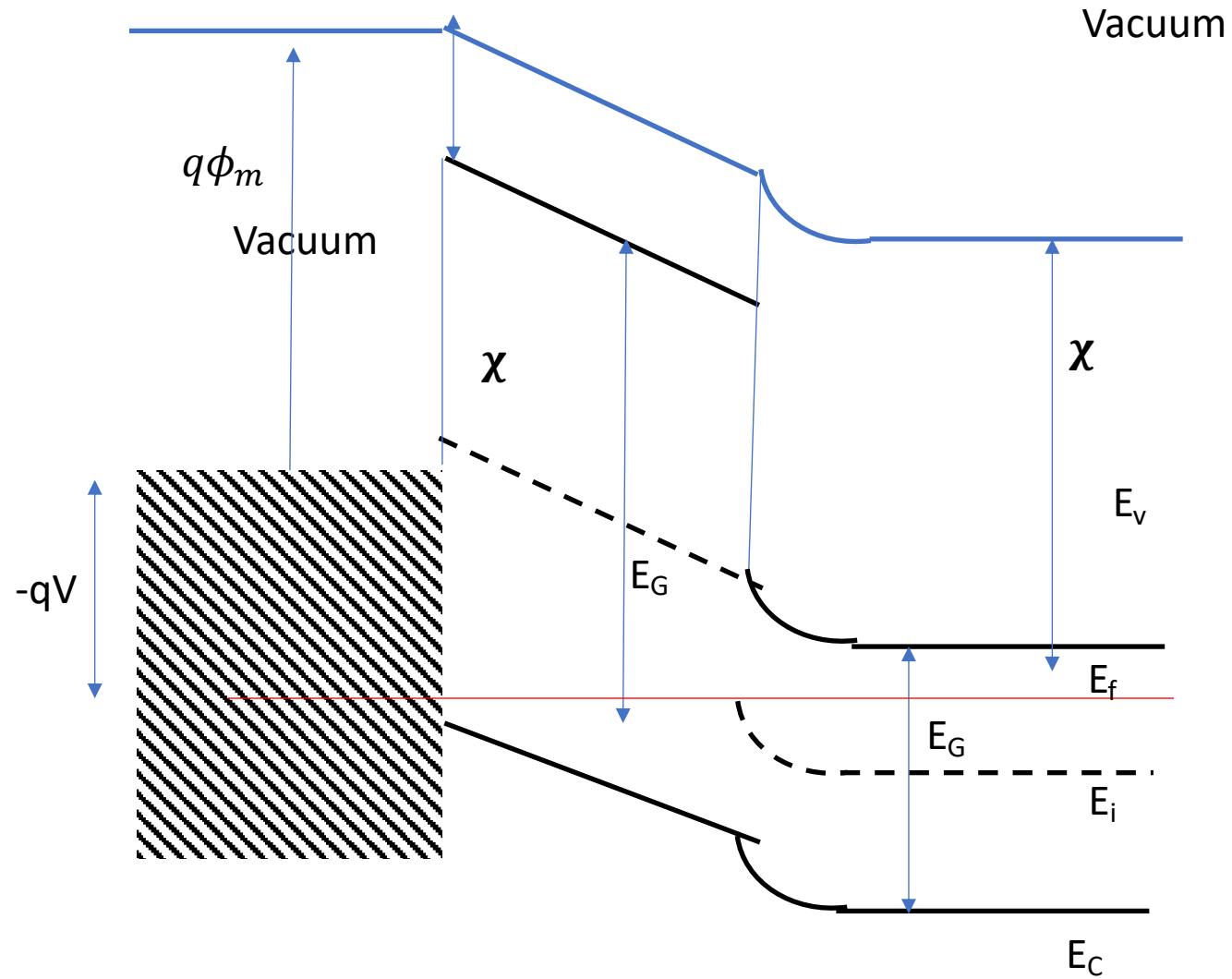


Where ever there is a band bending/slope,
Remember there is an electric field

Electron density at any point:

$$n = n_i e^{(E_F - E_i)/KT}$$

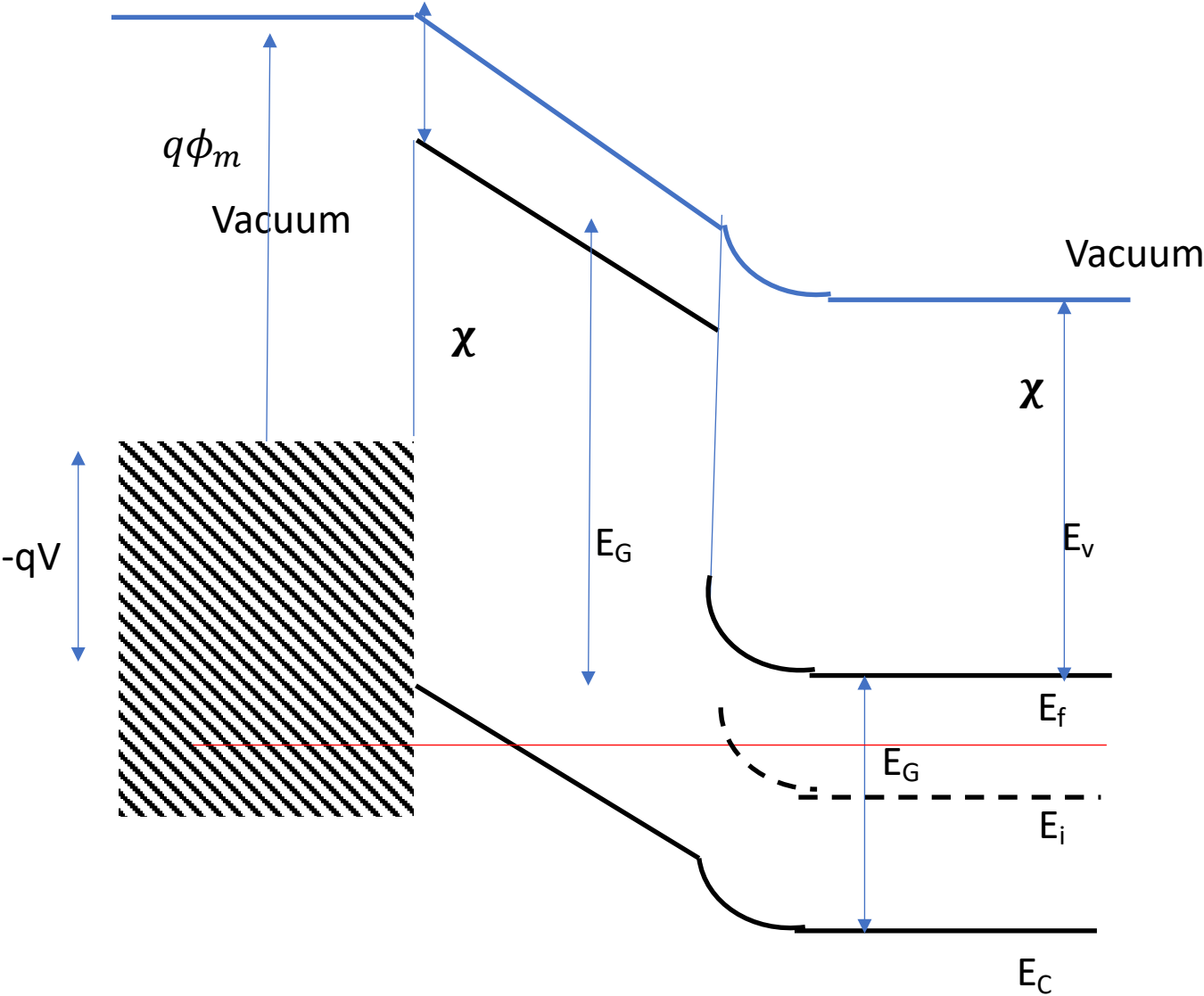
What happens when a negative bias is applied



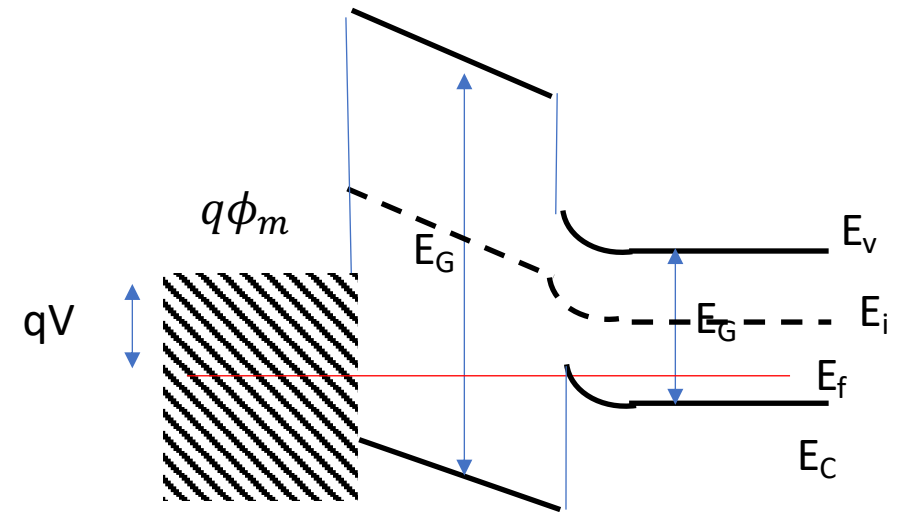
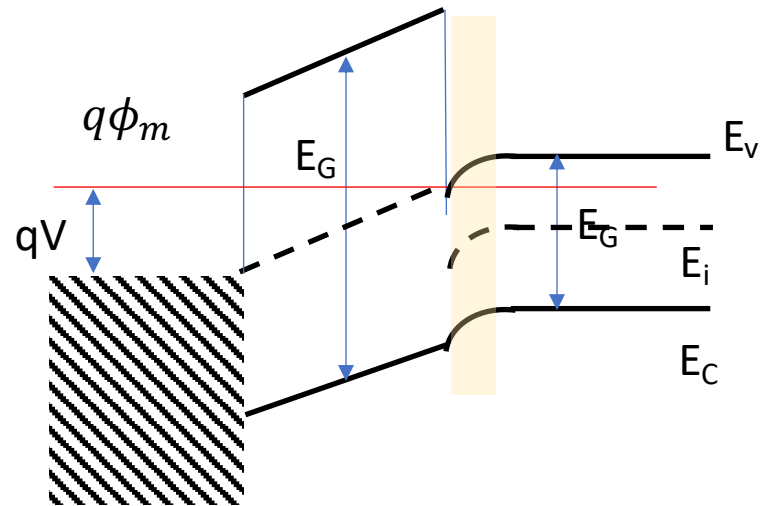
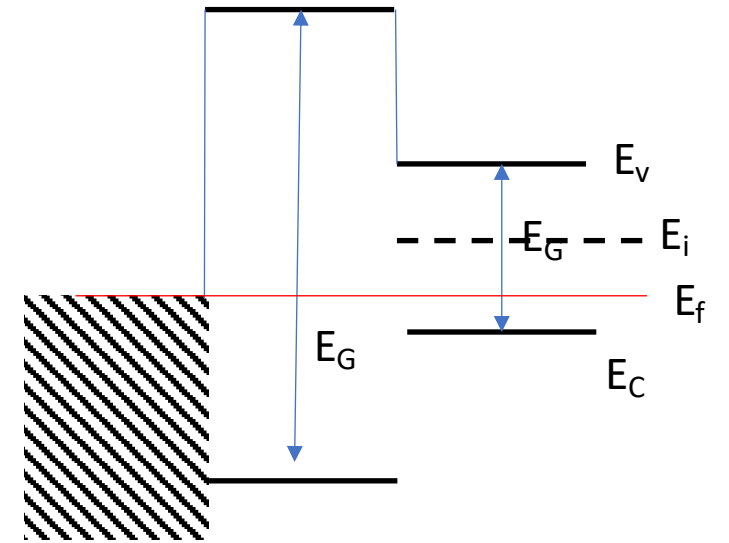
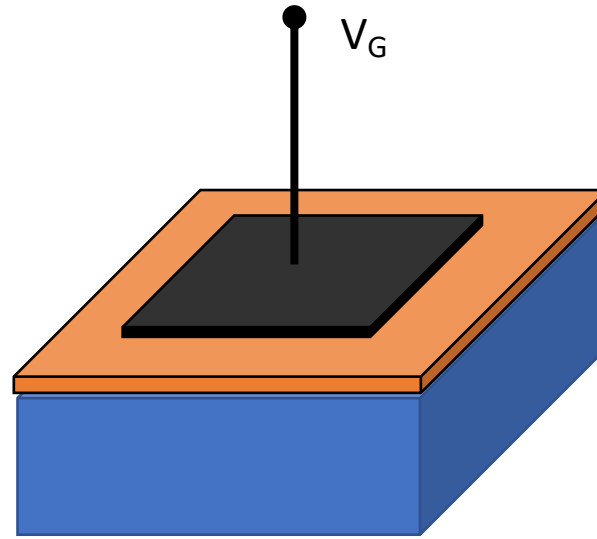
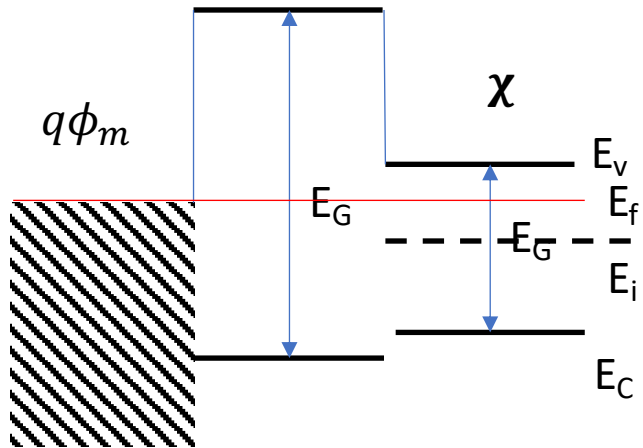
$$p = n_i e^{(E_i - E_f)/KT}$$

At this stage, interface is like intrinsic region

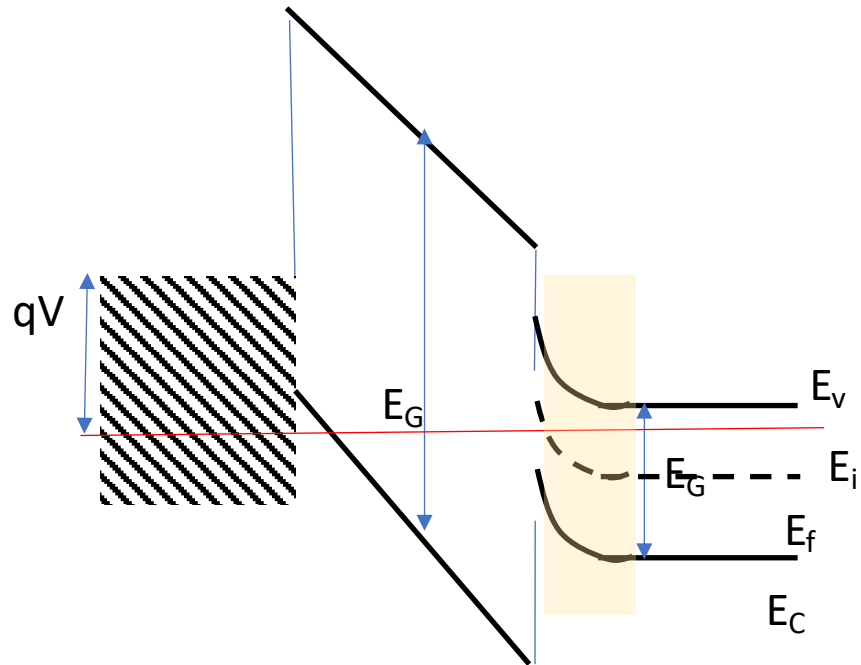
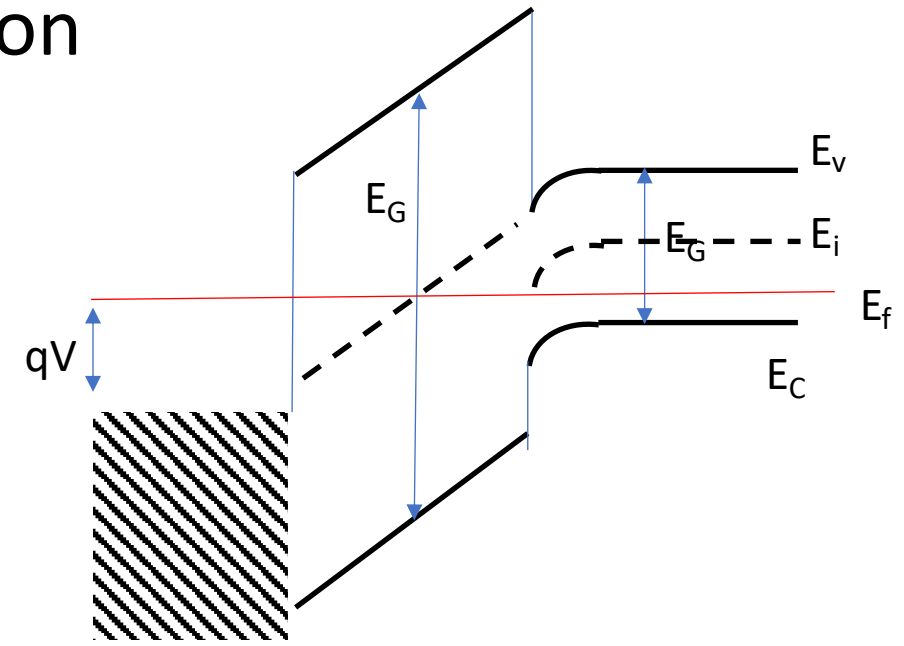
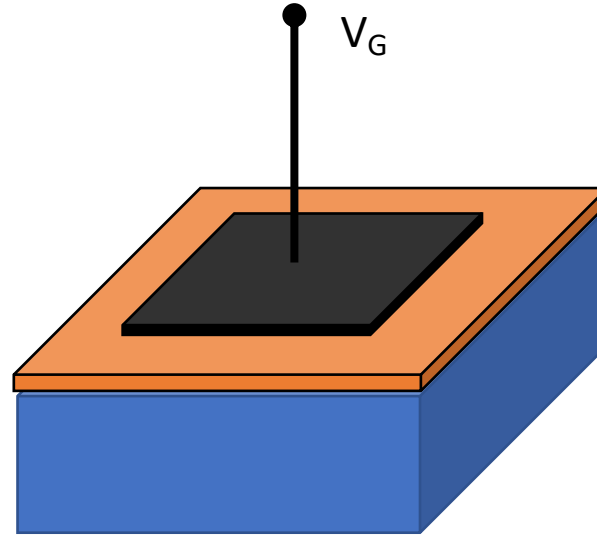
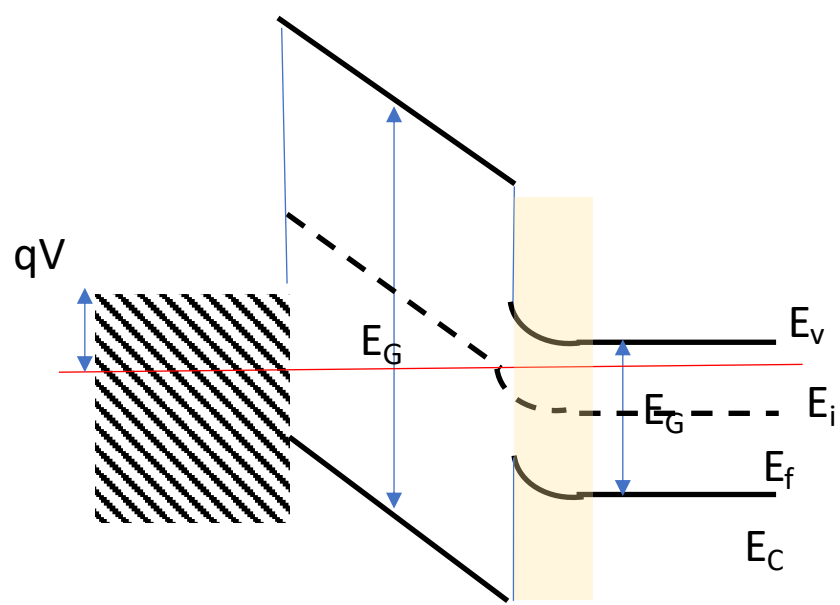
Further increase in negative potential to the metal



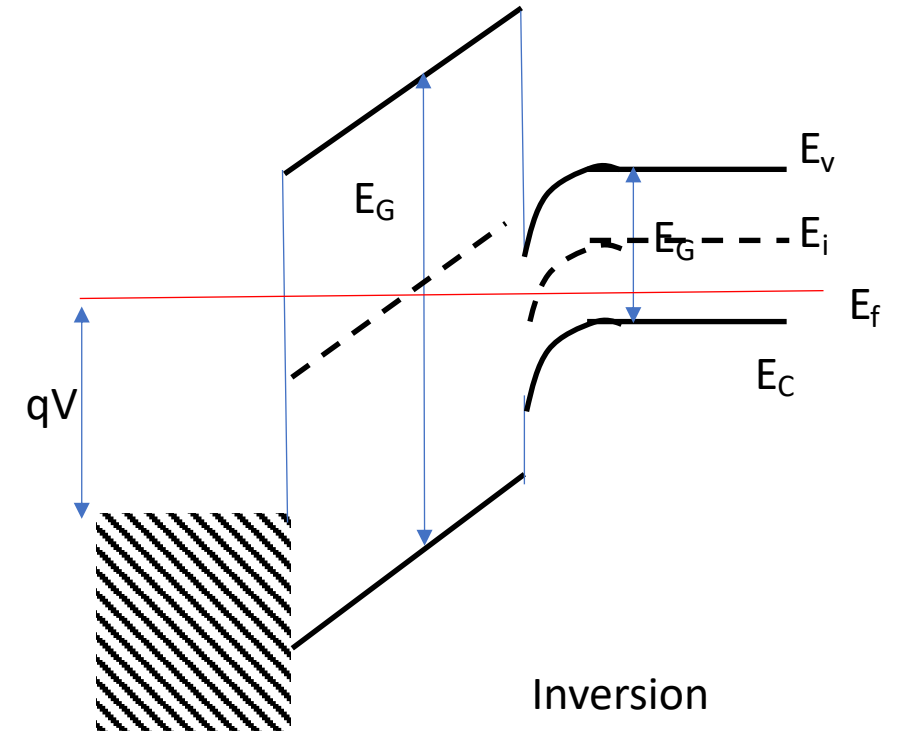
Accumulation



Depletion and Inversion

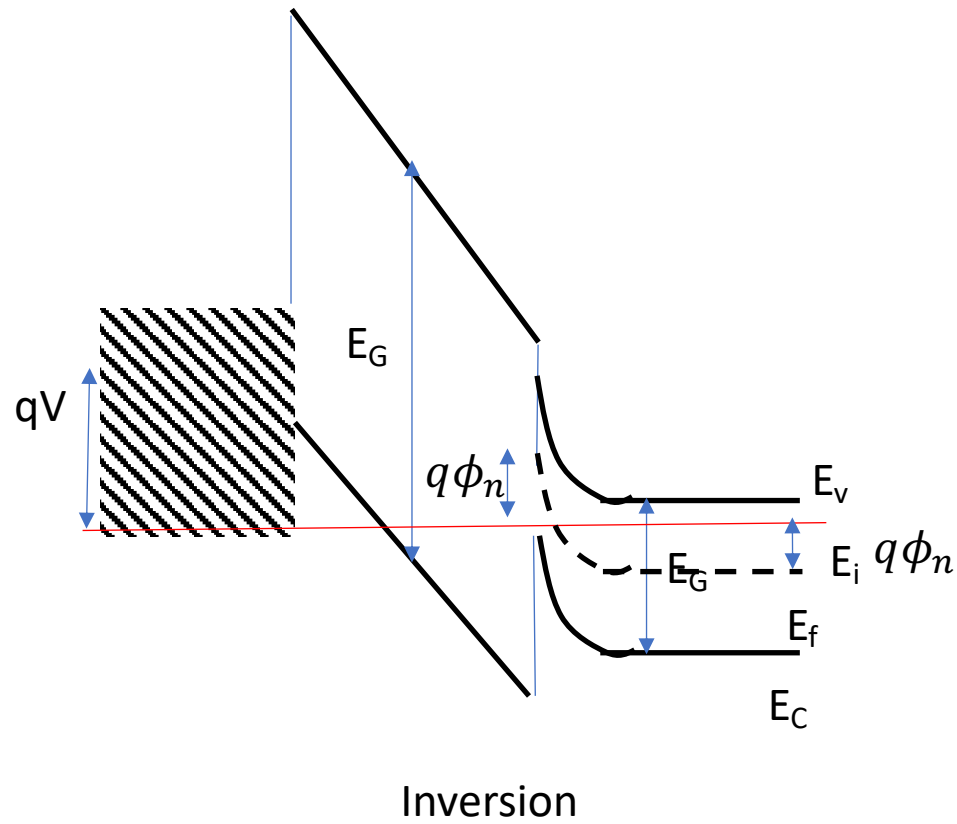


Inversion



Inversion

Strong Inversion



Onset of inversion when

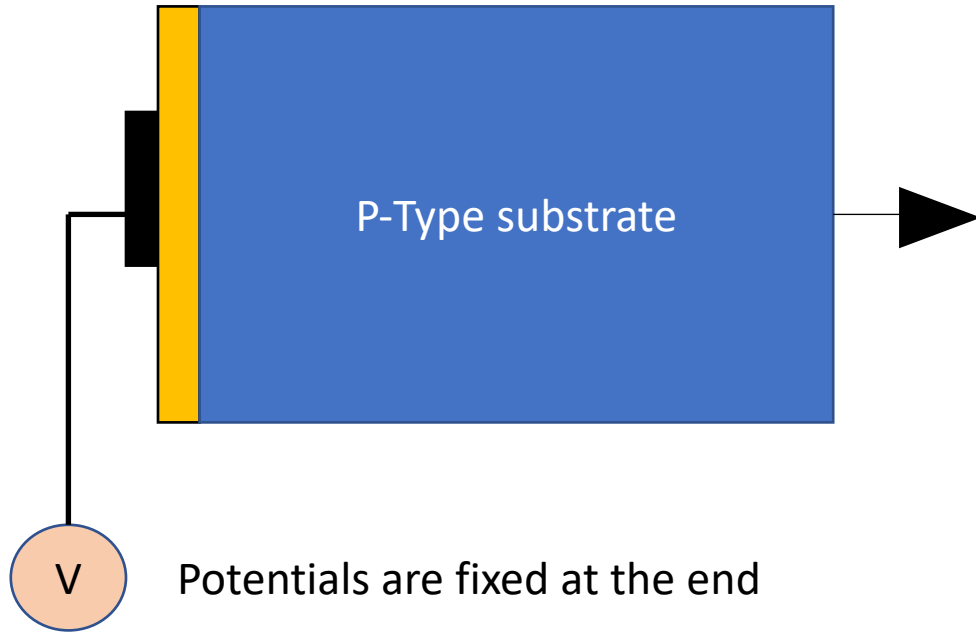
$$E_i \Big|_{bulk} - E_F = E_F - E_i \Big|_{surface}$$

At this stage, the concentration of holes $p = n_i e^{\frac{E_i - E_F}{KT}}$

Is same as the concentration of electrons in the bulk of the n-type semiconductor

The surface is inverted!

Any further increase in potential, will not cause increase in the depletion width, but further accumulation of holes in the surface.



We are still considering the situation, where the workfunction of metal and semiconductor are the same – Flat band assumption

How to find the potential $\Delta\psi$ distribution in the material ?

Poisson's equation

$$\frac{d^2 \Delta\psi}{dx^2} = -\frac{d\mathcal{E}}{dx} = -\frac{\rho}{\epsilon}$$

$$\rho(x) = q[p(x) - n(x) + N_D^+(x) - N_A^-(x)]$$

There are basically two kinds of charge in the semiconductor:

1. Depletion charge
2. Mobile carrier charge

The spatial variation of the potential gives an idea about the charge configuration

Let us take the potential at the surface to be $\psi_S = \Delta\psi(0)$ and the potential at end of bulk to be zero $\psi(x \rightarrow \infty) = 0$

Remember, there are no charges in the insulator.

$$\rho_{ox} = 0 \rightarrow \epsilon_{ox} = \text{constant} \rightarrow \psi_{ox} = Cx$$

Thus the bands in the oxide vary linearly. If the semiconductor surface potential is taken to be ψ_s

$$\text{Then } V_{appl} = \epsilon_{ox}x + \psi_s$$

Remember, bands are energy levels, and the potential at the point E/q

The potential ($\Delta\psi(x)$) at any point is the extent of bending in the bands

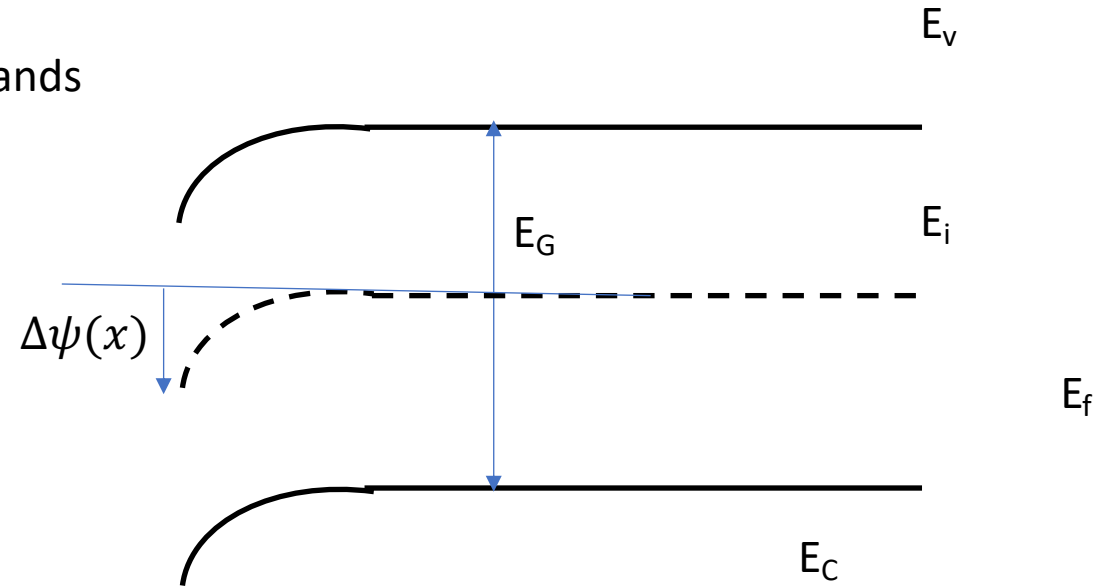
For a p-type material, the hole density is given by

$$p = n_i e^{(E_i - E_F)/KT}$$

Let $q\phi_p = E_i - E_F$ at the bulk

$$N_A = n_i e^{\frac{q\phi_p}{KT}}$$

At any point in x , $E_i(x) = E_i - q\Delta\psi(x)$



Thus, the hole density at any point is given by

$$p(x) = n_i e^{\frac{q\psi_p}{KT}} e^{-\frac{\Delta\psi}{KT}} = N_A e^{-\frac{q\Delta\psi}{KT}}$$

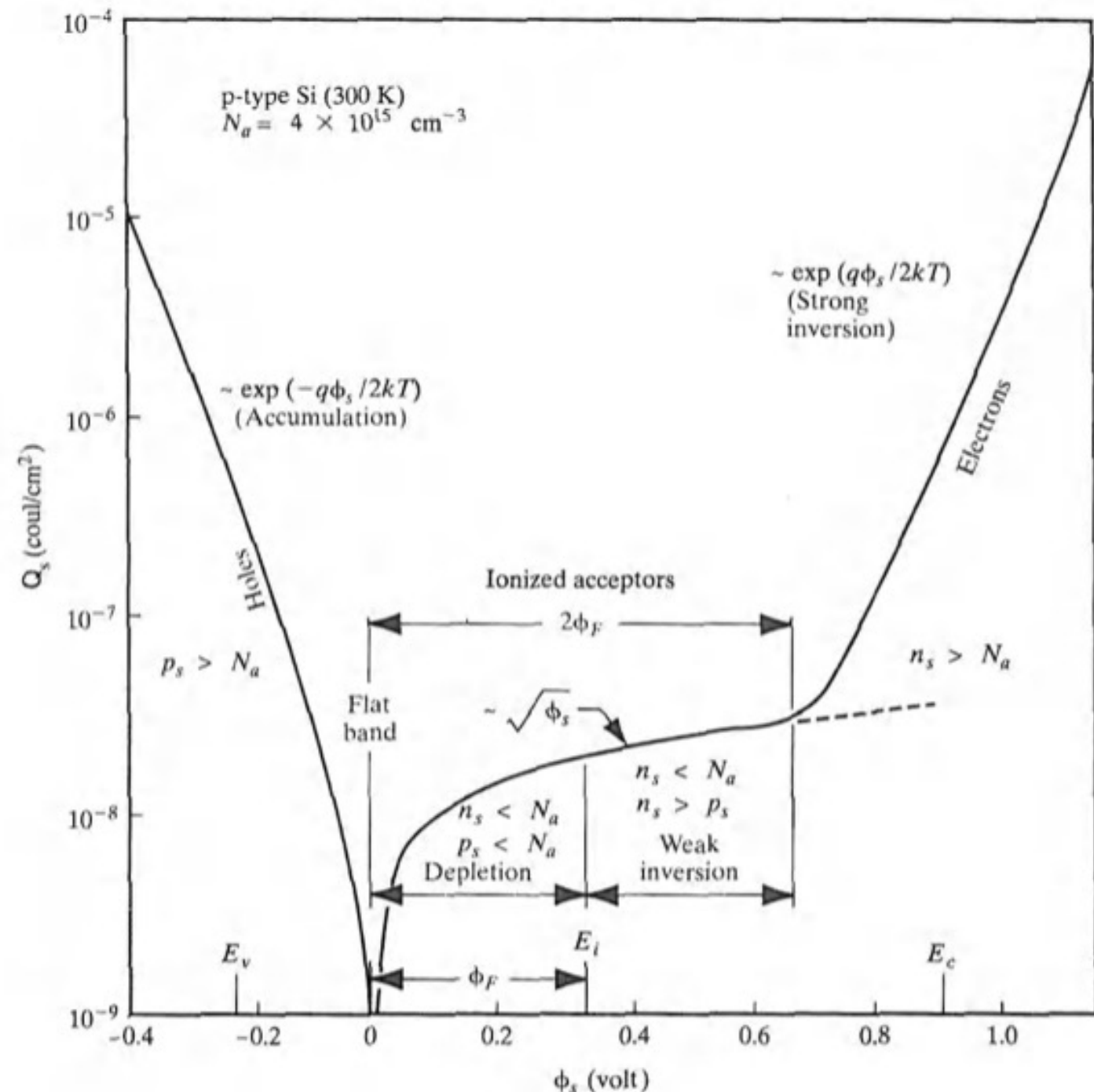
However, remember the law of mass action holds everywhere $n(x)p(x) = n_i^2$

Therefore, the electron density $n(x) = \frac{n_i^2}{N_A} e^{\frac{q\Delta\psi}{KT}}$

$$\rho(x) = -\frac{q}{\epsilon} \left[N_A \left[e^{-\frac{q\Delta\psi}{KT}} - 1 \right] - N_D \left[e^{\frac{q\Delta\psi}{KT}} - 1 \right] \right]$$

Let Q_s be the space charge density $\int \rho_s dx$ over a very small region near the surface.

$$Q_s = -\epsilon \mathcal{E}_s$$



Accumulation :

When a negative potential is applied to the metal, the bands bend in the opposite direction.

$\Delta\psi$ is negative.

$p(x)$ goes exponentially with $\Delta\psi$ and the surface charge density goes as $Q_s \propto e^{-\frac{q\Delta\psi}{2KT}}$ (2KT comes due to integration over space)

The charge density is due to mobile holes, the charges pile up near the interface due to the field on the oxide. Typical accumulation thickness is about ~20 nm from the surface .

The exponential ensures that the band bending $\Delta\psi$ is small, almost pinned to zero for most practical potentials.

Depletion:

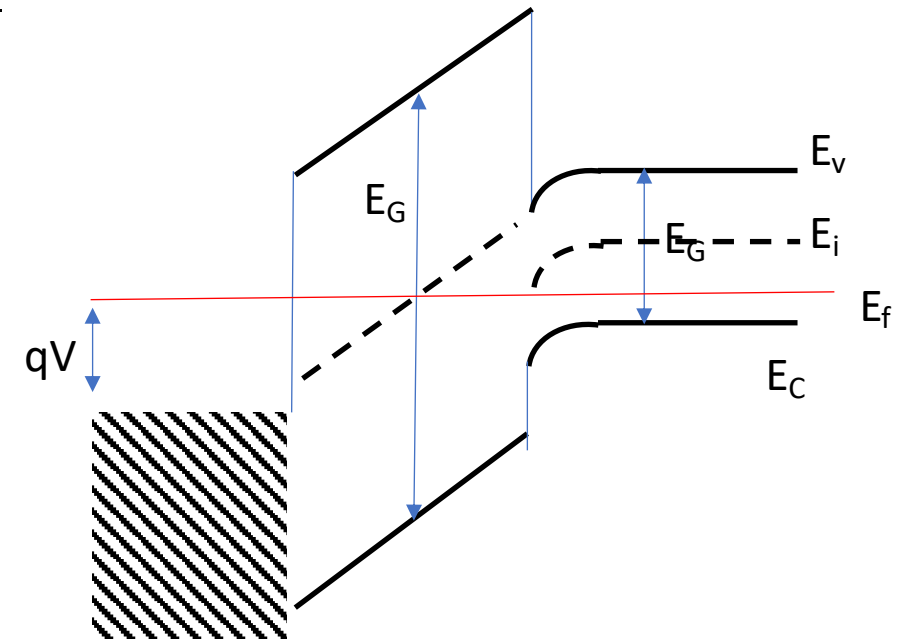
When a small positive potential is applied: $\Delta\psi$ is positive.

The hole concentration is now lower than the bulk hole concentration. The electron concentration is also not large.

This causes depletion at the surface .

The width of depletion region goes as square root of potential $W_D = \sqrt{\frac{2\epsilon\psi_s}{qN_A}}$

The square root dependence on the surface potential can be noted on Qs.



Strong Inversion:

Onset of strong inversion is when electron density is same as the bulk hole density

$$n_s = n(0) = N_A = \frac{n_i^2}{N_A} e^{\frac{q\Delta\psi}{KT}}$$

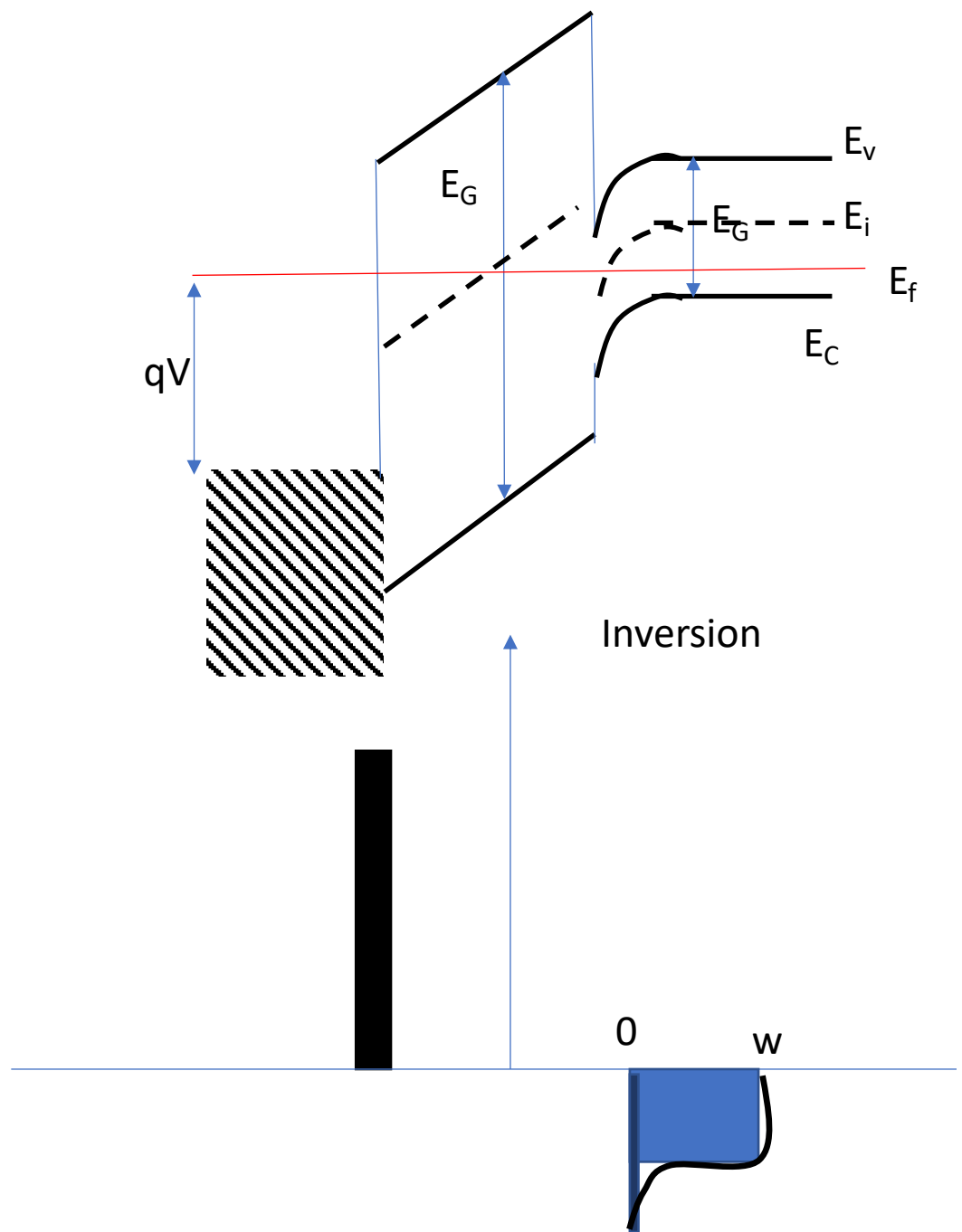
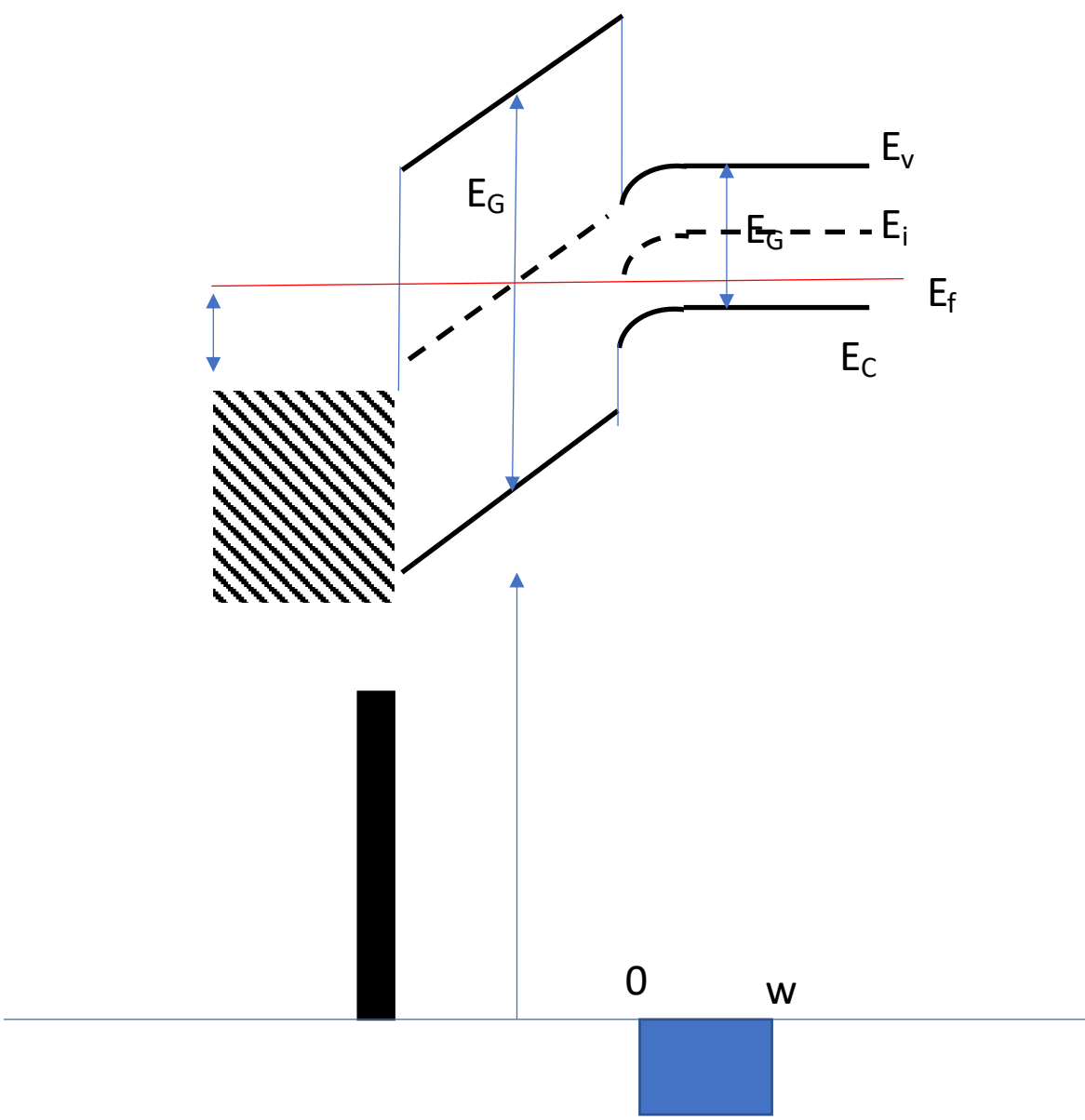
This means, the E_i at the surface is as far away from the Fermi level as the bulk material is, but in opposite direction

$$\Delta\psi = 2\phi_p$$

At the onset of inversion, the semiconductor no longer gets depleted. So, a maximum in depletion width is obtained.

$$\text{Maximum depletion width } W_m = \sqrt{\frac{2\epsilon_s\psi_{sinv}}{qN_A}} = q \left[\frac{\epsilon_s KT \ln\left(\frac{N_A}{n_i^2}\right)}{q^2 N_A} \right]^{\frac{1}{2}}$$

Charges in the material



The total charge in the depletion width $Q_d = -qN_A W_m = -2(q\epsilon_s N_A \psi_p)^{\frac{1}{2}}$

Just before the strong inversion, the surface potential is $\psi_s = 2\psi_p$

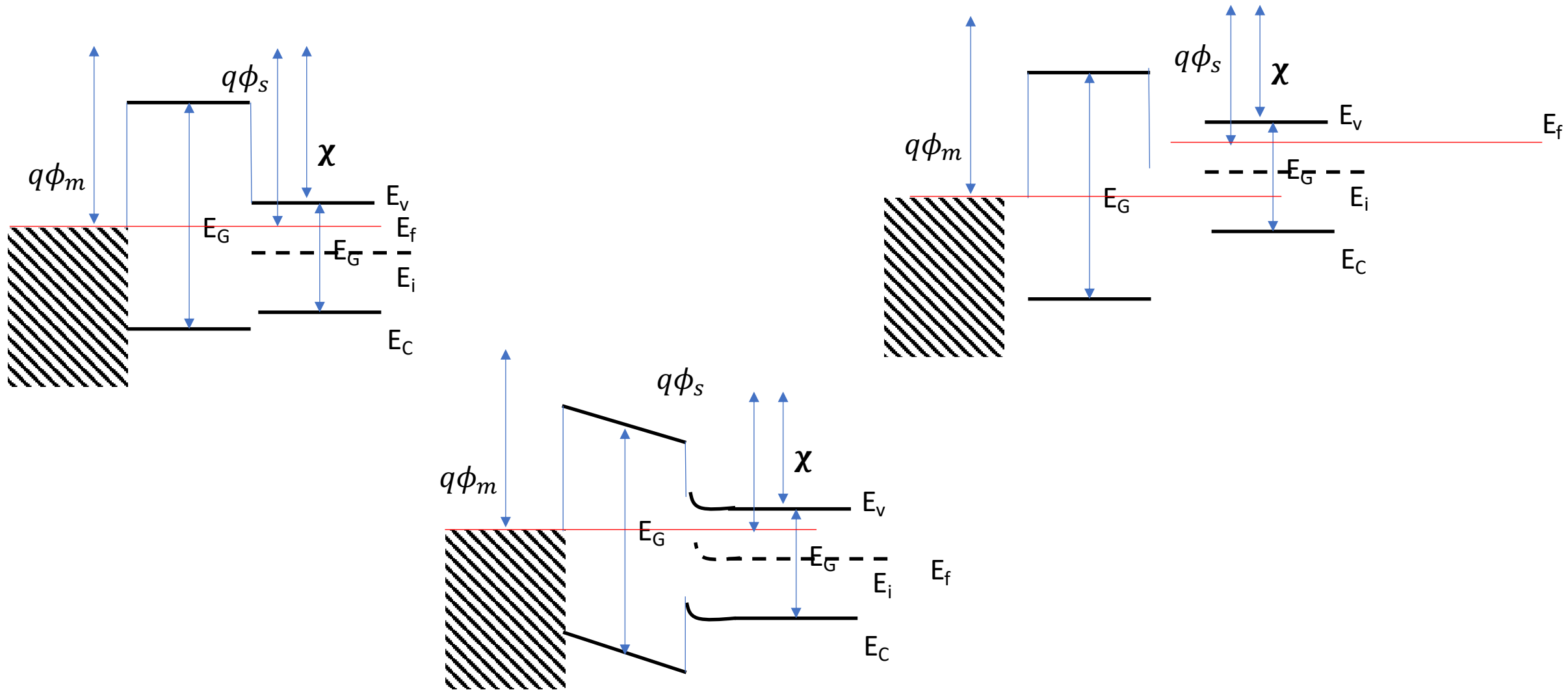
The potential drop across the oxide $\psi_{ox} = -\frac{Q_d}{C_{ox}}$

Therefore, the bias voltage required on the metal to achieve strong inversion $V_T = -\frac{Q_d}{C_{ox}} + 2\psi_p$

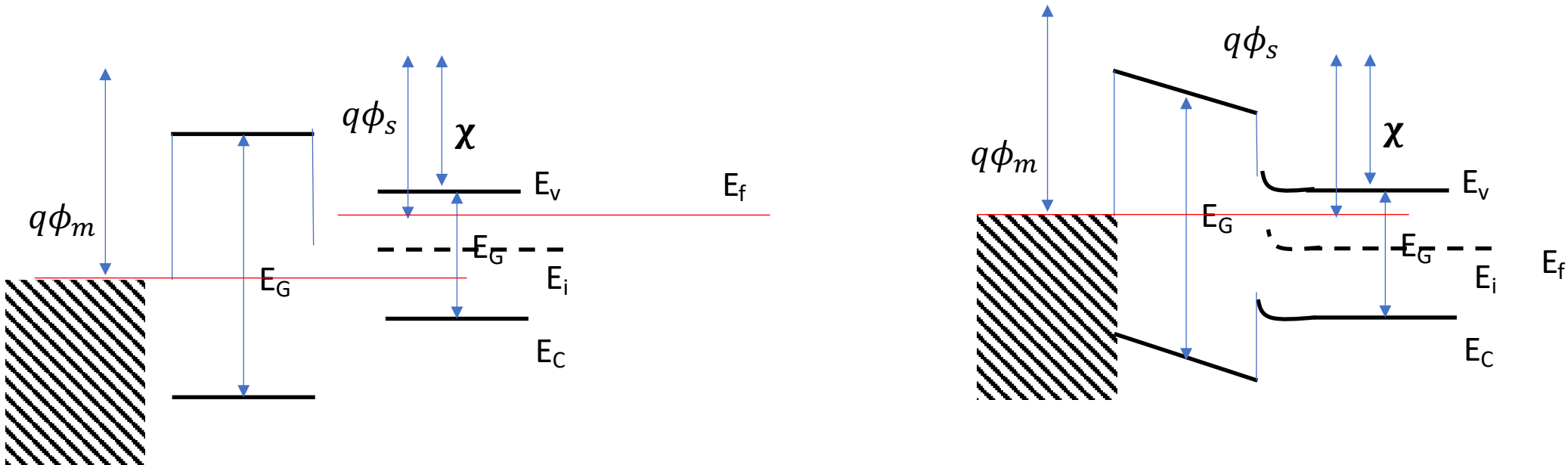
This is an important quality of a Metal-Oxide-Semiconductor interfaces and MOS transistor.

Non-idealities

Work function difference between metal and semiconductor: $\phi_{ms} \neq 0$



Condition to achieve flat band



ϕ_{ms} is positive. Bands bend up to deplete the electrons at the surface.

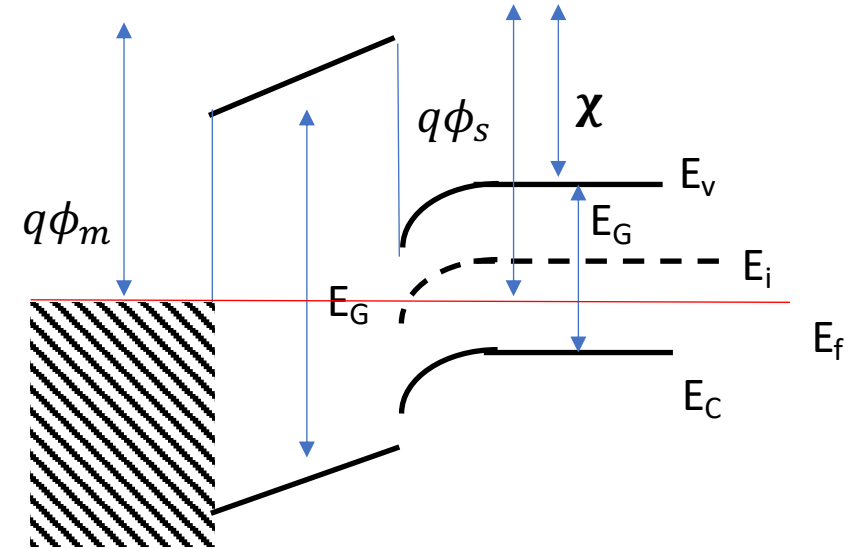
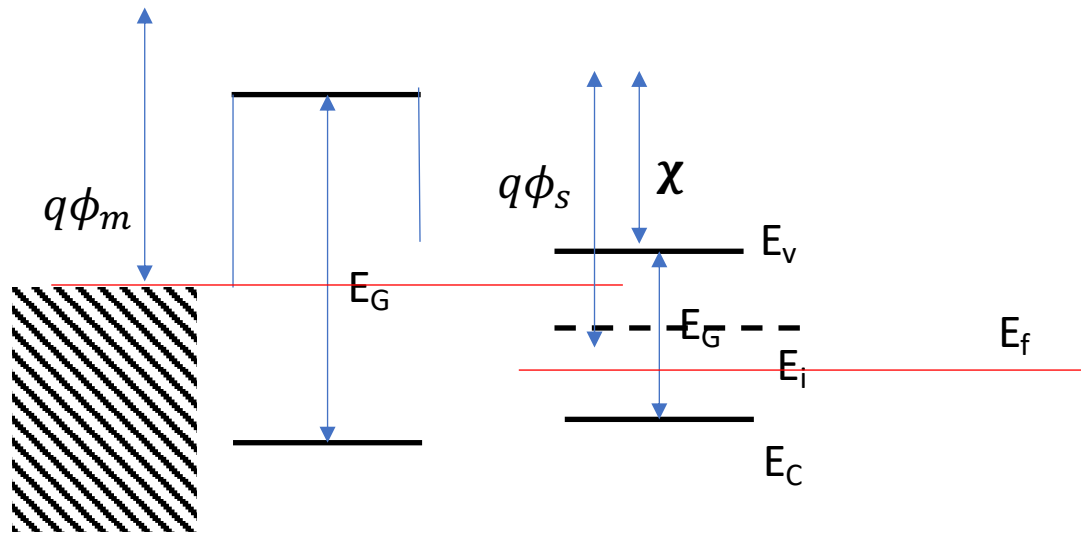
To achieve flat band, the metal Fermi level should be shifted down, with respect to semiconductor Fermi level.

This is achieved by applying a positive potential. $V_{FB} = \phi_{ms}$

Thus the semiconductor is already depleted to begin with.

Infact, when the ϕ_{ms} is sufficiently high, an inversion layer can exist even without application of external bias!

What happens on the other side:



When ϕ_{ms} is negative ?

It is clear, the Fermi level of the metal needs to be pushed up,
To obtain flat band. A negative potential on the metal will push it up

So $V = F_{FB} = \phi_{ms}$ is required to achieve flat band!

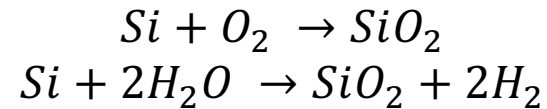
Effect of oxide charge density

Formation of junctions: Example Metal – Insulator – Semiconductor Junction

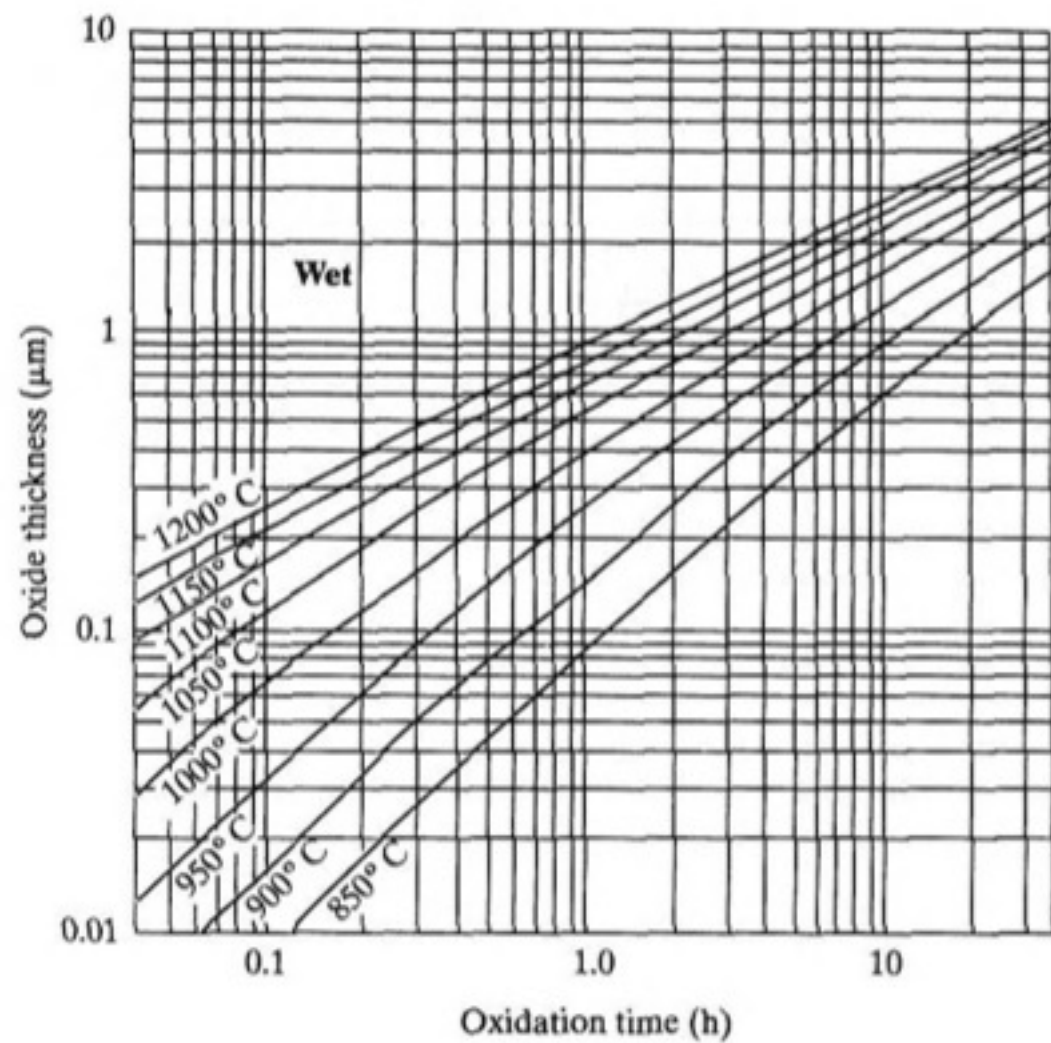
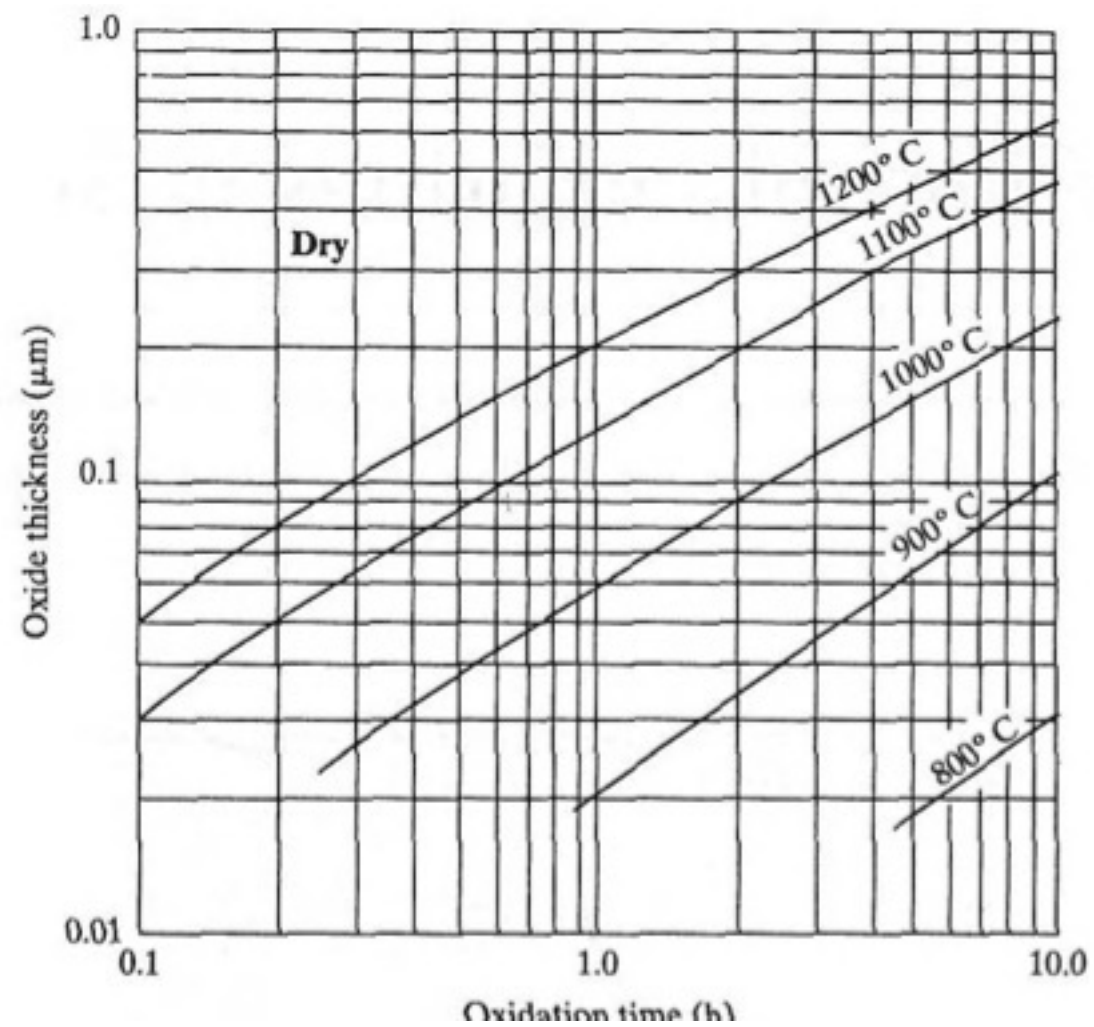
Thermal oxidation: “The main reason for dominance of Si is the existence of a stable oxide and good Si-SiO₂ interface.”

Most common technique to form oxides – Thermal oxidation.

1. Batch of wafer are placed in Quartz boats inside a quartz tube.
2. Tube heated to about 800 – 1000 °C in a furnace.
3. Oxide is grown on top of Si using two techniques (dry O₂ gas or steam)



4. In both cases, Si at the surface is consumed and oxide layer is formed.
5. For every μm of SiO₂ grown, 0.44 μm Si is consumed. 2.2 times the volume of Si consumed is obtained as SiO₂ layer.



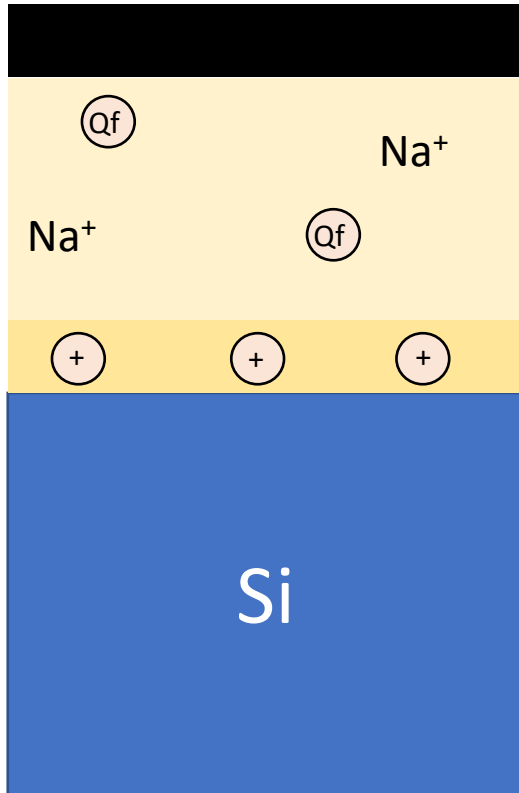
Bulk oxide charge densities

Most common contaminant in furnaces – Alkali metals

They tend to introduce positive charge densities in the bulk of oxides .

The effect of the ion charges depends on the position and the density.

The alkali ions are very small and mobile. They are influenced by the gate field as well as by the other drain-source potentials



Interfacial charge densities

An ideal interface is formed when all the Si atoms at the surface is coordinated right

However, it does not happen and some Si atoms at the interface remain as Si,

Leading to positive interface charge densities. [Remember the way SiO₂ is grown]

All the bulk and interface charge densities are typically positive.

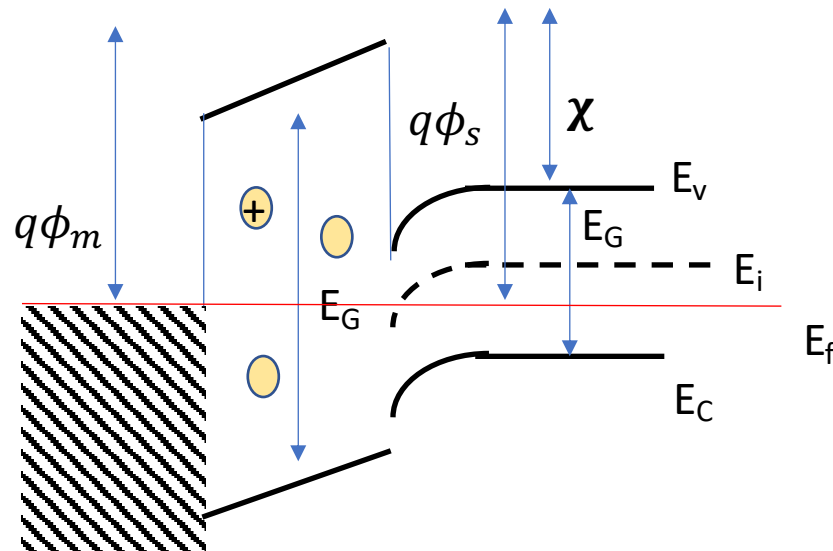
Generally, all the oxide charges are taken into a single term $Q_{ox} = Q_f + Q_{it}$

The effect of this positive charge density is to introduce field in the oxide, which attracts electrons in the semiconductor.

This will make the bands in the semiconductor to bend down.

To make these bands flat, a negative voltage is typically required to make a flat band.

-negative sign of Q_{ox} is because the charges are taken to be positive and a negative potential is required to remove the excess electrons accumulating at the interface



Thus the total potential required for flatband

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

The threshold voltage:

$$V_T = V_{FB} - \frac{Q_D}{C_{ox}} + 2\phi_p$$

The potential at the gate should first offset

1. non-ideality [Flat band potential]
2. Deplete the carriers at the interface
3. Invert the surface
4. Generate enough carriers to match the bulk majority carrier density

Let us take an example problem:

What potential is required to invert a P-type Silicon surface with doping density $5 \times 10^{15} \text{ cm}^{-3}$ with an interface trap charge density $4 \times 10^{10} / \text{cm}^2$. Assume oxide is 10 nm thick.

We should first assume metal and semiconductor work functions are the same.

$$\text{Oxide capacitance } C_{ox} = \frac{\epsilon_{Si}}{10^{-6}} \frac{F}{\text{cm}^2} = 3.9 * 8.85 * \frac{10^{-14}}{10^{-6}} = 3.45 * 10^{-7} \text{ F/cm}^2$$

$$\text{The flat band potential } V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} = - \frac{4 * 10^{10} * 1.6 * 10^{-19}}{3.45 * 10^{-7}} = 0.019 \text{ V}$$

The Fermi level is below the Intrinsic level is given by

$$\phi_p = \frac{kT}{q} \ln \frac{N_A}{n_i} = 0.026 * \ln \frac{5 * 10^{15}}{1.5 * 10^{10}} = 0.329 \text{ eV}$$

Maximum width of the depletion before strong inversion

$$W_m = 2 \sqrt{\frac{\epsilon \phi_p}{q N_A}} = 0.415 \text{ } \mu\text{m}$$

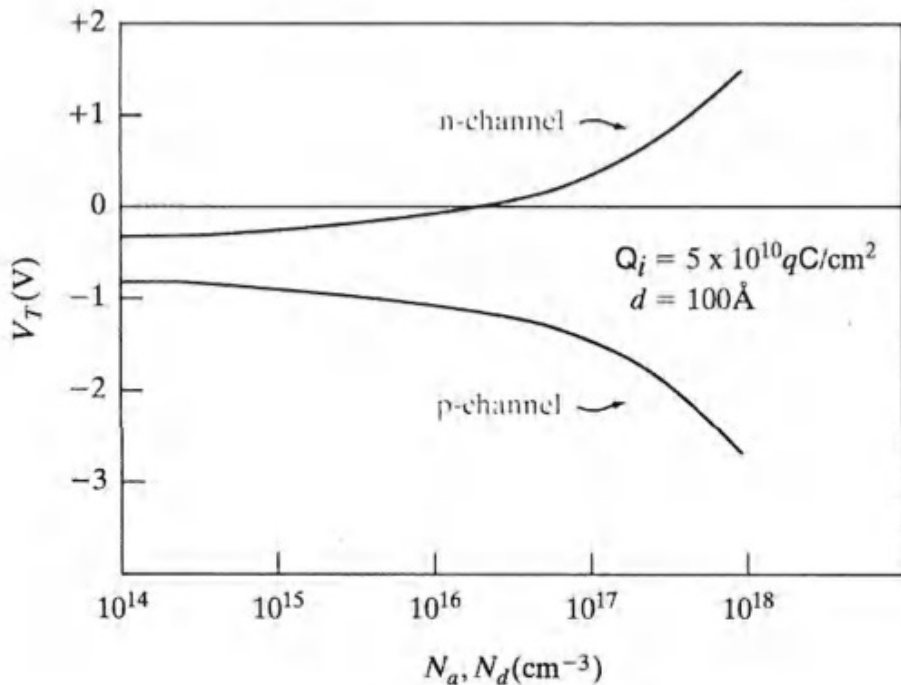
The total charge in the depletion

$$Q_D = -qN_A W_m = -1.6 * 10^{-19} * 5 * 10^{15} * 4.15 * 10^{-5} = -3.32 * 10^{-8} \text{ C/cm}^2$$

The total threshold potential

$$V_T = V_{FB} - \frac{Q_D}{C_{ox}} + 2\phi_p$$

$$V_T = -0.010 + 0.658 + 3.32 * \frac{10^{-8}}{3.45 * 10^{-7}} = +0.74 \text{ V}$$



Variation of threshold voltage for different doping density
- Onset of strong inversion.

1. Negative threshold voltage for p-type means, you need to apply the potential to invert
2. Negative threshold voltage for n-type means, even in the absence of gate potential, the surface is inverted.
3. This means, the channel is normally conducting! We will soon see such situations are bad for device applications

Capacitance measurements

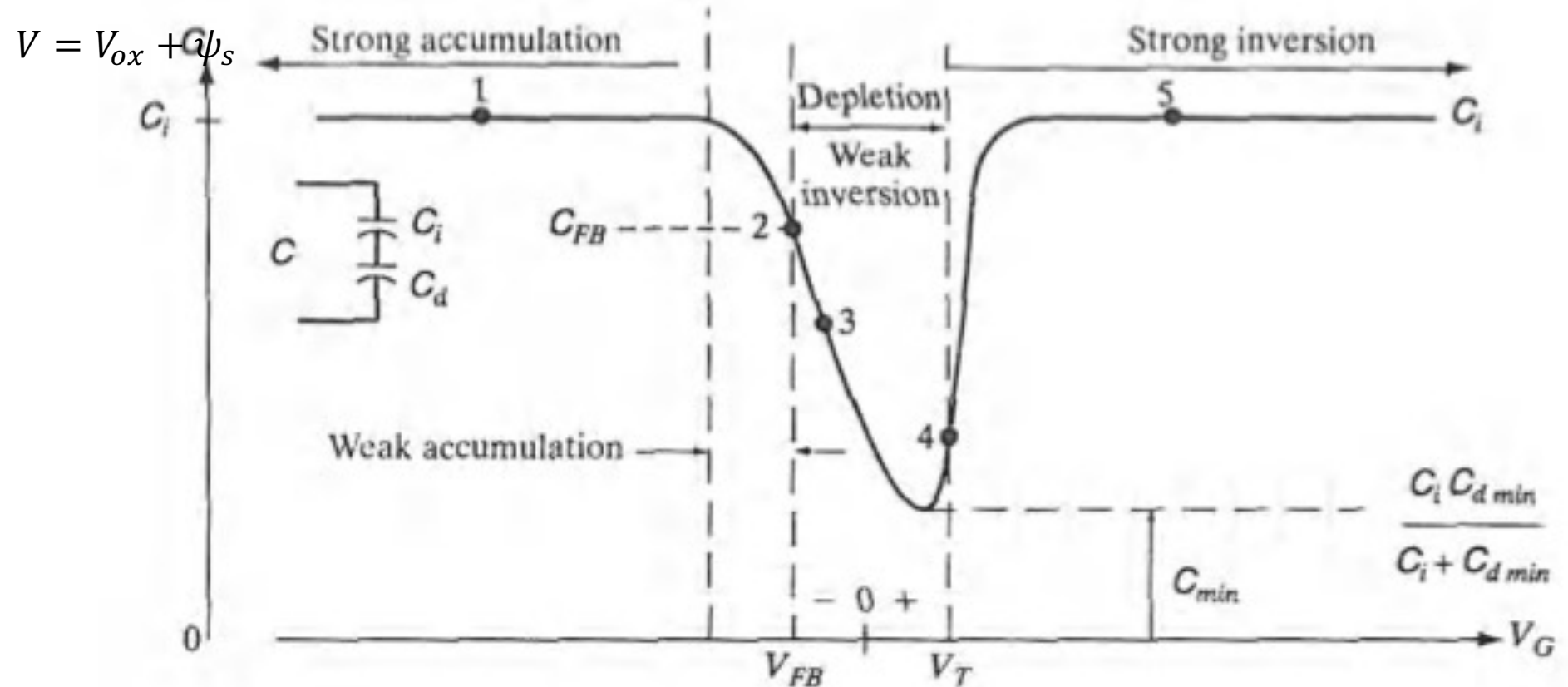
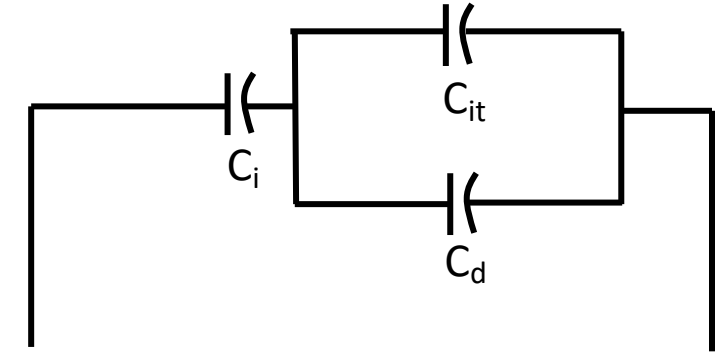
MOS Capacitor

There are different charge distribution in the semiconductor:

1. Mobile charges localized at the interface
2. Fixed charge density in the insulator
3. Depletion charge near the interface

The total potential is distributed across the oxide and the semiconductor

Equivalent circuit



Realistic case: MOS – CV measurement:

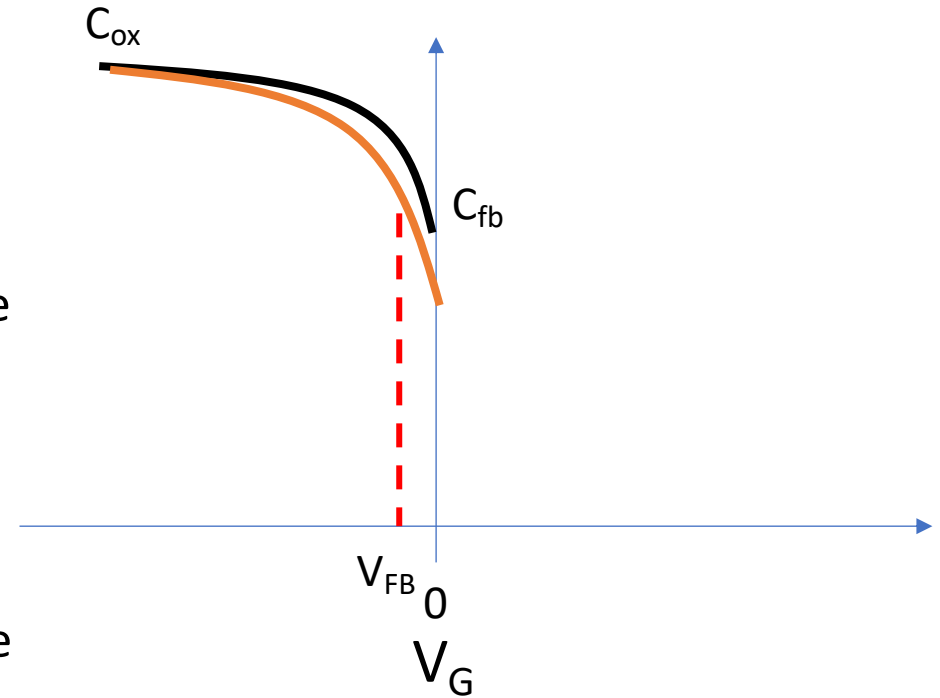
For a Ptype substrate:

1. A negative potential will cause accumulation.

1. If you assume flat band condition, for small positive potentials, there is a small depletion near the interface due to charge screening. The length of depletion is related to the screening length/Debye length (distance by which charge inhomogeneities are screened. We have weak accumulation

$$C_T = \left[\frac{1}{C_{ox}} + \frac{1}{C_D} \right]^{-1}$$

1. Further increase in negative potentials will lead to large hole concentration at the surface that cannot be screened. The only capacitance that is left is now the oxide capacitance. We have strong accumulation
2. If the non idealities are considered, the bands can bend even further, leading to lower total capacitance



The insulator capacitance

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}}$$

Is the maximum capacitance in the structure.

At positive gate biases, the surface gets depleted.

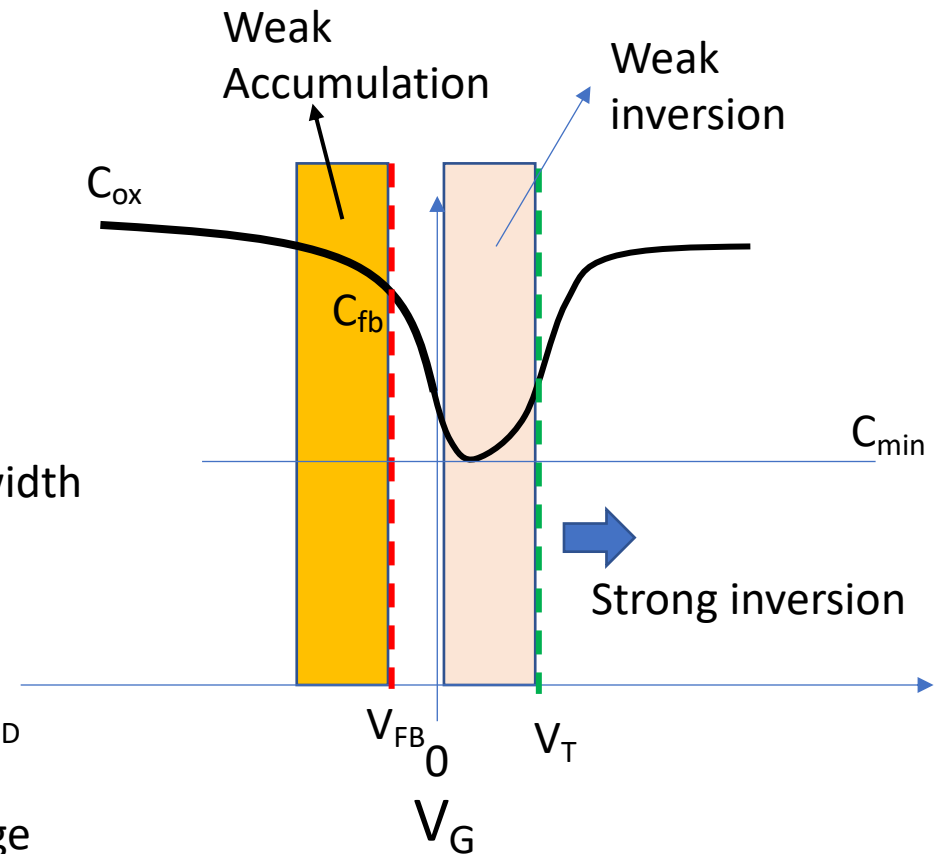
The minimum capacitance is obtained at the maximum depletion width

$$C_D^{min} = \frac{\epsilon_{si}}{W_D^{max}}$$

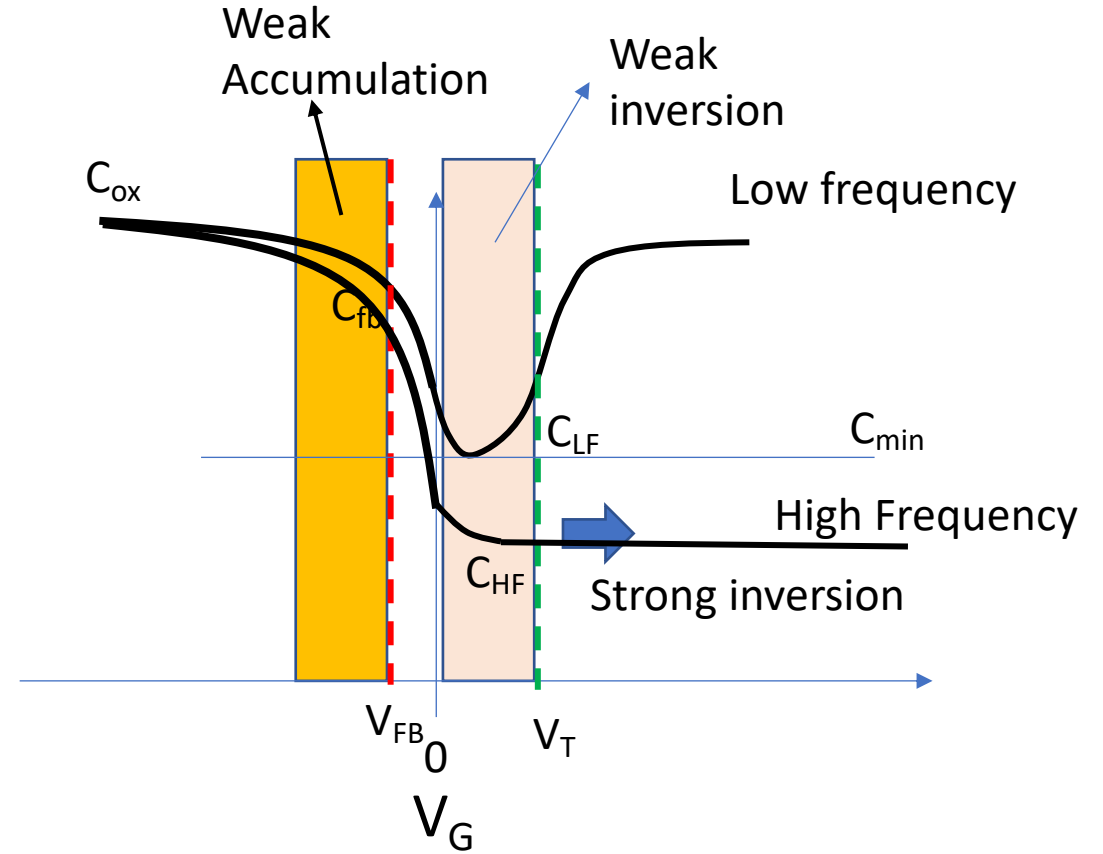
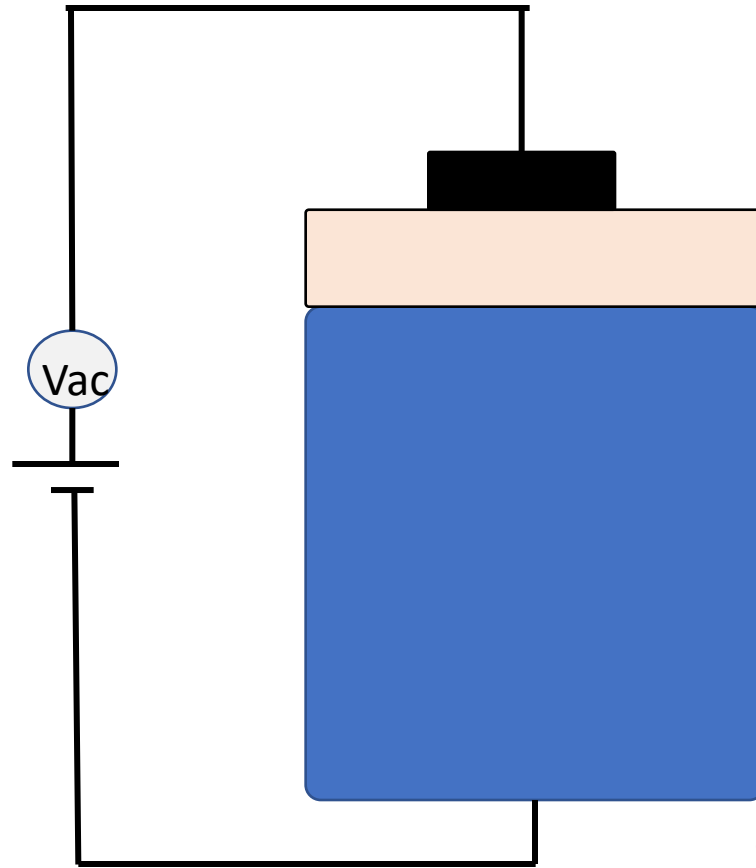
The total capacitance $C_T = \frac{C_{ox}C_D}{C_{ox}+C_D}$ will be strongly determined by C_D

Remember, Threshold voltage is when the surface is inverted: charge density at surface is same as the bulk charge density.

Therefore, V_T is not obtained when capacitance is minimum, rather, V_T is obtained when the C_{ox} is in series with $2C_D$



Effect of measurement frequency



Two observations at difference between the frequencies:

1. The minimum capacitance is lower in HF
2. Absence of strong inversion at high frequency

Lower $C_{\min}$ at high frequency:

Interface trap sites can be segregated into fast and slow responding traps sites.

Since each trap site captures charges and screens the potential, there is no need to deplete the semiconductor further.

Thus, fast traps allow for lower depletion width in the semiconductor and hence higher overall capacitance.

However, there are always slower traps sites, whose density increases with increasing measurement frequency. Thus, under such measurements, the depletion width is higher and hence an overall lower capacitance $C_{\min}$ is measured.

The measure of fast trap charge density

$$D_{it} = \frac{1}{q} \left[\frac{C_{ox} C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox} C_{HF}}{C_{ox} - C_{HF}} \right] \text{ cm}^{-2} \text{ V}^{-1}$$

Lack of strong Inversion

Actual measure of capacitance is $C = dQ_{ac}/dV_{ac}$

This measurement is conducted at different DC bias potentials.

When close to strong inversion, for a small dV_{ac} the questions is do we accumulate minority carriers at the interface, or deplete the channel further.

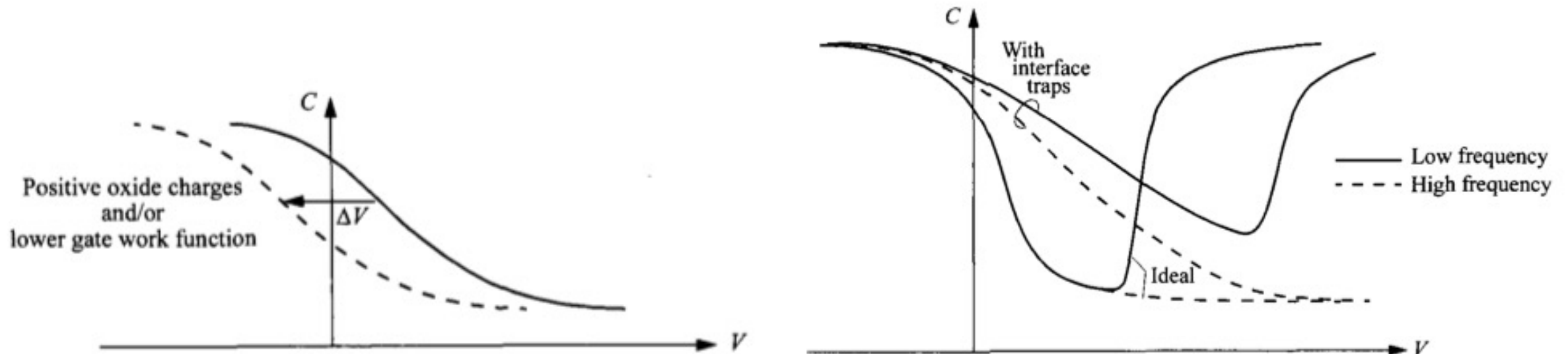
The minority carrier accumulation at the oxide interface requires thermal generation of electrons, deep depletion of holes at the interface is required to increase the electron density at the interface.

These things require time and depends on the the carrier lifetime and mobility.

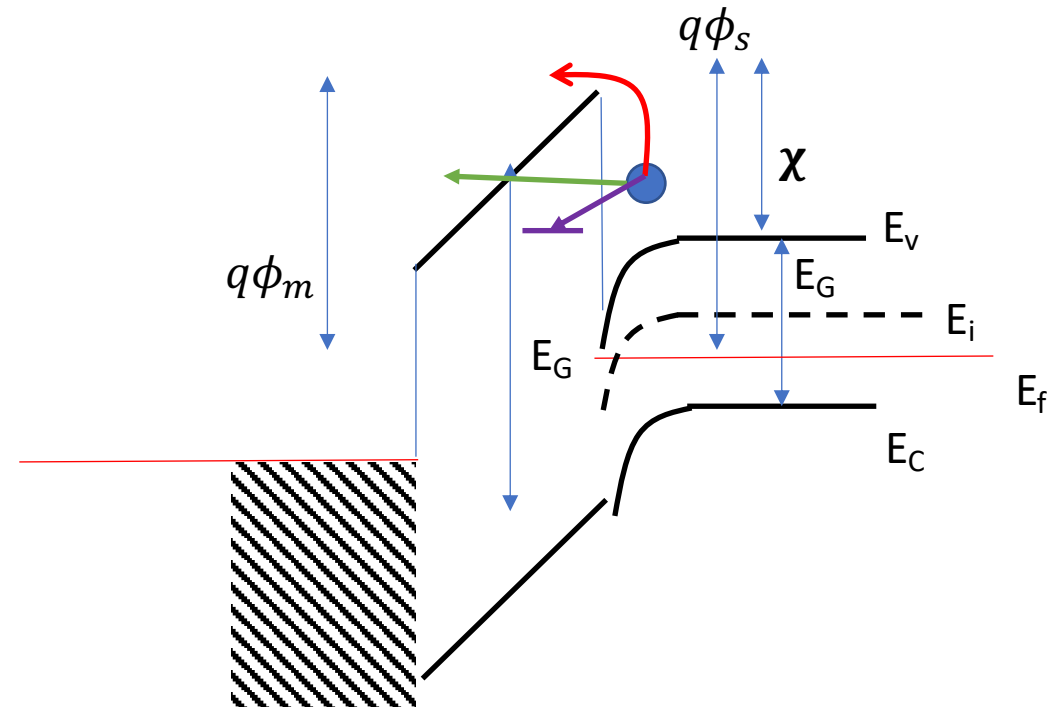
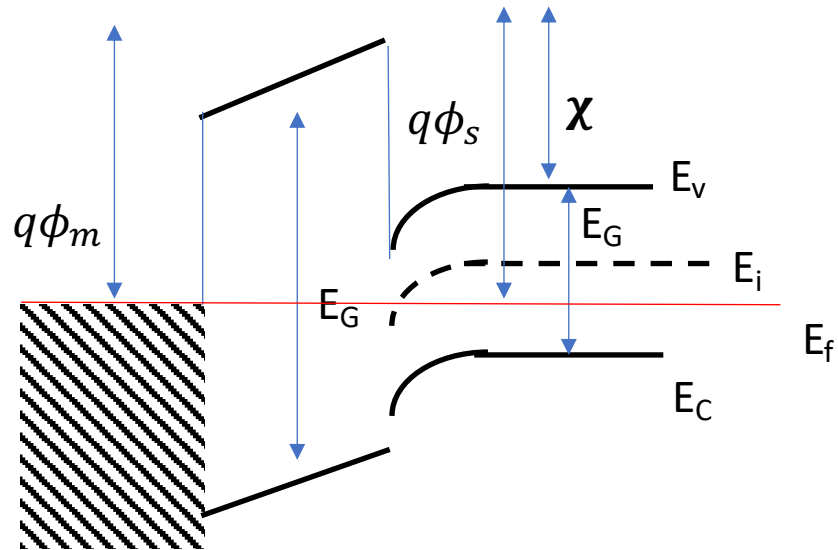
Thus, even at frequencies like 1kHz, the mos-CV does not follow the ideal curve.

C – V measurements bottomline:

1. Frequency of measurement determines the ability to invert the channel
2. Presence of fixed oxide charges leads to shift in the spectra (Flat band potential)
3. Nonzero ϕ_{ms} leads to shift in flat band potential
4. Interface trap-charge density leads to lower minimum capacitance.



Can we keep inverting ?



Various tunneling across the interface:

1. Thermal emission
2. Fowler-Nordheim tunneling
3. Frenkel-Poole emission

Tunneling across the insulator is a major reliability concern in modern day devices with shrinking oxide thickness!

Need for a switch:

Diodes

- Devices which current blocking characteristics used in rectifiers
- Varactors used in microwave devices and filters

Switches

- Three terminal devices useful in logic calculations
- Derived from vacuum tube devices used in computation

