Noname manuscript No.
(will be inserted by the editor)

A DC Model for Partially Depleted SOI Laterally Diffused MOSFETs Utilizing the HiSIM-HV Compact Model

Tarun Kumar Agarwal · M. Jagadesh Kumar

the date of receipt and acceptance should be inserted later

Abstract This paper presents a subcircuit compact model to study the dc characteristics of a partially depleted (PD) SOI laterally diffused metal oxide semiconductor field effect transistor (LDMOSFET) utilizing the HiSIM-HV compact model. Our model accounts both for the high-voltage and the floating-body effects such as the quasi saturation effect, the impact ionization in the drift region and the famous kink effect. The high-voltage effects, due to the surface MOS region of PD SOI LDMOSFET, are modeled using the HiSIM-HV model. The HiSIM-HV model, a surface-pote-ntial-based compact model, is used as a baseline model as it determines the potential consistently in the complete PD SOI LDMOSFET. And, to incorporate the floating-body effects into the HiSIM-HV model, we have used the same approach as used in developing BSIMSOI model. It is shown that to model the floating-body effects, mainly the kink in the output characteristics, the current due to the impact ionization in the drift region (I_{KIRK}) needs to be accurately modeled. An external current controlled current source (CCCS) is included in the proposed subcircuit model to model I_{KIRK} accurately. The model is validated for a set of channel and drift lengths to demonstrate the scalability of the model. The accuracy of the proposed subcircuit model is verified using 2-D numerical simulations.

Keywords SOI based high-voltage devices · floating-body effects · subcircuit approach

Tarun Kumar Agarwal
E-mail: tarun.agrawal90@gmail.com

M. Jagadesh Kumar
Department of Electrical Engineering
Indian Institute of Technology, Delhi
New Delhi - 110016
E-mail: mamidala@ieee.org

1 Introduction

Recently, for radio-frequency-integrated-applications (RFIC), LDMOSFETs on silicon-on-insulator (SOI) substrate have become the devices of choice due to enhanced power added efficiency (PAE) and reduced crosstalk [1, 2]. The LDMOSFET on SOI substrate can be designed for a wide range of applications ranging from a power amplifier (PA) in mobile handsets and base stations to automotive systems [3, 4]. To optimally design the power circuits, an accurate model for PD SOI LDMOSFET is required including the high-voltage (HV) and the floating-body effects.

To model the HV effects observed in bulk LDMOSFET and SOI LDMOSFET with body contact, various modeling approaches are reported in literature such HV-EKV, MOS Model 20 (MM20), and HiSIM-HV [5–9]. These models incorporate the HV effects with in the framework of the bulk MOSFET compact models such as EKV, MM11, and HiSIM. Similarly, to model the floating-body effects observed in the partially depleted SOI devices, various modeling approaches such as BSIMSOI, PSP-SOI, and HiSIM-SOI [10–12] are reported which are also developed within the framework of the bulk MOSFET compact models such as BSIM3, PSP and HiSIM.

To account for both the HV and floating-body effects observed in PD SOI LDMOSFETs, we therefore introduce two modeling approaches. One modeling approach uses the BSIMSOI compact model as a baseline model and incorporates the HV effects in the model using a subcircuit [13]. Another modeling approach uses the HiSIM-HV compact model as a baseline model and incorporates the floating-body effects in the model using a subcircuit. The HiSIM-HV model, a surface-potential-based compact model, is used as a baseline model

as it determines the potential consistently in the complete PD SOI LDMOSFET. To the best of our knowledge, there is no surface-potential-based compact model in literature for the partially depleted SOI LDMOSFETs taking into account the floating-body and the HV effects simultaneously.

The aim of this paper is therefore to develop a subcircuit model based on a surface-potential-based compact model for PD SOI LDMOSFETs simultaneously considering all the above special dc effects. To model these effects accurately, a subcircuit consisting of a pair of diodes, a parasitic BJT and an external current controlled current source are used along with HiSIM-HV compact model [14]. HiSIM-HV compact model can accurately predict the quasi saturation effect. But, the impact ionization in the drift region is not accurately captured in the model. Therefore, to accurately model the impact ionization in the drift region, an external current controlled current source is included in the subcircuit. And, to capture the floating-body effect such as the kink in the output characteristics of the floating-body PD SOI LDMOSFETs, a subcircuit, consisting of a pair of diodes and a parasitic BJT, is added to the HiSIM-HV compact model. The accuracy of the proposed subcircuit model is verified by 2-D device simulations [15].

2 Device structure and simulation results

Fig. 1 shows the cross-sectional schematic of a conventional bulk transistor and a floating-body PD SOI LDMOSFET respectively. Due to the presence of the body contact in Fig. 1(a), the floating-body effects are absent in bulk LDMOS devices. Therefore, a body-contacted PD SOI LDMOS device shows the same dc behavior as a bulk high-voltage MOSFET shown in Fig. 1(a) except the self-heating. On the other hand, due to the absence of the body contact, the dc behavior of a floating-body PD SOI LDMOSFET can be categorized into the HV and the floating-body effects. To analyze the special dc behavior of a floating-body PD SOI LDMOSFET, the transistor can be divided into the surface MOS and the parasitic BJT region as shown in Fig. 1(b). The device parameters for simulation are given in Table. 1 based on a fabricated PD SOI LDMOSFET in [16]. The device simulations are done using a 2-D numerical simulator, ATLAS [15]. To maintain sanity in the simulated data, calibration of the impact ionization model in ATLAS is performed with the measured data of PD SOI LDMOSFET fabricated with SOI CMOS process [16]. Impact ionization coefficients are optimized to best fit the experimental results (AN1 = 2x10^6 cm^{-1}, AN2 = 2x10^6 cm^{-1}, BN1 = 1.7x10^6 V/cm and BN2 = 1.7x10^6 V/cm). The drift region doping for the reference device is chosen to have a breakdown voltage higher than 15 V for the floating-body device and 20 V for the body contacted device. Some aspects such as graded channel doping density and gate overlap are not considered in the design of PD SOI LDMOSFET shown in Fig. 1(b). This is due to the availability of sub micrometer photolithography to define the channel length in the same way as CMOS devices and a self aligned drift-region implantation to the gate, rather than relying on the double-diffusion process [17].

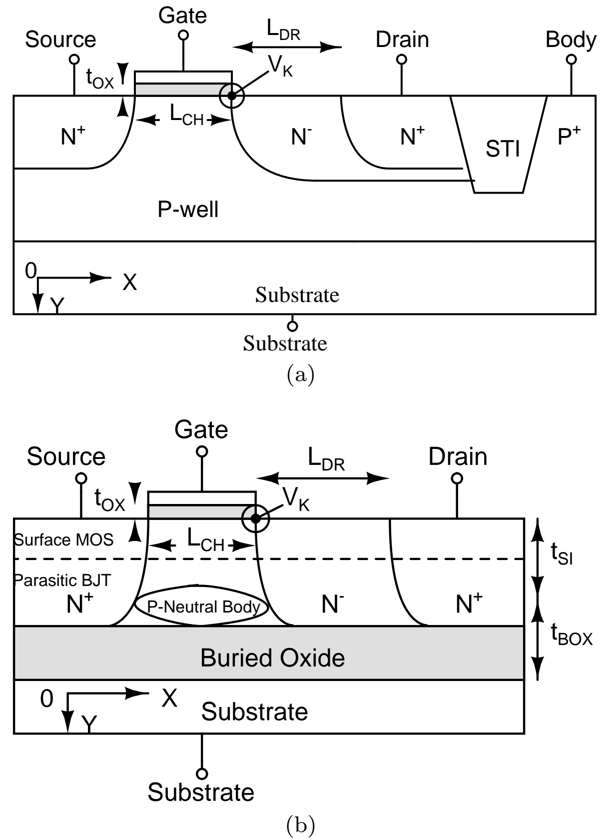


Fig. 1: Cross sectional schematics of the n-channel devices. (a) A bulk LDMOSFET. (b) A floating-body PD SOI LDMOSFET.

Table 1: Device parameters used in the simulation, derived from a reference device in [16].

Symbol	Description	Value
t_{OX}	Gate oxide thickness	30 nm
t_{SI}	Silicon film thickness	180 nm
t_{BOX}	Buried oxide thickness	1 μm
N_{ch}	Channel doping concentration	1.5x10^{17} cm^{-3}
N_{dr}	Drift region doping concentration	4x10^{16} cm^{-3}
L_{CH}	Channel length	0.64 μm
L_{DR}	Drift region length	1 μm

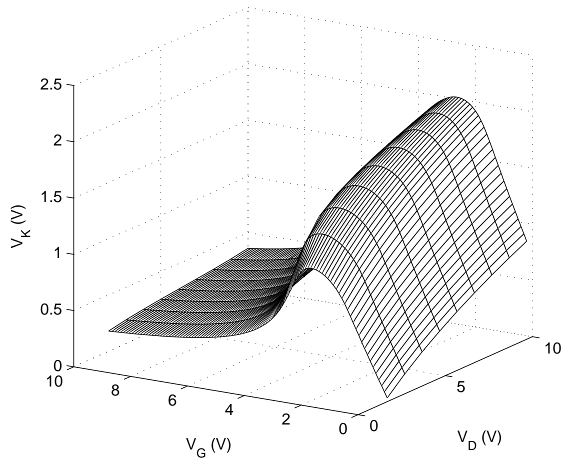
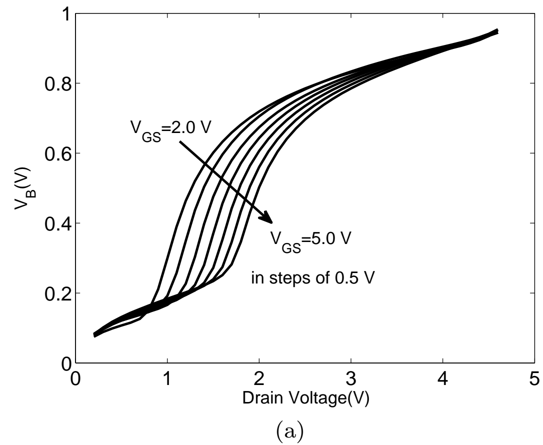


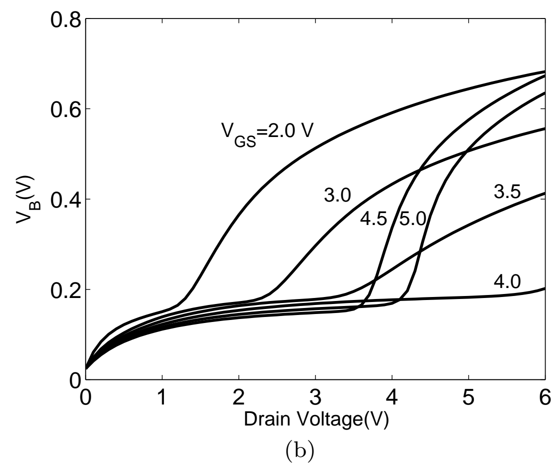
Fig. 2: Variation of V_K with gate bias the gate and drain biases obtained from ATLAS.

The surface MOS region of a PD SOI LDMOSFET can be further divided into the channel and the drift region. This classification and the concept of the intrinsic drain potential (V_K) have been a powerful tool to understand the HV effects such as the quasi saturation effect and the impact ionization in the drift region [18]. As Fig. 1(b) shows, V_K denotes the surface potential at the junction of the channel region and the drift region and Fig. 2 shows the variation of V_K with the gate and the drain voltage. Based on the variation of V_K with the gate voltage, the two modes of operation for HV MOSFET are defined. First being, a low voltage FET (the channel region) dominant mode of operation in which V_K increases with the gate voltage and reaches to a maximum value (V_{KMAX}). The second mode of operation is when the drift region starts dominating and V_K starts decreasing from V_{KMAX} with an increase in the gate voltage. Based on the variation of V_K, the quasi saturation and the impact ionization in the drift region are physically explained using Kirk effect i.e. when the injected electron density from the channel to the drift region exceeds the doping concentration of the drift region (N_{dr}), the transistor enters the triode mode of operation and the peak electric field shifts to the n^{-}– n^{+} junction.

To understand the floating-body effects in the PD SOI LDMOSFET, a conventional PD SOI MOSFET is chosen as a starting point. And it is observed that in a conventional floating-body PD SOI MOSFET, with an increase in the drain voltage, the electron-hole pair generation increases at the body-drain junction due to the increased impact ionization. The holes generated in this process are collected by the floating-body, which



(a)



(b)

Fig. 3: Body potential variation with drain bias obtained from ATLAS. (a) A conventional floating-body PD SOI MOSFET. (b) A floating-body PD SOI LDMOSFET.

in effect, raises the potential of the body, as shown in Fig. 3(a).

This increase in the body potential causes the forward-biasing of the source-body junction and lowers the threshold voltage (V_T) of the device, resulting in a kink in the output characteristics of a floating-body PD SOI MOSFET. This kink or the sudden increase in the drain current is shown in Fig. 4(a). On the other hand, a floating-body PD SOI LDMOSFET behaves as a conventional floating-body PD SOI MOSFET in the first mode of operation. And, in the drift dominant second mode of operation, due to the impact ionization in the drift region or the electron-hole pair generation at n^{-}–n^{+} junction, the floating-body potential show a different behavior than a conventional floating-body PD SOI MOSFET as shown in Fig. 3. At higher gate biases, as the floating-body potential rises at lower drain voltages

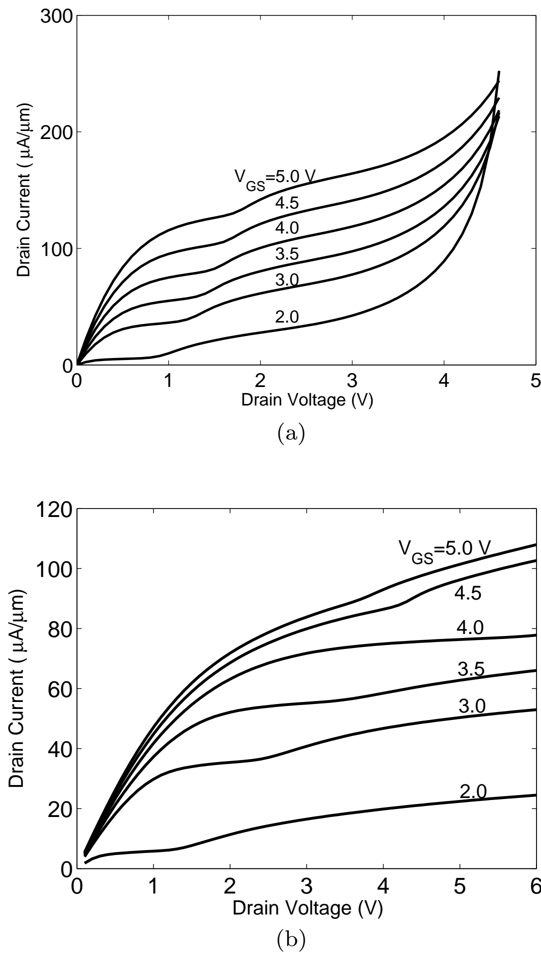


Fig. 4: Output characteristics of the n-channel devices obtained from ATLAS. (a) A conventional floating-body PD SOI MOSFET. (b) A floating-body PD SOI LDMOSFET.

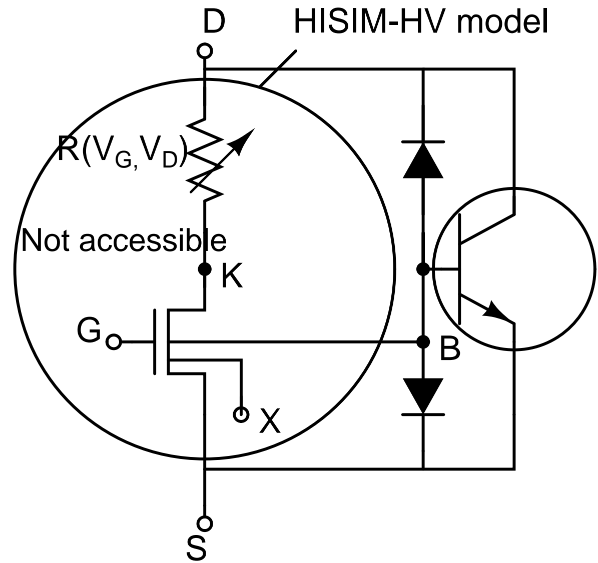


Fig. 5: SPICE subcircuit implementation with HiSIM-HV compact model.

due to the impact ionization in the drift region, the kink in the output characteristics occurs at lower drain voltages as shown in Fig. 4(b). In conclusion, to accurately model the kink behavior in the output characteristics, all the body current components, mainly the impact ionization current, are to be accurately modeled.

3 Modeling strategy

Based on the physical insights gained from the simulations, a model for PD SOI LDMOSFET can be derived from the HiSIM-HV compact model and a subcircuit. Here, HiSIM-HV compact model is used to model the surface MOS region and the subcircuit, consisting of a pair of diodes and a parasitic BJT, is used to model the parasitic BJT region of the transistor. Quasi saturation and impact ionization in the drift region are taken into account in HiSIM-HV model by using a bias dependent resistance and a current source for the impact ionization in the drift region. Fig. 5 shows the SPICE subcircuit implementation, containing a bulk HV MOSFET (accounting for the surface MOS region), a pair of diodes and a parasitic BJT. The parasitic BJT's collector terminal is the drain node (D) in this approach rather than the "K" node which is not accessible in HiSIM-HV compact model.

Therefore, to calculate the accurate potential at the base-collector junction of the parasitic BJT, a lateral npn BJT model with quasi saturation should be used in SPICE implementation of the subcircuit. But, in this paper, modeling of the breakdown phenomenon is not taken into consideration. Therefore, the accurate modeling of the parasitic BJT is not addressed here. In this way, the drain to source current (I_{DS}) and the body current (I_B) are expressed explicitly in terms of the external node voltages at the nodes D, G, S, B and X.

3.1 Bulk high-voltage MOSFET or surface MOS region modeling

A body-contacted PD SOI LDMOS device shows the same dc behavior as a bulk high-voltage MOSFET shown in Fig. 1(a) except the self-heating. The surface MOS region (the channel and the drift region), which results in HV effects, is modeled using the HiSIM-HV compact model. The HiSIM-HV model shows good capability in modeling HV effects such as the quasi saturation and the impact ionization in the drift region with chan-

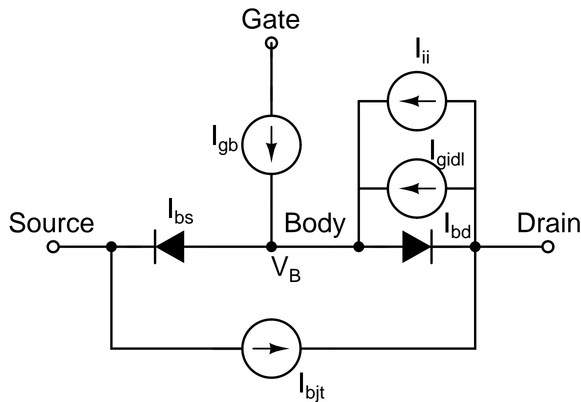


Fig. 6: Circuit representation of the floating-body potential calculation under the influence of various dc currents for a conventional PD SOI MOSFET [19].

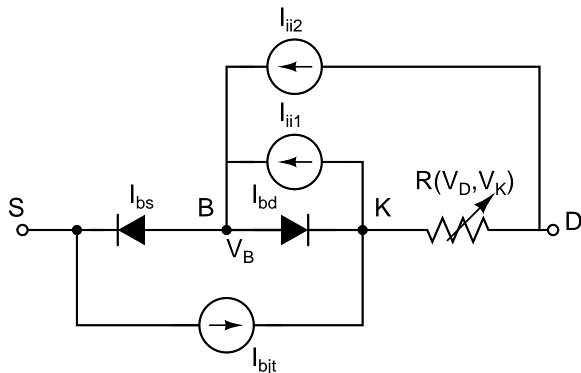


Fig. 7: Circuit representation of the floating-body potential calculation for a PD SOI LDMOSFET.

nel and the drift length scaling. In HiSIM-HV model, the channel region is modeled using a surface potential based model, HiSIM2, and the drift region is modeled using a bias dependent resistance. HiSIM-HV model also accounts for the impact ionization in the drift region by adding an extra current which is a function of the drain to source current (I_{DS}) and the surface potentials at the nodes D, K and S.

3.2 floating-body effect and parasitic BJT modeling

To model the floating-body effects observed in a conventional PD SOI MOSFET, BSIMSOI model uses an equivalent circuit as shown in Fig. 6.

This is to calculate the floating-body voltage under the influence of various body currents. In BSIMSOI model, the kink in the output characteristics of a PD SOI MOSFET is effectively modeled by monitoring the degree of forward bias of the body-to-source junction as a function of the impact ionization current (I_{ii}), which is a strong function of V_D [19]. It is due to the fact that the hole current due to the impact ionization (I_{ii}) at the body-drain junction flows into the body and forward biases the source-to-body diode so that the diode current is equal to I_{ii}. Thus, the voltage across the diode or the floating-body voltage (V_{BS}) is indicated by the IV characteristics of the source to body diode. An increase in V_B causes lowering of the threshold voltage (V_T) due to the body effect. The change in V_T causes a sudden increase in the drain current when the impact ionization becomes significant which results in the famous kink effect in the output characteristics as shown in Fig. 4(a).

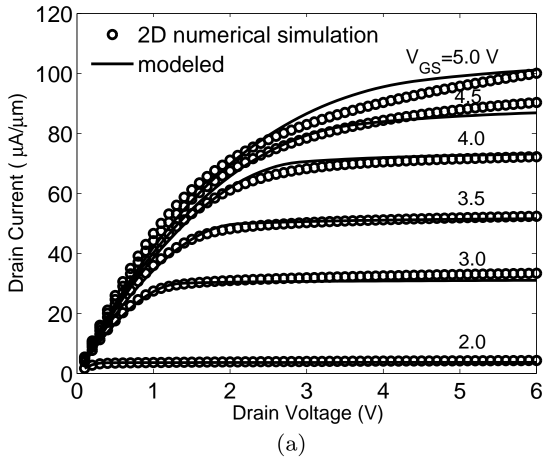
The circuit shown in Fig. 7 is derived from the circuit shown in Fig. 6 to calculate the floating-body potential in the PD SOI LDMOSFET. Considering the device parameters used in our simulations, I_{gb} and I_{gidl} can be neglected. Moreover, $R(V_D, V_K)$ is also neglected since the accurate modeling of parasitic BJT is not addressed in this paper.

4 Results and discussion

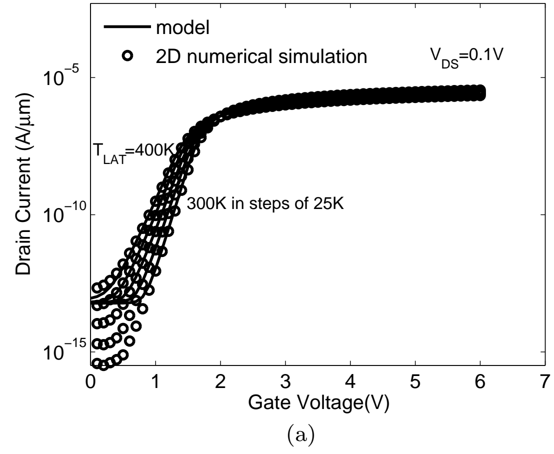
The parameters of the developed model are extracted using a commercial extraction software package, IC-CAP, after implementing the SPICE subcircuit shown in Fig. 5 in Spectre. The potential of the floating node "B" is calculated within the simulator using the HiSIM-HV in-built compact model and the proposed subcircuit. The surface MOS region is modeled using a surface potential based model, HiSIM-HV which is an industry standard model for high-voltage bulk MOSFETs.

A body-contacted PD SOI LDMOS device minimizes the floating-body and the parasitic BJT effects. Therefore, the model parameters of HiSIM HV compact model are extracted using the scalable data for the body-contacted PD SOI LDMOSFET. HiSIM HV is capable of modeling the quasi saturation and the impact ionization in the drift region. And, to model the floating-body effects, a subcircuit consisting of a pair of diodes and a parasitic BJT is added to HiSIM HV compact model, as shown in Fig. 5. The calculated results from the proposed model are calibrated with the 2-D numerically simulated characteristics of both the body contacted and the floating-body PD SOI LDMOSFETs for different dimensions.

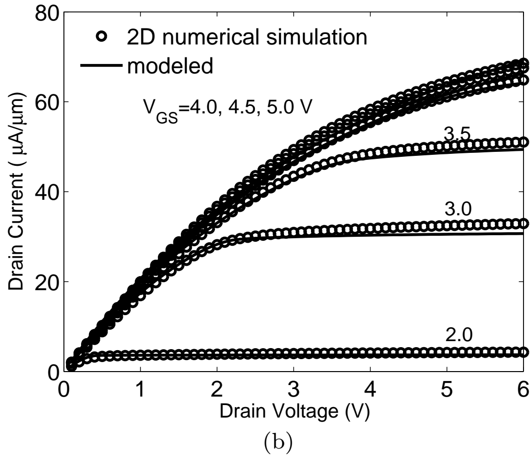
Fig. 8 shows that the calculated output characteristics of the body contacted transistor have a good consistency with the 2-D numerically simulated data for different channel and drift lengths. Additionally, Fig. 9 shows that the self-heating effect is included in the developed model by accurately calculating the transfer



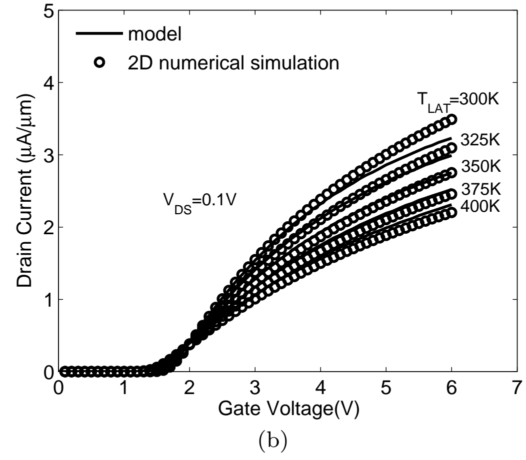
(a)



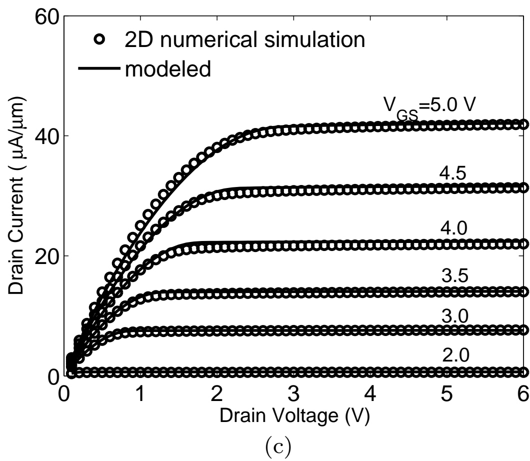
(a)



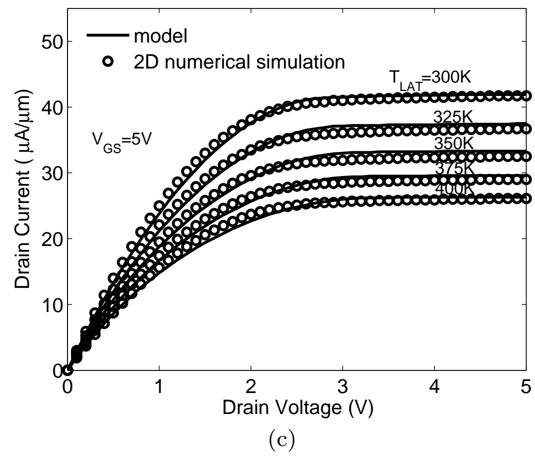
(b)



(b)



(c)



(c)

Fig. 8: (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a body contacted PD SOI LDMOSFET using HiSIM-HV approach for (a) L_{CH}=0.64 μm and L_{DR}=1 μm. (b) L_{CH}=0.64 μm and L_{DR}=3 μm. (c) L_{CH}=3 μm and L_{DR}=1 μm.

Fig. 9: (symbols) 2-D numerically simulated and (solid lines) calculated transfer and output characteristics of a body contacted PD SOI LDMOSFET (L_{CH}=3 μm and L_{DR}=1 μm) for different lattice temperatures (a) transfer characteristics in logscale for drain voltage=0.1 V. (b) transfer characteristics for drain voltage=0.1 V. (c) output characteristics for gate voltage=5 V.

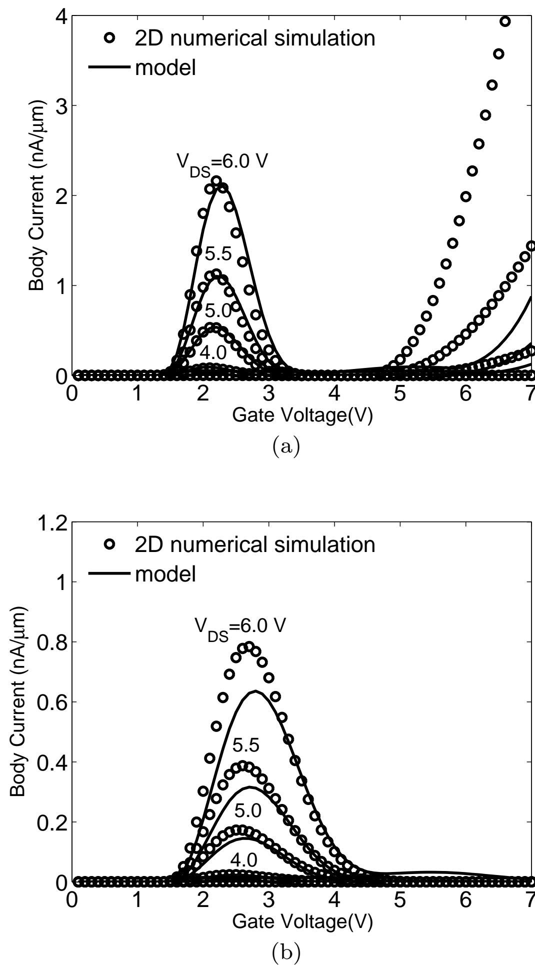


Fig. 10: (symbols) 2-D numerically simulated and (solid lines) calculated body current characteristics of PD SOI LDMOSFET using HiSIM-HV approach for (a) L_{CH}=0.64 μm and L_{DR}=1 μm. (b) L_{CH}=3 μm and L_{DR}=1 μm.

and output characteristics of the body contacted transistor with the temperature-dependent 2-D numerically simulated data.

HiSIM-HV captures the quasi saturation effect and the impact ionization in the drift region with the internal drift resistance model and an extra impact ionization current, respectively. To accurately calculate the inferred body potential in the floating-body PD SOI LDMOS, all the body current components such as impact ionization current, diode current and the parasitic BJT currents need to be accurately modeled. Fig. 10 shows that the impact ionization current in the first mode of operation is well modeled for different channel lengths, but the impact ionization current due to the drift region is not modeled accurately. The accuracy of the impact ionization current due to the drift region is limited in the HiSIM-HV compact model. It may be because of the fact that the substrate current modeling in the bulk devices is only to predict the device reliability [20].

The output characteristics of the floating-body PD SOI LDMOSFET shows the kink behavior which is modeled by calculating the inferred body potential using a subcircuit connected to the body node. Fig. 11(a) shows that the kink behavior in the drift dominant mode of operation is not accurately captured due to the less number of fitting parameters in HiSIM-HV model for modeling the impact ionization in the drift region. But, Fig. 11(b) and Fig. 11(c) show that the kink behavior in the output characteristics is accurately modeled for large channel and drift region lengths. In conclusion, to accurately model the floating-body effects of PD SOI LDMOSFET using HiSIM-HV based approach, a more accurate model of the impact ionization current in the drift region is required. Therefore, we propose a subcircuit which accurately models the current due to the impact ionization in the drift region (I_{KIRK}) and thus, the kink effect.

4.1 Accurate modeling of the impact ionization in the drift region

To accurately model the impact ionization in the drift region, an external current controlled current source is added in the subcircuit as shown in Fig. 12.

The equation of the external current controlled current source used in this subcircuit is developed as follows: A general body current equation due to impact ionization in the drift region can be written as:

$$I_{ii2} = \int_0^{L_{DR}} alpha \cdot I_{DS} \cdot exp(-\frac{B}{E_y})dy \quad (1)$$

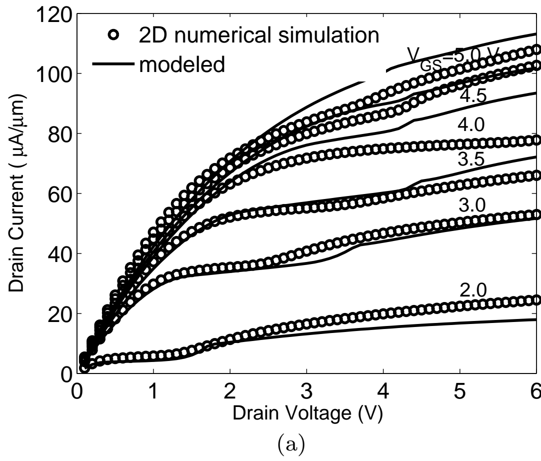
Eq. 1 can be approximated into a well known equation as given below [21]:

$$I_{ii2} = alpha \cdot (V_D - (EC*l)) \cdot I_{DS} \cdot exp\left(-\frac{B \cdot L_{DR}}{(V_D - (EC*l))}\right) \quad (2)$$

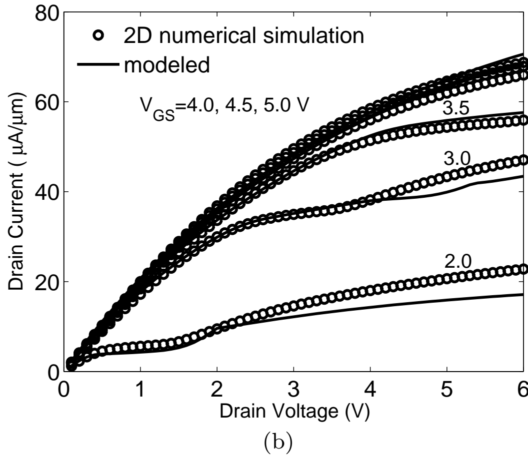
Here, $EC * l$ is the potential at y=0 (at body-drift region junction) as the node "K" is unavailable in the HiSIM-HV model and V_D is the potential at y=L_{DR} where, l is the channel length of the device.

Since I_B increases with gate voltage continuously until the device breaks down after the transistor enters the triode region. To model this behavior, eq. 2 is modified as:

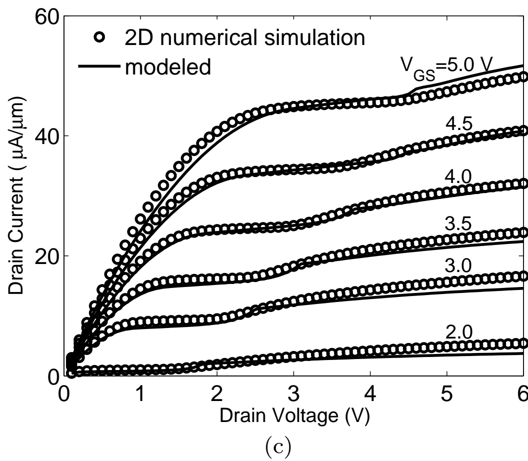
$$I_{ii2} = alpha \cdot (V_D - (EC * l)) \cdot I_{DS} \cdot exp\left(-\frac{B}{E_{eff}}\right) \quad (3)$$



(a)



(b)



(c)

Fig. 11: (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a floating-body PD SOI LDMOSFET using HiSIM-HV approach for (a) L_{CH}=0.64 μm and L_{DR}=1 μm. (b) L_{CH}=0.64 μm and L_{DR}=3 μm. (c) L_{CH}=3 μm and L_{DR}=1 μm.

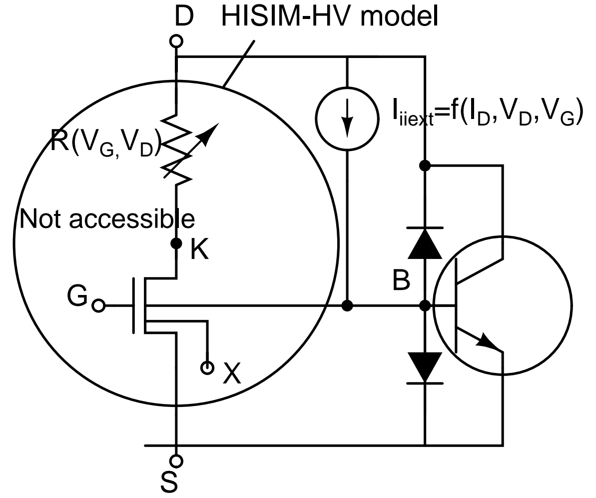


Fig. 12: Improved subcircuit implementation in SPICE with HiSIM-HV compact model.

where,

$$E_{eff} = \left(\frac{(V_D - (EC * l))^{coeff2} \cdot (V_{GS} - V_{OFF})^{coeff1}}{L_{DR}} \right) \quad (4)$$

The model parameters in the current controlled current source model (eq. 3) are *alpha, B,* V_{OFF}*, EC, coeff1* and *coeff2*.

After implementing the SPICE subcircuit shown in Fig. 12 in Spectre, model parameters of the external current controlled current source are extracted. Fig. 13 and Fig. 14 show the comparison of the characteristics of the subcircuit models with and without the external current controlled current source. Fig. 13 shows the accurate modeling of the impact ionization in the drift region with the subcircuit including the external current controlled current source. It is clear from Fig. 14 that accurate modeling of the impact ionization in the drift region gives a better fitting of the kink behavior in the output characteristics of the floating-body device.

5 Conclusion

A scalable model for HV PD SOI devices is developed using a proposed subcircuit approach by utilizing the HiSIM-HV compact model. The developed model includes HV and the floating-body effects observed in PD SOI LDMOS devices. The current due to the impact ionization in the drift region is modeled accurately by including a current controlled current source in the proposed subcircuit. To study and model the floating-body and HV effects, the device is divided into the surface MOS and the parasitic BJT region. Using the 2-D numerical simulator, ATLAS, a physical description of the specific dc behavior of partially depleted

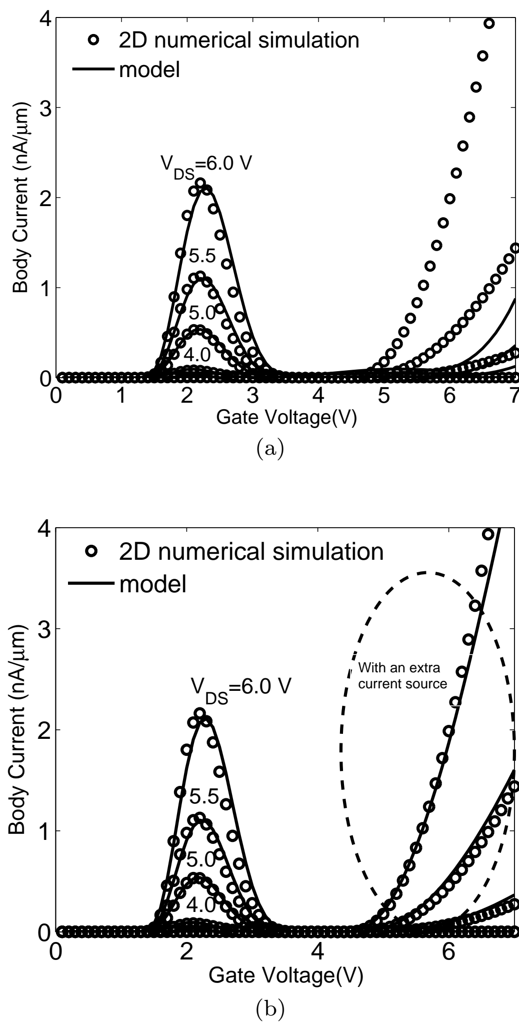


Fig. 13: (symbols) 2-D numerically simulated and (solid lines) calculated body current characteristics of PD SOI LDMOSFET using HiSIM-HV approach for L_{CH}=0.64 μm and L_{DR}=1 μm with (a) the subcircuit without external CCCS. (b) Improved subcircuit with external CCCS.

SOI LDMOSFET is presented. In the proposed modeling approach, the surface MOS region is modeled using the HiSIM-HV compact model while to capture the floating-body effects, BSIMSOI model approach is used. The model performance is demonstrated for the 20-V LDMOS device by implementing the SPICE subcircuit in Spectre (Cadence). Generally, the proposed compact models can be run on any SPICE simulator, since the model equations of the standard HiSIM-HV and BJT (Level=1) compact models are not changed. Therefore, the developed compact models here will enable the accurate design of complex circuits, using PD SOI LDMOS devices based on SPICE simulation.

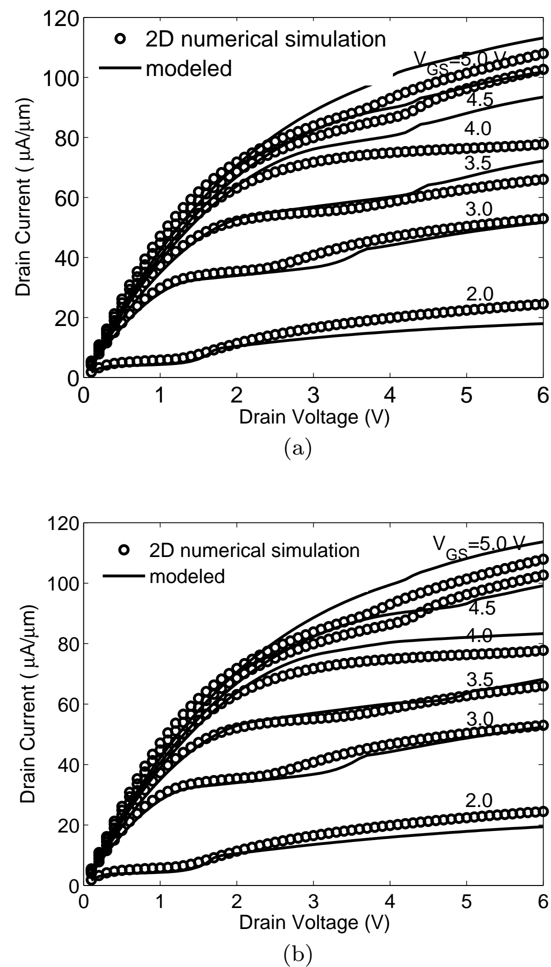


Fig. 14: (symbols) 2-D numerically simulated and (solid lines) calculated output characteristics of a floating-body PD SOI LDMOSFET using HiSIM-HV approach for L_{CH}=0.64 μm and L_{DR}=1 μm with (a) the subcircuit without external CCCS. (b) Improved subcircuit with external CCCS.

Acknowledgment

The authors would like to thank V. Subramanian, A. R. Trivedi, Y. S. Chauhan and A. Bandyopadhyay for their interesting comments.

References

1. J. G. Fiorenza and J. A. del Alamo, "Experimental comparison of RF power LDMOSFETs on thin-film SOI and bulk silicon," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 687-692, Apr. 2002.
2. R. Yang, H. Qian, J. Li, Q. Xu, C. Hai and Z. Han, SOI technology for radio-frequency integrated-circuit applications, *IEEE Transactions on Electron Devices*, vol.53, no.6, pp. 1310-1316, June 2006.

3. R. Sithanandam and M. J. Kumar, Linearity and speed optimization in SOI LDMOS using gate engineering, *Semiconductor Science and Technology*, Vol.25, no. 015006, pp. 1-6, Jan 2010.
4. M. J. Kumar and R. Sithanandam, Extended-p+ Stepped Gate (ESG) LDMOS for Improved Performance, *IEEE Transactions on Electron Devices*, Vol.57, July 2010.
5. Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. B. Desormeaux, A. Sharma, M. Declercq and A. M. Ionescu, "Scalable general high voltage MOSFET model including quasi-saturation and self-heating effects," *Solid State Electron.*, vol. 50, no. 11/12, pp. 1801-1813, Nov./Dec. 2006.
6. Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. Declercq, and A. M. Ionescu, "An EKV-based high voltage MOSFET model with improved mobility and drift model," *Solid State Electron.*, vol. 51, no. 11/12, pp. 1581-1588, Nov./Dec. 2007.
7. A. C. T. Aarts, N. DHalleweyn, and R. van Langevelde, "A surface potential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 999-1007, May 2005.
8. A. C. T. Aarts and W. J. Kloosterman, "Compact modeling of high-voltage LDMOS devices including quasi-saturation," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 897-902, Apr. 2006.
9. H.J. Mattausch, T. Kajiwara, M. Yokomichi, T. Sakuda, Y. Oritsuki, M. Miyake, N. Sadachika, H. Kikuchihara, U. Feldmann, M. Miura-Mattausch, "HiSIM-HV: A compact model for simulation of high-voltage-MOSFET circuits," in *International Conference on Solid-State and Integrated-Circuit Technology*, Oct. 2008, pp.276-279.
10. D. Sinitsky, S. Tang, A. Jangity, F. Assaderaghi, G. Shahidi and C. Hu, "Simulation of SOI devices and circuits using BSIM3SOI," *IEEE Transactions on Electron Devices*, vol. 19, no. 9, pp. 323-325, Sep 1998.
11. W.Wu, X. Li, G. Gildenblat, G.Workman, S. Veeraraghavan, C. McAndrew, R. van Langevelde, G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen and J. Watts, PSP-SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs, in *IEEE Custom Integrated Circuits Conference*, pp.41-48, Sept. 2007.
12. H.J. Mattausch, N. Sadachika, S. Kusu, K. Ishimura, T. Murakami, M. Ando and M. Miura-Mattausch, The surface-potential-based compact model HiSIM-SOI for Silicon-On-Insulator MOSFETs, in *MIXDES* 09, pp.77-81, June 2009.
13. T. K. Agarwal, A. R. Trivedi, V. Subramanian and M. J. Kumar, Compact Modeling of Partially Depleted Silicon-on-Insulator Drain- Extended MOSFET (DEMOSFET) including High-voltage and Floating Body Effects, *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3485-3493, Oct 2011.
14. HiSIM HV 1.0.1 Users Manual, Copyright 2008, Hiroshima University and STARC, http://home.hiroshima-u.ac.jp/usdl/HiSIM HV/CCode/ HiSIM HV 1.0.2 Users-Manual.pdf.
15. Atlas Users Manual: Device Simulation Software. Santa Clara, CA: Silvaco Int., 2008.
16. J.G. Fiorenza, D.A. Antoniadis, J.A. del Alamo, RF power LDMOSFET on SOI, *IEEE Electron Device Letters*, vol.22, no.3, pp.139-141, Mar 2001.
17. L. Wang, J. Wang, C. Gao, J. Hu, P. Li, W. Li and S.H.Y.Yang, Physical Description of Quasi-Saturation and Impact-Ionization Effects in High-Voltage Drain-Extended MOSFETs, *IEEE Transactions on Electron Devices*, vol.56, no.3, pp.492-498, Mar. 2009.
18. C. Anghel, N. Hefyene, A. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier, and Y. Mourier, Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage, in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 399-402.
19. M. Chan, P. Su, H. Wan, C.-H. Lin, S. K. H. Fung, A. M. Niknejad, C. Hu, and P. K. Ko, Modeling the floating-body effects of fully depleted, partially depleted, and body-grounded SOI MOSFETs, *Solid State Electron.*, vol. 48, no. 6, pp. 969-978, Jun. 2004.
20. E. Vandenbossche, C. De Keukeleire, M. de Wolf, H. V. Hove and J. Witters, Modelling and simulation of hot-carriers degradation of high voltage floating lateral NDMOS transistors, *Microelectronics Reliability*, Vol.38, no.6-8, pp.1097-1101, Jun 1998.
21. N. Arora, MOSFET Models for VLSI Circuit Simulation: Theory and Practice, Springer-Verlag New York, Inc., Secaucus, NJ, USA, 1993.