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2D-simulation and analysis of lateral SiC N-emitter SiGe P-base Schottky metal-collector (NPM) HBT on SOI

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Abstract

We report a novel BiCMOS compatible lateral SiC N-emitter, SiGe P-base Schottky metal-collector NPM HBT on SOI. The proposed lateral NPM HBT performance has been evaluated in detail using 2-dimensional device simulation by comparing it with the equivalent NPN HBT and homojunction silicon NPM BJT structures. Based on our simulation results, it is observed that while both the lateral NPM and NPN HBTs exhibit high current gain, high cut-off frequency compared to the homojunction NPN BJT, the lateral NPM HBT has the additional benefit of suppressed Kirk effect and excellent transient response over its counterpart lateral NPN HBT. The improved performance of the proposed NPM HBT is discussed in detail and a CMOS compatible process is suggested for its fabrication.

1. Introduction

Heterojunction bipolar transistors based on either SiC [1–3] wide-bandgap emitter on Si-base or Si emitter on narrow bandgap SiGe-base [4,5] have wide applications in high speed applications. Device designers have started recognizing the utility of SiC as an emitter in HBTs to take the full advantages of its excellent material properties together with its fabrication compatibility with silicon. In the past, several structures were reported in literature [6,7] with SiC as emitter in HBTs. Similarly, SiGe is a promising material in applications such as RF circuits, mixed signal circuits and precision analog circuits.

While the SiC/Si and SiGe/Si based HBTs have several advantages, they also suffer from many non-ideal effects such as base widening at high collector currents and excessive base storage time. To overcome this problem, one can use a Schottky collector either as a vertical structure [8] or as a lateral structure on SOI [9]. Although reproducible Schottky contacts are not easy to realize due to surface conditions, Schottky collector offers several advantages in terms of suppressing base-widening and preventing the transistor from entering hard saturation both of which are detrimental for high current and high speed applications. It is also worth mentioning that lateral bipolar transistors are best preferred over vertical structures in CMOS design because of their process simplicity. In the recent past, several lateral BJT structures on SOI have been reported.

However, to combine the advantages of SiC and SiGe with the combination of SOI technology and lateral Schottky collector, for the first time, we propose a novel SiC N-emitter, SiGe P-base lateral Schottky metal-collector NPM HBT. To the best of our knowledge this is the first work to suggest the integration of SiC emitter, SiGe base, lateral Schottky collector and SOI for BiCMOS applications providing an incentive for further experimental exploration.

We evaluated the performance of the proposed NPM HBT and its equivalent NPN HBT and NPM BJT structures using two-dimensional device simulator ATLAS [10] which is widely used in industry. Our simulation results show that while both the lateral NPM and NPN HBTs exhibit high current gain, high cut-off frequency compared to the homojunction NPN BJT, the lateral NPM HBT is demonstrated to have additional

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benefits of suppressed Kirk effect and excellent transient response over its counterpart lateral NPN HBT.

2. Device structure, simulation parameters and proposed fabrication steps

Top and cross-sectional view of the proposed NPM HBT (SiC N-emitter, SiGe P-base lateral Schottky metal-collector HBT), implemented in the two-dimensional device simulator ATLAS [10] is shown in Fig. 1. We start with an SOI wafer having a p-type epitaxial layer of 0.2 μm thickness doped at 5×10^{17} cm^{-3}. Deposit a thick CVD oxide and pattern as shown in Fig. 2(a). In the next step, epitaxially grow the n^+ SiC on the vertical edge (at point A in Fig. 2(b)) of the silicon surface which acts as a seed for the lateral growth of SiC [11–14] as shown in Fig. 2(b). It may be pointed out that due to the dangling bonds at the emitter–base heterojunction interface, recombination current may be large. However, it has been shown that the recombination current due to dangling bonds at the heterojunction and in SiC can be minimized by adding a terminator [15]. CMP process, a thick CVD oxide deposition and its patterning follow as shown in Fig. 2(c). Following this step, a nitride film is deposited as shown in Fig. 2(d) and is etched using an unmasked RIE etch to retain a nitride spacer at the vertical edge of thick CVD oxide as shown in Fig. 2(e). Next, a thick CVD oxide deposition and surface planarization using CMP follow as shown in Fig. 2(f). The nitride spacer is removed with selective etching to open a window in the oxide as shown in Fig. 2(g).

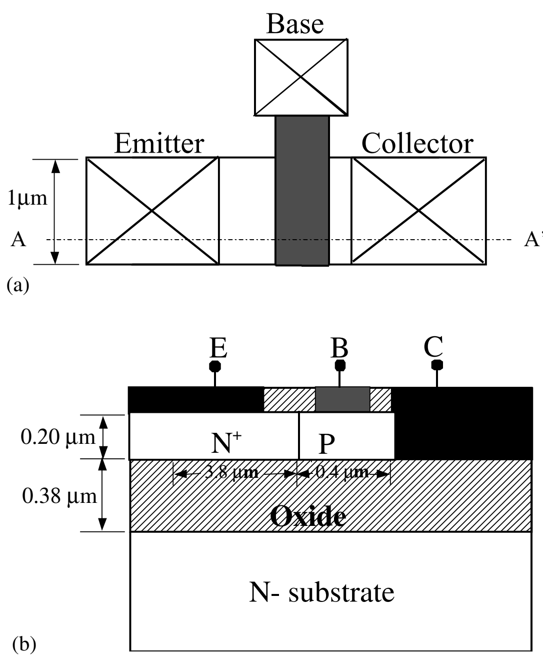

Fig. 1. (a) Top and (b) cross-sectional view of the proposed NPM HBT (SiC emitter, SiGe base lateral Schottky collector HBT on SOI).

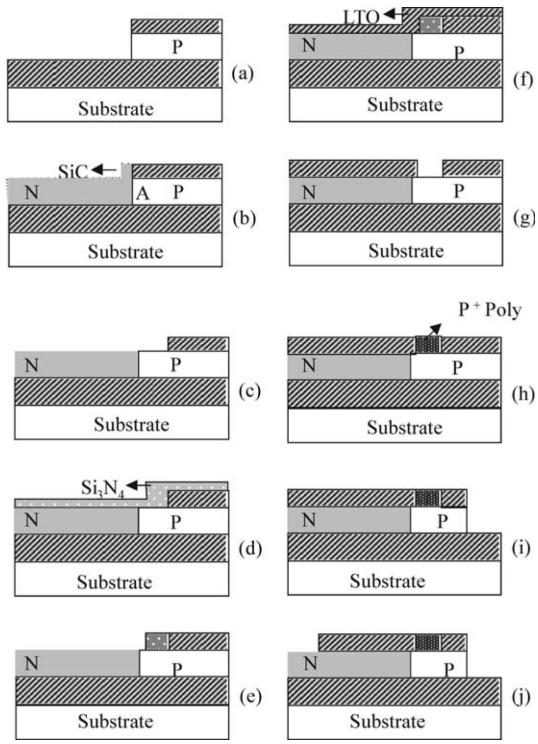

Fig. 2. Fabrication steps for the proposed NPM HBT.

To create the SiGe base region, we now need to implant Ge through this oxide window. It has been shown [16–19] that Ge implantation is a useful technique to create SiGe regions. Energies in the range of 130 keV and fluences of the order of 3×10^{16} cm^{-2} can be used for this purpose. This needs to be followed by a rapid thermal annealing for at least 10 s to recrystallize the amorphous SiGe region [4]. In our simulations we have assumed a maximum Ge concentration of 20% which is the maximum limit for most practical applications [4,5].

After converting silicon in the base region to SiGe, we deposit p^+-poly followed by CMP process and planarization leaving only p^+-poly in the window as shown in Fig. 2(h). Next, windows are opened for metal Schottky collector (Fig. 2(i)) and n^+ emitter contacts (Fig. 2(j)). Finally, palladium silicide is deposited to form the Schottky collector contact and ohmic contacts on the emitter and p^+-poly base region.

Palladium silicide is chosen for the Schottky collector as it gives the highest barrier height (0.7 eV) with p-type SiGe [20,21]. The final structure appears as shown in Fig. 1(b). The ATLAS [9] input parameters for the

Table 1
ATLAS input parameters for the proposed lateral NPM HBT, NPN HBT and homojunction silicon NPM BJT

Parameter	Value
SOI thickness t_{si} (initially)	0.20 μm
Buried oxide thickness t_{box}	0.38 μm
Field oxide thickness t_{ox}	0.18 μm
Emitter length	3.80 μm
Base length	0.40 μm
Emitter region doping concentration	5×10^{19} cm^{-3}
Base region doping concentration	5×10^{17} cm^{-3}
Collector region doping concentration (only for NPN HBT)	2×10^{17} cm^{-3}
Barrier height lowering coefficient	2.0×10^{-7} cm
SRH concentration parameter for electrons and holes NSRHN and NSRHP (both for Si and SiGe)	1×10^{22} cm^{-3}

proposed NPM HBT and those of the compatible NPN HBT and NPM BJT are listed in Table 1. These parameters are chosen based on reported experimental results for lateral bipolar transistors on SOI [22].

3. Performance evaluation and comparison

In the two-dimensional device simulation using ATLAS [10], we have used suitable physical models for mobility, bandgap narrowing, Shockley–Read–Hall and Auger recombination. For the carrier statistics purpose, we used the Fermi–Dirac distribution. The incomplete ionisation model is used to account for the deep donor (N_D) and deep acceptor (N_A) levels in SiC emitter. Standard thermionic emission model is incorporated including image force barrier lowering phenomenon for the Schottky collector junction. Electrical properties of SiC are taken from the literature [23].

3.1. DC Performance

Fig. 3 shows the simulated common-emitter output characteristics of the proposed lateral NPM HBT and its equivalent devices (lateral NPN HBT and NPM BJT). We observe that the proposed NPM HBT and NPN HBT show a large transconductance compared to the homojunction silicon NPM BJT. The proposed NPM HBT however shows a finite collector offset voltage [24,25]. Since the proposed structure includes both the heterojunction on the emitter side and the Schottky junction on the collector side, its collector offset voltage is expected to be larger than that of lateral NPN HBT and NPM BJT. This should be taken into account in the digital logic circuit design.

The Gummel plots are shown at $V_{CE} = 1$ V in Fig. 4. We note that the base current of the proposed NPM HBT is less than that of the NPN HBT even at high-level injection of carriers which clearly shows the suppression of the Kirk effect [26] in the proposed NPM HBT. Fig. 5 shows the gain versus collector current for all the three structures considered in our study. As it is clear from the figure, the gain of the proposed lateral NPM HBT and NPN HBT is very high compared to that of lateral homojunction NPM BJT due to the high emitter injection efficiency because of differing barrier heights for electrons and holes at the emitter junction. We also note that the lateral NPM HBT can also operate at higher collector currents than the NPN HBT because of the metal collector.

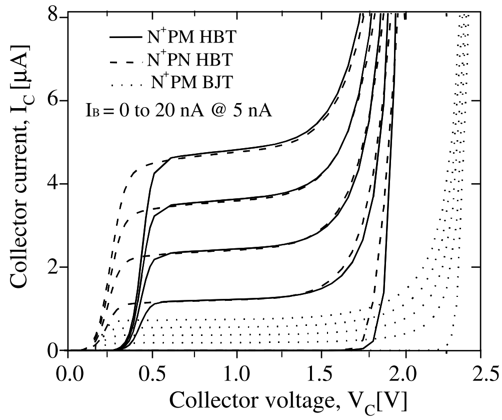

Fig. 3. Common-emitter IV characteristics of the proposed NPM HBT and compared with NPN HBT, NPM BJT.

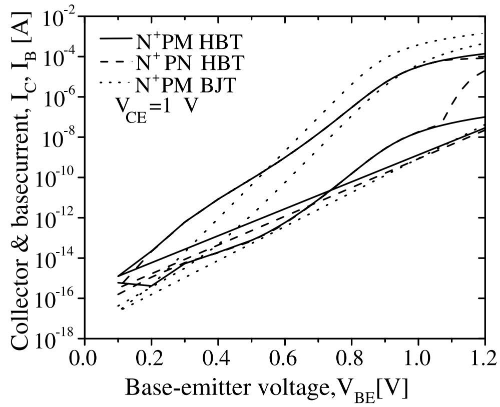

Fig. 4. Gummel plot of the proposed NPM HBT compared with NPN HBT, NPM BJT for a fixed collector emitter voltage ($V_{CE} = 1$ V).

3.2. Dynamic behaviour analysis

Fig. 6 shows the unity gain cut-off frequency versus collector current for all the three structures and we note

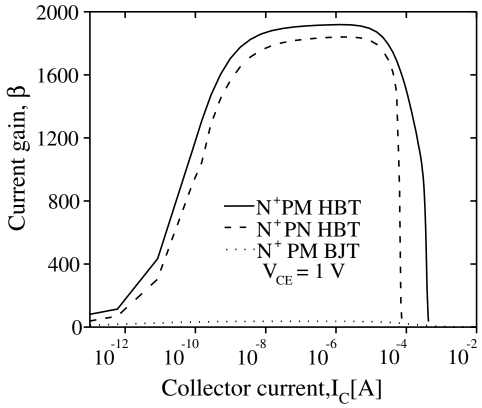

Fig. 5. Gain versus collector current characteristics of the proposed NPM HBT compared with those of NPN HBT, NPM BJT for a fixed collector emitter voltage ($V_{CE} = 1$ V).

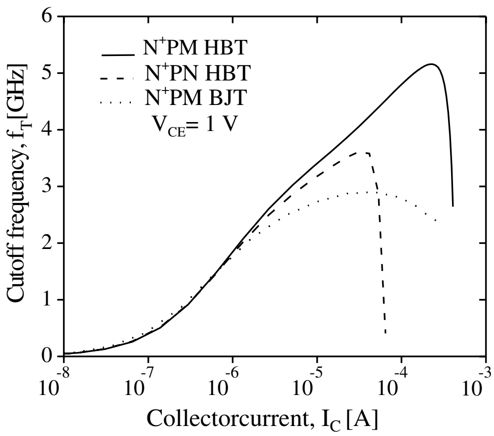

Fig. 6. Unity gain cut-off frequency versus collector current of the proposed NPM HBT and its counterparts (NPN HBT and NPM BJT).

that the cut-off frequency of the proposed lateral NPM HBT is higher than those of lateral NPN HBT and NPM BJT due to its metal collector and higher transconductance g_m. The proposed lateral NPM HBT exhibits an f_T of 5.2 GHz at a collector current of 0.2 mA, whereas for the comparable NPN HBT and NPM BJT, f_T falls to a negligible value at the above current due to Kirk effect and decrease in transconductance.

From the transient behaviour shown in Fig. 7, it is clear that the proposed lateral NPM HBT shows excellent transient response with nearly zero base charge storage time due to its metal collector and suppressed Kirk effect. The lateral NPN HBT shows a higher storage time due to the Kirk effect and also the electron pile-up at the collector–base heterojunction [7].

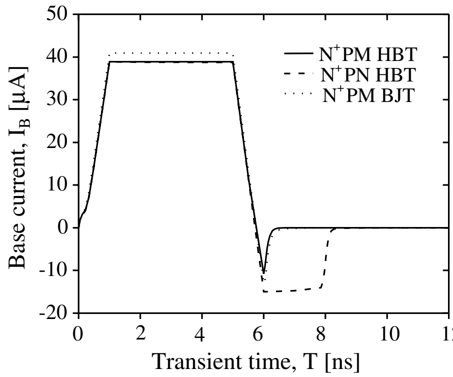

Fig. 7. Transient behaviour of the proposed NPM HBT which is compared with NPN HBT and NPM BJT.

4. Conclusion

A thorough investigation of the proposed lateral SiC N-emitter, SiGe P-base Schottky collector HBT has been presented. We conclude from our study that the proposed lateral NPM HBT exhibits superior performance in terms of high current gain, high cut-off frequency, suppressed Kirk effect and excellent transient response over its counterparts. Its excellent transient response is expected to result in a reduced power-delay product. The proposed NPM HBT finds applications in BiCMOS compatible high current-driving circuits and high speed circuits such as RF, mixed signal and in precision analog circuits.

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