The Simulation of a New Asymmetrical Double-Gate Poly-Si TFT With Modified Channel Conduction Mechanism for Highly Reduced OFF-State Leakage Current

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***Abstract*—Poly-Si thin film transistors (TFTs) exhibit large OFF-state reverse leakage currents since their channel conduction is controlled by the gate-induced grain barrier lowering (GIGBL). This also leads to the presence of the pseudosubthreshold region in the transfer characteristic. In this paper, we report a novel poly-Si multiple-gate TFT (MG-TFT), where the front gate consists of three sections with two different materials, in order to reduce the OFF-state leakage current with no significant change in the ON-state current. We demonstrate that the dominant conduction mechanism in the channel can be controlled entirely by the accumulation charge density modulation by the gate (ACMG) instead of the GIGBL, leading to a steep subthreshold slope without any pseudosubthreshold region when compared to an asymmetrical double-gate poly-Si TFT (DG-TFT), resulting in a significantly reduced OFF-state leakage current. Using two-dimensional (2-D) and two-carrier device simulation, we have analyzed the various performance and design considerations of the MG-TFT and explained the reasons for the improved performance of the MG-TFT.**

***Index Terms*—Double gate, grain boundary, leakage current, polysilicon, pseudosubthreshold, thin film transistor (TFT), traps, two-dimensional simulation.**

I. Introduction

THIN film transistors (TFTs) made with amorphous silicon (a-Si) and polysilicon represent an interesting field of study for their application in flat-panel active-matrix liquid crystal displays (AMLCDs) [1], [2]. For these applications, scaled-down poly-Si TFTs with high performance and high reliability are required [3]. However, the performance of conventional poly-Si TFT is far from satisfactory to meet the current drive requirements for these applications [4]. One of the problems of poly-Si TFTs is the large OFF-state leakage current due to the presence of the grain boundaries (GBs) in the channel [5], which results in poor switching characteristics. Various solutions such as the offset gate, the p-n-p gate, and the lightly doped drain (LDD) poly-Si TFT structures have been proposed to reduce the OFF-state leakage currents [6]–[9]. Also, it has been shown that double-gate structures are able to improve the current drivability, short channel effects, and subthreshold slope of these devices. [10]–[12].

In recent years, it has become possible to control the grain growth and create devices where only a single or a small number of discrete GBs exist in the channel of the poly-Si TFT [13], [14], using modern metal-induced lateral crystallization (MILC) or excimer laser annealed (ELA) methods. This has led to high-performance poly-Si TFTs [15]–[17] typically with one or fewer GBs in the channel [11], [15]. Therefore, the channel lengths of the poly-Si TFTs are now aggressively scaled down to submicrometer lengths [18], [19]. Unfortunately, when compared to the silicon-on-insulator (SOI) MOSFETs, the OFF-state leakage currents in these advanced poly-Si TFTs are unacceptably larger.

The dominant conduction mechanism in a conventional SOI MOSFET is due to the inversion charge density modulated by the gate (ICMG) [20], resulting in a steep subthreshold slope in their transfer characteristic. However, the gate-induced grain barrier lowering (GIGBL) is the dominant conduction mechanism in a poly-Si TFT below the turn-ON region [21]. The transfer characteristic of a poly-Si TFT, therefore, consists of a subthreshold region and a pseudosubthreshold region [21], [22]. The challenge that we have addressed in this paper, therefore, is to examine if we can force the poly-Si TFT to perform like a single-crystal SOI MOSFET by converting the dominant channel-conduction mechanism from GIGBL to accumulation charge density modulation by the gate (ACMG) [23] as SOI MOSFETs. This should result in a complete absence of pseudosubthreshold region in the transfer characteristic following a steep subthreshold slope, and a significantly diminished OFF-state leakage current, without affecting the ON-state current.

In this paper, considering one and three GBs in the channel of the poly-Si TFT [13]–[17] and combining with the advantages of double-gate structures, we propose for the first time, a new device structure called the poly-Si multiple-gate TFT (MG-TFT), in which the top gate consists of two side gates with different work functions. Using the two-dimensional (2-D) simulator MEDICI [24], we first explain how the presence of the side gates will shift the channel-conduction mechanism from GIGBL to ACMG, and compare the performance of MG-TFT with that of the asymmetrical double-gate poly-Si TFT (DG-TFT). We have also studied the effect of varying: 1) the side-gate parameters; 2) number of channel GBs; and

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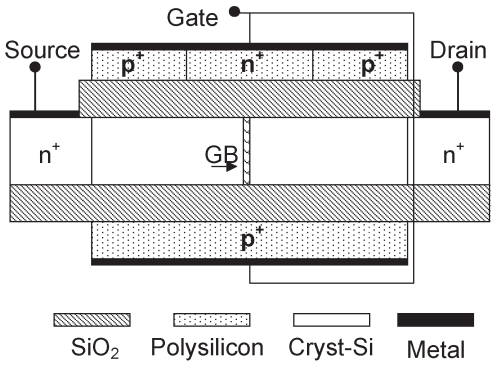


Fig. 1. Cross-sectional view of the asymmetrical MG-TFT.

3) the temperature on the performance of the device. Compared to the DG-TFT, we demonstrate that the proposed MG-TFT exhibits significantly reduced leakage current, making it an extremely reliable device configuration for high-performance poly-Si TFT applications.

II. MG-TFT Structure and Simulation Parameters

Fig. 1 shows a schematic cross-sectional view of the MG-TFT implemented in the 2-D device simulator MEDICI. This is an asymmetrical double-gate structure under the main gate because the top-gate region consists of p^+-poly and n^+-poly for the side gates and the main gate, respectively, and the bottom gate is made of p^+-poly. The following assumptions are made: 1) a single GB is present in the center of the undoped poly-Si channel; and 2) the regions on both sides of the GB are completely defect free so that all the defect states are localized in the GB. A conventional drift-diffusion method is used to model the carrier transport, and the Shockley–Read–Hall recombination model is used for the capture and emission processes. Based on the work of Kitahara *et al.* [26], we have employed the Caughey–Thomas model [25] for the carrier mobility (the typical values of electron and hole mobility are 700 and 130 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, respectively). We have also included the impact ionization model [27] for considering the effect of electric field associated with the GB on device performance. The simulation parameters of the structure are given in Table I. The main-gate and the side-gate lengths (L_M and L_S) are identical and the channel length $L(=2L_\mathrm{S}+L_\mathrm{M})$ is kept constant at 0.4 μm. All the device parameters of the MG-TFT are equivalent to those of the DG-TFT and the DG-SOI structures. A similar simulation approach has been used by Walker *et al.* [18] to prove the validity of their model. In many applications, such as active-matrix liquid crystal displays (AMLCDs), the polarity between the source and drain of poly-Si TFT is required to be altered to reduce the dc stress of liquid crystals [28]. Therefore, in the proposed MG-TFT, we have used identical lengths for the side gates on both sides of the main gate.

TABLE I
Parameters for the MG-TFT Structure Used in MEDICI Simulation

Parameter	Value
Doping in n^+ source/drain	10^{19} cm^{-3}
Trap density at the grain boundary	10^{13} cm^{-2}
Electron trap energy relative to the conduction band	0.51 eV
Hole trap energy relative to the valence band	0.51 eV
Capture rate for electrons and holes	10^{-8} cm^3/sec [18]
Width of the grain boundary (GB)	10 nm
Thickness of the polysilicon channel layer	50 nm
Top/bottom gate oxide thickness	10 nm
Channel length L	0.4 μm
p^+-poly gate work function	5.25 eV
n^+-poly gate work function	4.17 eV

III. Performance Considerations and Discussion

A typical MEDICI-simulated 2-D conduction-band potential distribution for MG-TFT and DG-TFT structures for $V_\mathrm{DS}=0$ V is shown in Fig. 2. We note from Fig. 2(a) that a central potential barrier is present at the GB. This is due to the carrier immobilization by the traps at the GB [29], [30]. Also, due to the asymmetrical nature of the main gate, the potential distribution is almost linear in the channel [31]. Therefore, the dominant conduction mechanism of the DG-TFT is determined by GIGBL. However, in the proposed MG-TFT, due to its multiple-gate structure, in addition to the central barrier, two extra barriers (side barriers) are created in the side-gate regions because of the work-function difference between the side gate and the main gate, as shown in Fig. 2(b). The side and central barriers not only differ in their height but also in their shape. It is worth noting that the MG-TFT is an asymmetrical structure under the main gate, while it is a symmetrical structure under the side gate, and is the main point why the side barriers are produced in the structure. As a result, the dominant conduction mechanism in the MG-TFT should be controlled by the side barriers since the central barrier does not play any significant role. This should lead to a steep subthreshold slope in the transfer characteristic of the device, just as in the case of a typical DG-SOI MOSFET, as shown in Fig. 3, in which the transfer characteristics of the MG-TFT are compared with that of the DG-TFT and the DG-SOI MOSFET. Because of the steep subthreshold slope, the MG-TFT will have several orders of magnitude lesser OFF-state leakage current when compared to the DG-TFT. This has become possible by nullifying the effect of the central barrier associated with the GB on the channel-conduction mechanism so that the pseudosubthreshold region is almost eliminated. It is worth noting that the side barriers are created very well even at a higher drain voltage, as shown in Fig. 4, for $V_\mathrm{GS}=0$ V and $V_\mathrm{DS}=1$ V. Therefore, the MG-TFT should exhibit a reduced leakage current, both in linear as well as saturation regions, when compared to the DG-TFT.

With increasing gate voltage, however, the height of the side barrier will decrease, and at some critical gate voltage (V_CGS), the side-barrier height will become equal to the central-barrier height. After this critical-gate-voltage (V_CGS) condition is reached, the channel-conduction mechanism will be determined by GIGBL. The value of critical gate voltage V_CGS at which the central-barrier height becomes equal to the side-barrier height

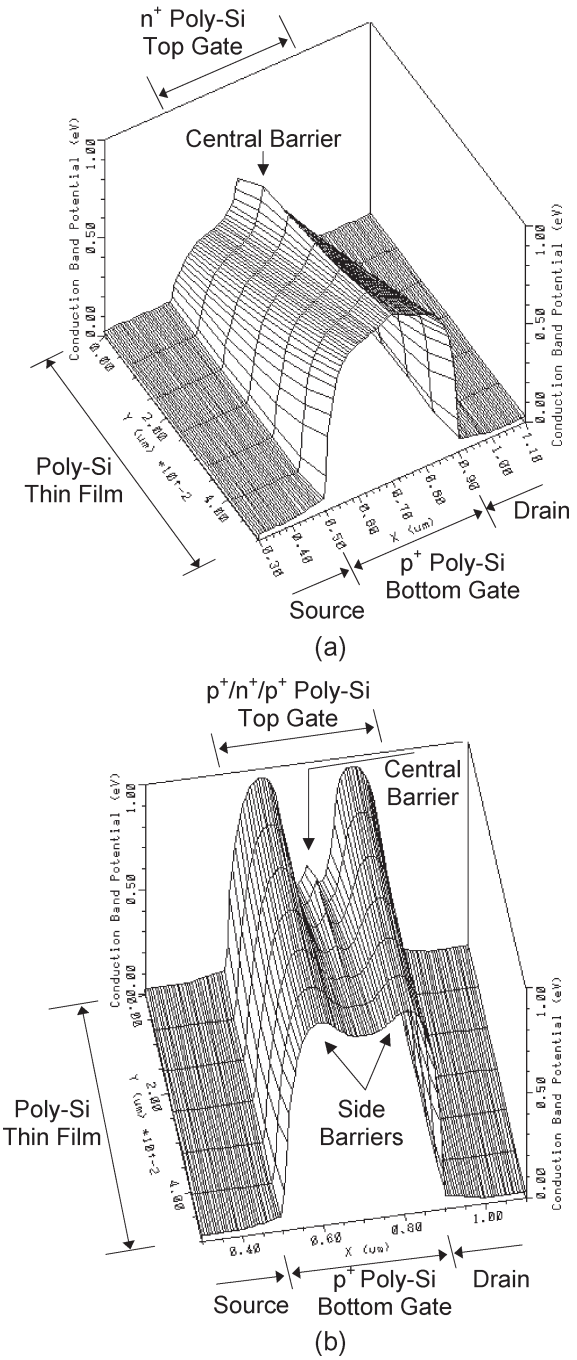


Fig. 2. Conduction-band potential distribution for (a) DG-TFT and (b) MG-TFT structures for $V_{\rm GS} = 0$ V and $V_{\rm DS} = 0$ V.

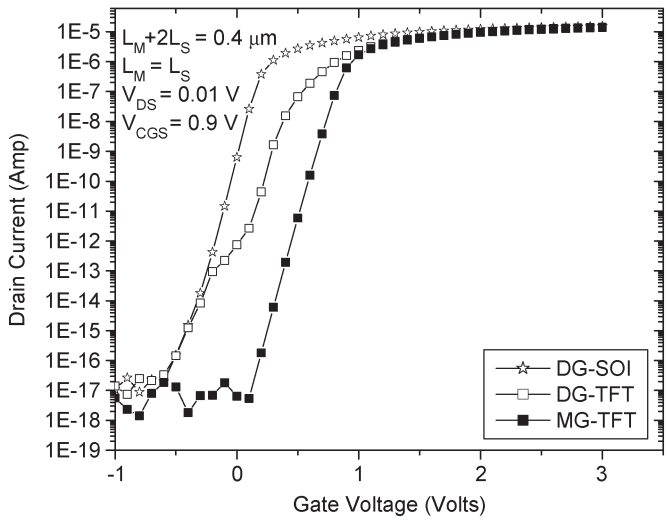


Fig. 3. Transfer characteristics of MG-TFT, DG-TFT, and DG-SOI structures.

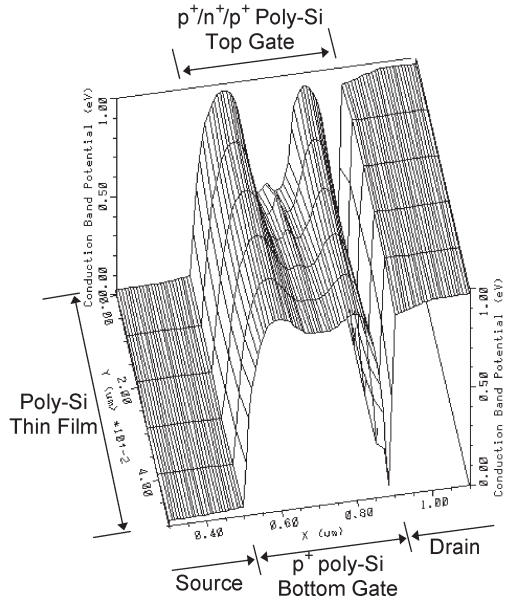


Fig. 4. Conduction-band potential distribution for the MG-TFT structure with $V_{\rm GS} = 0$ V and $V_{\rm DS} = 1$ V conditions.

is very important in controlling the pseudosubthreshold region, and hence, the reduction in the OFF-state leakage current. If the critical gate voltage $V_{\rm CGS}$ is near 0 or negative, the MG-TFT structure is not very useful in improving leakage current and will behave like the DG-TFT. On the other hand, if the critical voltage $V_{\rm CGS}$ is near the ON voltage, the MG-TFT structure will not exhibit the pseudosubthreshold region. The work function of the side gate $(\varphi_{\rm Msg})$ strongly determines the value of $V_{\rm CGS}$. Fig. 5 shows the transfer characteristic of the MG-TFT for different values of the side-gate region work function. The critical gate voltage $V_{\rm CGS}$ will reduce with decreasing work function of the side-gate region due to the height of the side barriers. Therefore, it is very important to choose the appropriate work function for the side gate for a given main-gate work function $(\varphi_{\rm Mmg})$. It is worth noting that the work function of the bottom gate is fixed and is equal to 5.25 eV in our analyses.

The transfer characteristics of the MG-TFT are compared with that of the DG-TFT in Fig. 6 for different channel lengths ranging from 0.2 to 1.0 μm. The slope of the subthreshold region will improve as the channel length increases [32], as is commonly observed in the DG-SOI MOSFETs. In addition, the critical voltage $V_{\rm CGS}$ will not change significantly for larger channel lengths due to a reduction in the interaction between side and central barriers.

It is well known that the conductivity in a polycrystalline TFT is strongly dependent on the trap density at the GBs [29], [30], [33], [34]. To estimate the effect of traps, we have compared the transfer characteristics of MG-TFT and DG-TFT

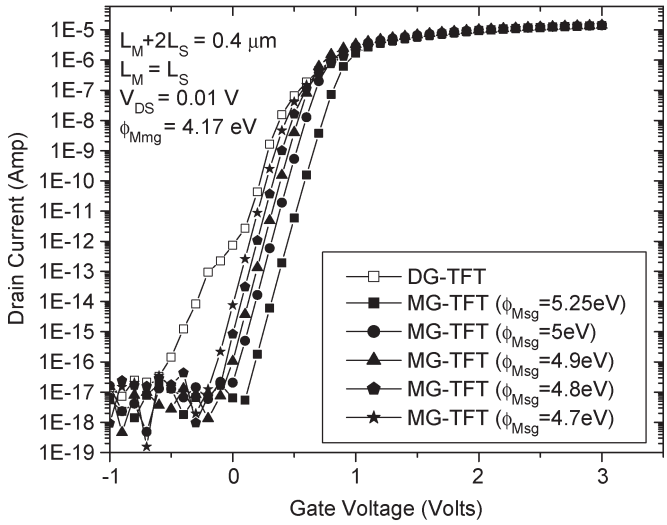


Fig. 5. Transfer characteristic of the MG-TFT structure for different work functions of the side gates.

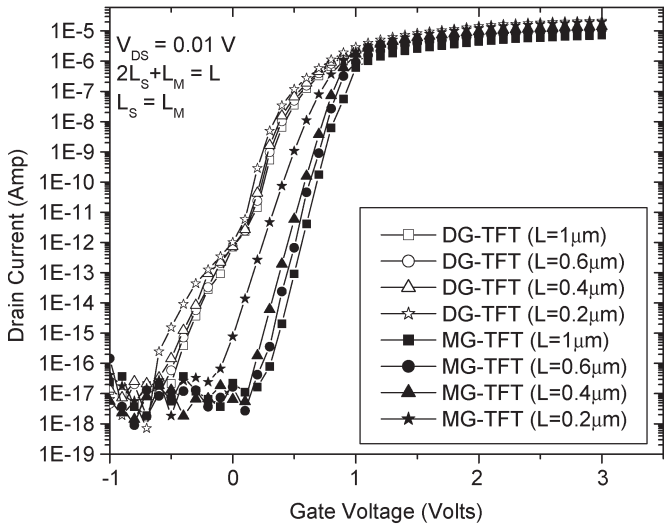


Fig. 6. Transfer characteristics of MG-TFT and DG-TFT for different channel lengths.

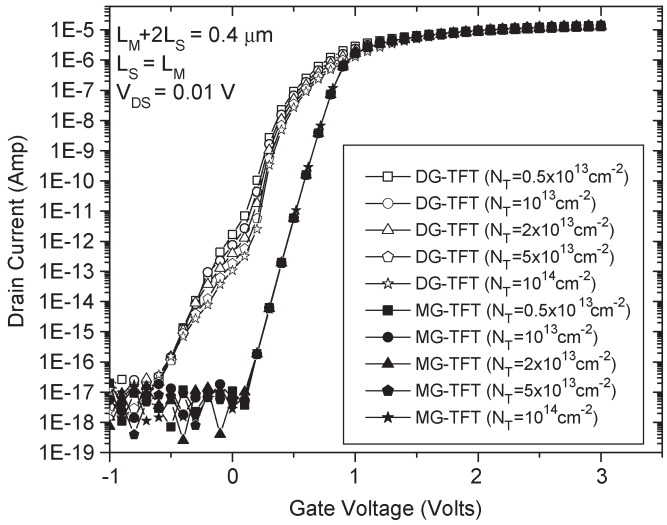


Fig. 7. Transfer characteristics of MG-TFT and DG-TFT for different trap densities. The values of central-barrier height at the center of the GB for trap densities 5×10^{12}, 10^{13}, 2×10^{13}, 5×10^{13}, and 10^{14} cm^{-2} are 0.65, 0.67, 0.7, 0.72, and 0.74 eV, respectively, for $V_{\rm GS} = 0$ V and $V_{\rm DS} = 0$ V.

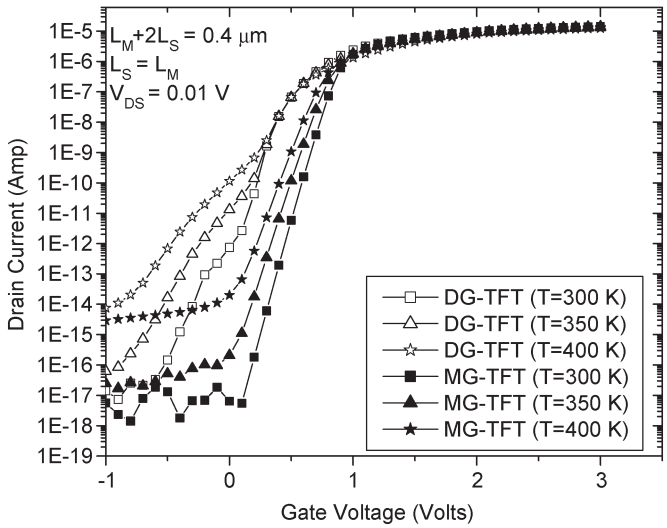


Fig. 8. Transfer characteristics of MG-TFT and DG-TFT for different temperatures.

structures in Fig. 7 for different trap densities. As the trap density increases, the pseudosubthreshold region will be more gradual in the DG-TFT structure. However, there is no significant change in the subthreshold slope of the MG-TFT since, in this structure, the subthreshold slope is dependent on side-barrier height and not on the central GB barrier height. Therefore, even if the GB trap density is large, the OFF-state leakage current in the MG-TFT structure is significantly smaller compared to the DG-TFT.

An increase in temperature significantly affects the performance of the poly-Si TFTs due to their gradual subthreshold slope, unlike in the case of the SOI MOSFETs. We have compared the temperature dependence of the transfer characteristics of MG-TFT with that of the DG-TFT in Fig. 8. The MG-TFT exhibits a much smaller OFF-state leakage current and a steeper subthreshold slope when compared to the DG-TFT, even at 400 K, which makes the MG-TFT much more reliable at higher temperatures than the DG-TFT.

IV. Design Considerations of MG-TFT

In all our simulations above, we have chosen the main-gate length $L_{\rm M}$ equal to the side-gate length $L_{\rm S}$ [35]–[38] as this results in a very low OFF-state leakage current. Fig. 9 shows the transfer characteristic of the MG-TFT for different side-gate lengths, and it is clearly seen that there is no significant change in the critical gate voltage $V_{\rm CGS}$ when the side-gate length is reduced with respect to the main-gate length. However, as demonstrated in the case of a dual material gate (DMG) SOI MOSFET [35]–[38], the subthreshold slope is steeper and the leakage current is the lowest when the side-gate length is equal to the main-gate length.

When the gate-oxide thickness is reduced, the gate control over the channel improves, leading to a reduction in the subthreshold slope, making the device near ideal. The gate-oxide thickness is, therefore, an important parameter in the design

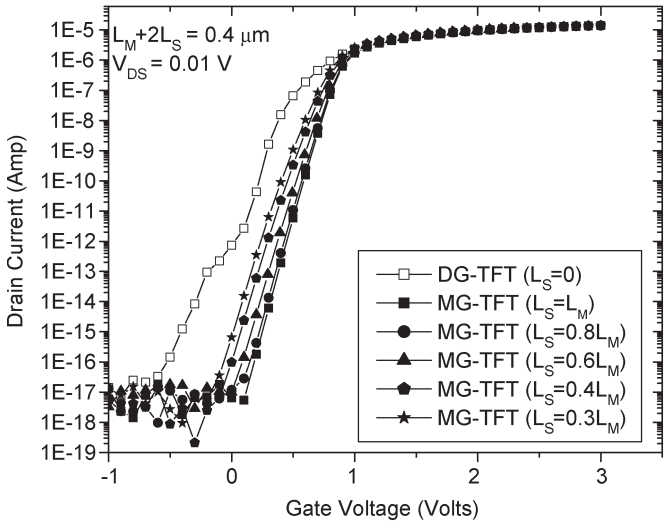


Fig. 9. Transfer characteristics of MG-TFT for different side-gate lengths. $L_{\rm M}$ and $L_{\rm S}$ are the main- and side-gate lengths, respectively. The channel length $(L = 2L_{\rm S} + L_{\rm M})$ is fixed at 0.4 μm.

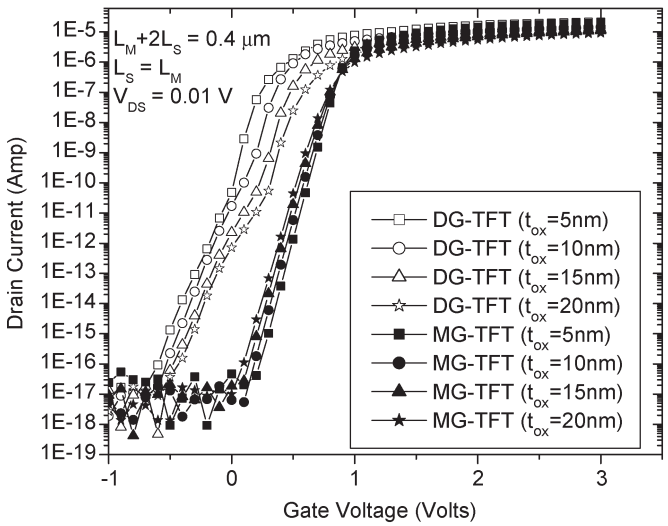


Fig. 10. Transfer characteristics of MG-TFT and DG-TFT for different gate-oxide thicknesses.

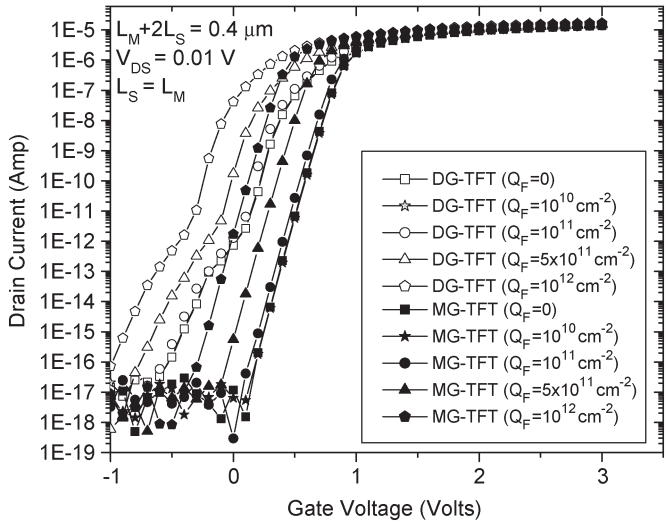


Fig. 11. Transfer characteristics of MG-TFT and DG-TFT for different fixed charges at the interface between the top/bottom gate and poly-Si thin film.

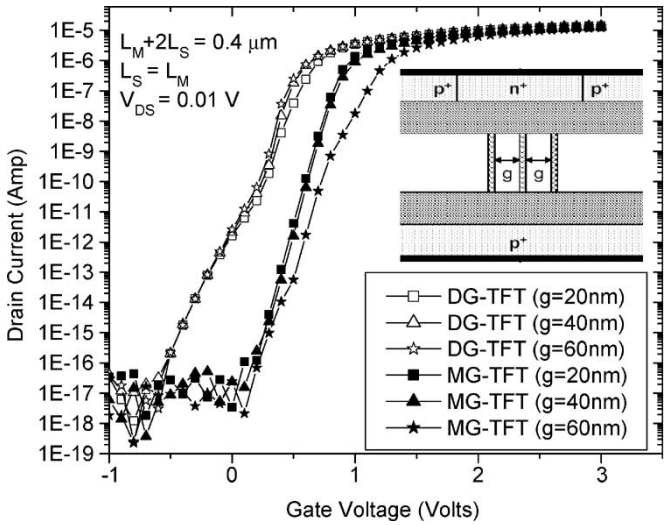


Fig. 12. Transfer characteristics of MG-TFT and DG-TFT for three GBs in the main channel.

of the poly-Si TFT. Fig. 10 shows the transfer characteristics of MG-TFT and DG-TFT for different gate-oxide thicknesses. When the gate-oxide thickness reduces, the MG-TFT exhibits near-ideal transfer characteristics, while the DG-TFT has a significantly large OFF-state leakage current even at a low gate-oxide thickness.

The influence of charges at the oxide/poly-Si interface is an important issue. The presence of these charges is unavoidable in practical devices. To investigate the effect of fixed charges at the interface between top/bottom gate and poly-Si thin film, the transfer characteristics of the MG-TFT and DG-TFT structures are shown in Fig. 11 for different fixed charge densities. As can be seen from the figure, there is no significant change in the transfer characteristics if the fixed charge density is either 0 or 10^{10} cm^{-2}. The latter value can be easily realized under good fabrication conditions. If the fixed oxide charge density increases beyond this value, there is an increase in the OFF-state leakage current of both MG-TFT and DG-TFT. However, the OFF-state leakage current of MG-TFT is still orders of magnitude smaller than that of the DG-TFT. Therefore, it shows that the idea of converting the dominant channel-conduction mechanism from GIGBL to ACMG works very well even in the presence of fixed charge densities at the oxide/polysilicon interface.

The positioning of the GB relative to the source and drain is difficult in a real device. Therefore, the GB position in the channel is very important in MG-TFT. However, our simulation results show that there is no significant change in the transfer characteristic of the MG-TFT even if there is a 20% shift in the position of the GB with respect to the center of the channel. If the GB is very close to the source, the interaction between the side barrier and central barrier will increase and it may affect the extent to which the leakage current can be reduced.

Another important question that needs to be addressed is what happens if there are multiple GBs in the channel of the

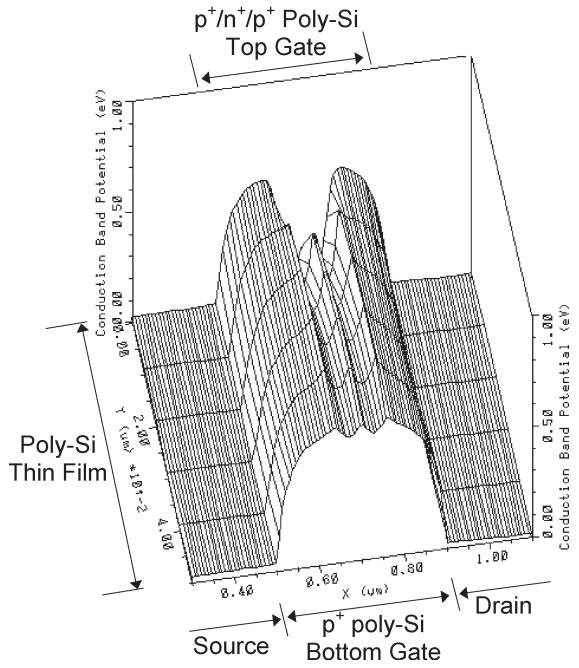


Fig. 13. Conduction-band potential distribution of the MG-TFT structure with three GBs in the channel ($g = 60$ nm) for $V_{\rm GS} = 0.5$ V and $V_{\rm DS} = 0.01$ V.

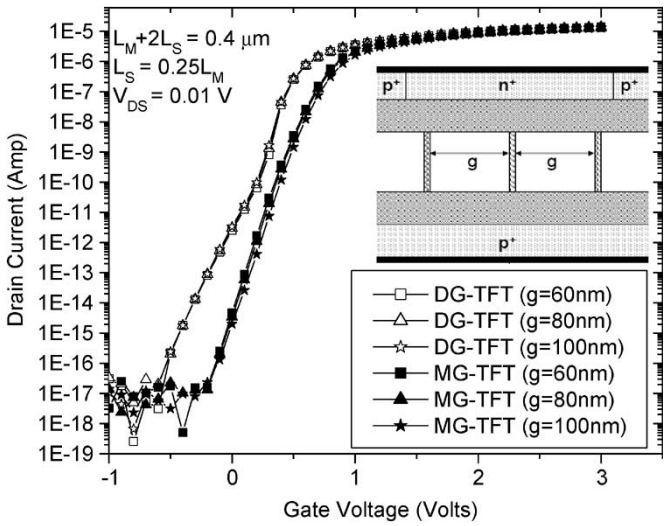
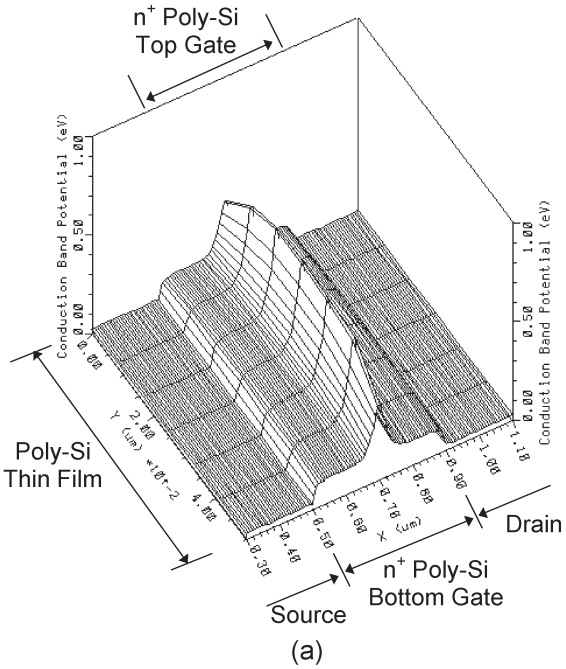


Fig. 14. Transfer characteristics of MG-TFT and DG-TFT for three GBs in the channel for small side-gate length ($L_{\rm S} = 0.25 L_{\rm M}$).



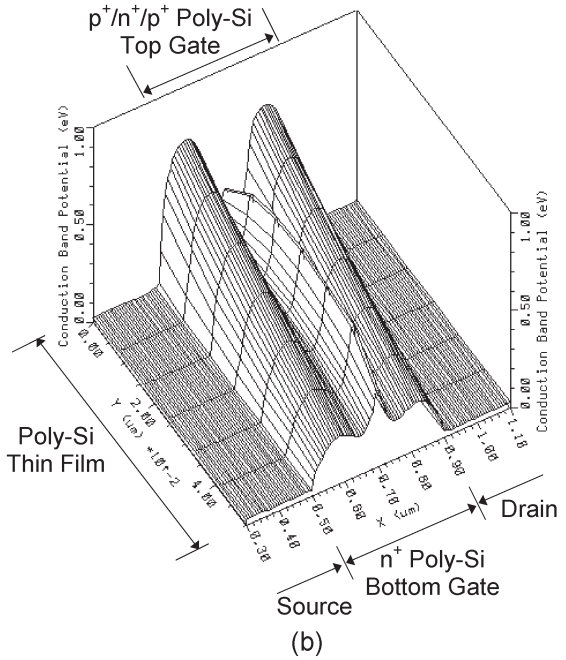


Fig. 15. Conduction-band potential distribution for (a) SDG-TFT and (b) SMG-TFT structures for $V_{\rm GS} = 0$ V and $V_{\rm DS} = 0$ V. The SMG-TFT structure is a multiple-gate structure made on an SDG-TFT.

MG-TFT. To study this effect, we have considered three GBs in the channel and different distances between the grains. Fig. 12 shows a comparison of the transfer characteristic of the MG-TFT with the DG-TFT. Undoubtedly, the OFF-state leakage current of the MG-TFT structure is significantly small even in the presence of multiple GBs in the channel, while the pseudosubthreshold slope in the DG-TFT further deteriorates. However, when the GBs are separated by a larger distance ($g = 60$ nm in the figure), the transfer characteristic becomes similar to that of DG-TFT due to the interaction between the side-gate barriers and GB trap barriers. Fig. 13 shows a disturbance in the conduction-band potential distribution of the MG-TFT structure, for $V_{\rm GS} = 0.5$ V and $V_{\rm DS} = 0.01$ V, having three GBs in the channel, with a 60-nm separation between the grains. We notice that the shape of the side barriers has changed and the height of trap barriers is slightly larger than the side barriers at $V_{\rm GS} = 0.5$ V. However, even in this case, the leakage current of the MG-TFT is significantly better than that of the DG-TFT. Therefore, the location of GBs is very important in eliminating the pseudosubthreshold region, and hence, the reduction in the OFF-state leakage current. However, even if the distance between the grains is too large, the pseudosubthreshold region can still be eliminated if the side-gate barriers are moved away from the GB barriers by choosing appropriate values of $L_{\rm S}$ and $L_{\rm M}$, as shown in Fig. 14. The important point that needs to be noted from above is that for eliminating the

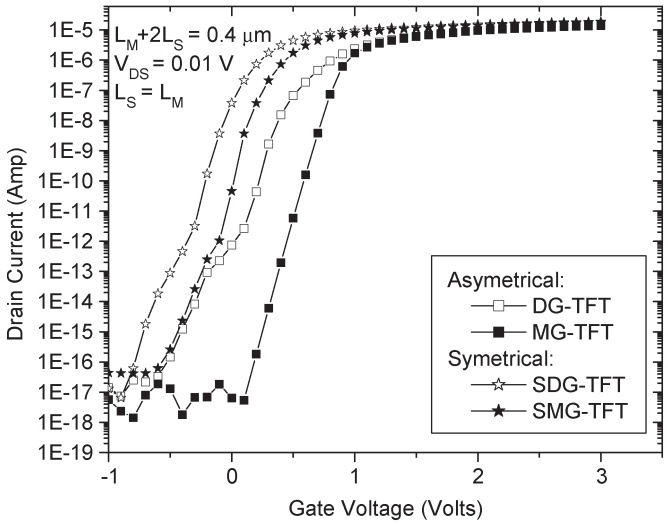


Fig. 16. Transfer characteristics of DG-TFT, MG-TFT, SDG-TFT, and SMG-TFT structures. The DG-TFT and MG-TFT are asymmetrical structures, while the SDG-TFT and SMG-TFT are symmetrical structures under the main gate.

pseudosubthreshold region, the side-gate potential barriers should not be too close to the GB potential barrier.

V. Comparison Between Asymmetrical/Symmetrical MG-TFTs

In this section, we analyze the possibility of applying the MG-TFT structure to a symmetrical DG-TFT (SDG-TFT) in which both the top and bottom gates are made of n^+-poly. The conduction-band potential distribution of the SDG-TFT structure is shown in Fig. 15(a), in which the central barrier is created in the center of the channel due to the presence of the GB. For this SDG-TFT, if the multigate concept is applied (let us call the resulting structure SMG-TFT), the top gate consists of p^+-poly and n^+-poly for the side and main gates, respectively, and the bottom gate is made of n^+-poly. The conduction-band potential distribution of the SMG-TFT is shown in Fig. 15(b). Comparing this potential distribution with that of the asymmetrical MG-TFT shown in Fig. 2(b), we note that the multiple-gate concept does not work well for the SMG-TFT since the side barriers are not formed properly, allowing the dominant conduction mechanism in the channel to be controlled by GIGBL and not by ACMG. This can also be observed clearly from Fig. 16, in which the transfer characteristics of the SDG-TFT, known as SMG-TFT, are compared with that of the MG-TFT. Since the side-barrier height is comparable to that of the central barrier (and even less near the bottom gate) in the case of the SMG-TFT, the pseudosubthreshold region is still present, resulting in no special advantage in terms of reducing the OFF-state leakage current, while the MG-TFT structure works very well.

VI. Conclusion

For the first time, we have demonstrated in this paper that by applying a multiple-gate concept to the front gate of an asymmetrical DG-TFT, the OFF-state leakage current can be reduced significantly, improving the performance of DG-TFTs in AMLCD or other applications. In the proposed poly-Si MG-TFT, due to the presence of side barriers that are more dominant than the central potential barrier associated with the GBs, the dominant conduction mechanism in the channel is controlled by the ACMG [20] and not by the GIGBL. As a result, the pseudosubthreshold region is eliminated, resulting in several orders of magnitude reduction in the OFF-state leakage current with no detectable change in the ON voltage. The effect of varying the channel length, gate-oxide thickness, number of GBs, trap density at the GBs, temperature, and the work function of the gate material are also studied. Our studies also show that the MG-TFT idea does not work satisfactorily in the case of an SDG-TFT structure. We expect that the proposed structure should be of great practical importance in many advanced poly-Si TFT applications in which power dissipation due to OFF-state leakage current is a major problem.

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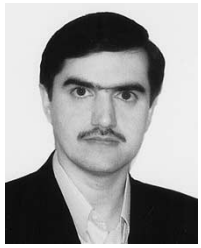

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