Department of Mechanical Engineering
Indian Institute of Technology New Delhi
I Semester -- 2026 – 2027

MCL 348 THERMAL MANAGEMENT OF ELECTRONICS

Practice Problems on Compact Thermal Modelling

Ques 1. – The physical structure depicted in Fig. 1 is a TO-247 package mounted on an extruded, finned, free convection-cooled sink without any insulating interface but with thermal grease. The device itself is bounded to the header using solder or epoxy; the header is made part of a package that is mounted to a heat sink (perhaps with some intervening insulating material); and the heat sink is thermally connected to the ambient environment, generally through free or forced convection. Draw an equivalent thermal resistance network for the given die package. Also, typical values of the thermal resistances of the die, interface1, header, interface2, and heat sink are 1.1, 0.032, 0.12, 0.08 and 1.8, respectively, all units being °C/ W. Calculate the junction temperature for 25W power dissipation if the ambient temperature is 40°C and comment on the safety of die package.

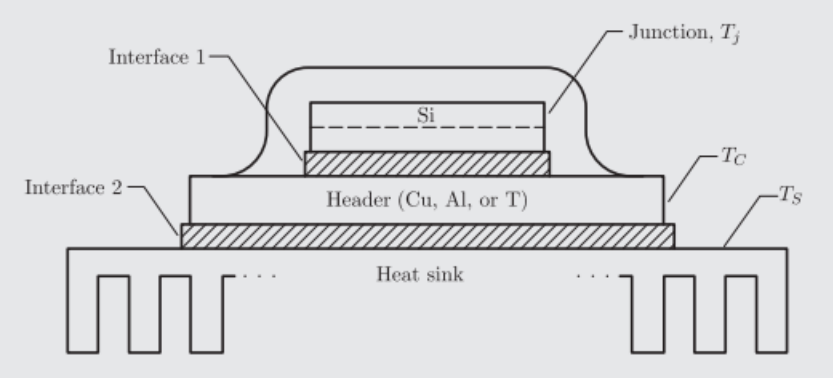


Fig. 1 – Typical mechanical structure used for mounting semiconductor die.

Ques 2. – Figure 2 shows two identical devices, Q1 and Q2, mounted on a common heat sink. The devices are in TO-220 packages and have a thermal resistance from junction to case of $R_{\theta jc}$ = 1.2 °C/ W. The interface between the case and sink has a thermal resistance of $R_{\theta jc}$ = 0.20°C/W, and the thermal resistance between the sink and ambient is $R_{\theta SA}$ = 0.8 °C/ W.

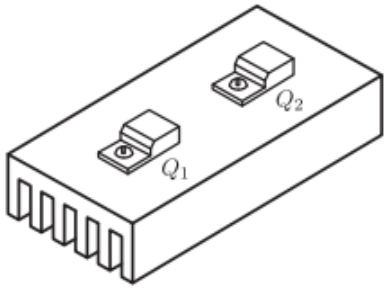


Fig. 2 – TO-220 die Package

(a) Draw the static thermal model for the thermal system of Fig. 2.

(b) If the devices are dissipating the same power, and Ta = 40°C, what is the maximum total power that can be dissipated if $T_{j\,max}$ = 150°C?

(c) What is the maximum possible power dissipated if only one of the devices is operating?

Ques 3. – Construct an equivalent thermal resistance model for the die package shown below: a) Consider convection heat transfer only, b) Consider both radiation and convection heat transfer modes between package and ambient.

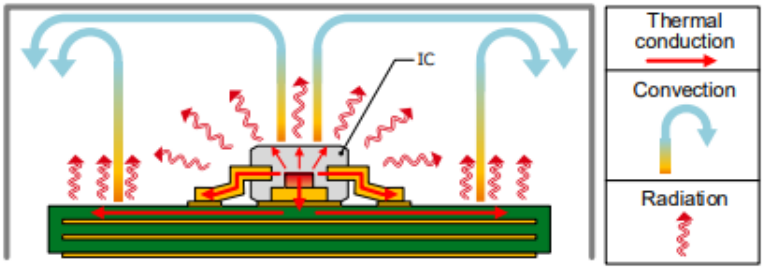


Fig. 3 – Cross-sectional diagram of surface-mounted package IC on PCB

Ques 4. - A cross-sectional view of a single-chip BGA package is shown in Figure 4. The package has been provided with various temperature nodes that must be considered when constructing a thermal network of resistances. Construct a thermal network to estimate the junction temperature of the package using the information given below –

Parameter	Value
Power	2W
Junction-case resistance	1°C/W
Junction-board resistance	5°C/W
Air-gap resistance	2°C/W

Parameter	Value
Convection resistance	65°C/W
PCB resistance	33°C/W
Skin resistance	0.039°C/W

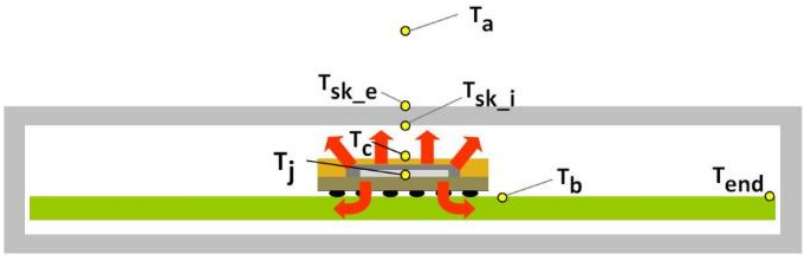


Fig. 4 – Cross-sectional view of single-chip BGA package

Ques 5. - Construct an equivalent thermal resistance model for the given below die packages

a) Lateral multi-chip package

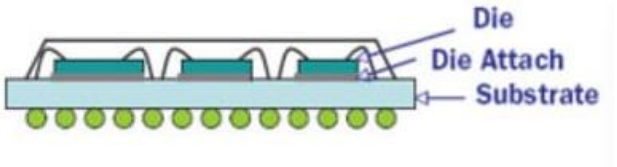


Fig. 5a – Simplified thermal circuit diagram for Lateral Multi-chip package

b) Figure 5b shows a Flip Chip package with different defects. Construct equivalent thermal resistance models for all the sections of the flip chip, considering the direction of heat flow in the package.

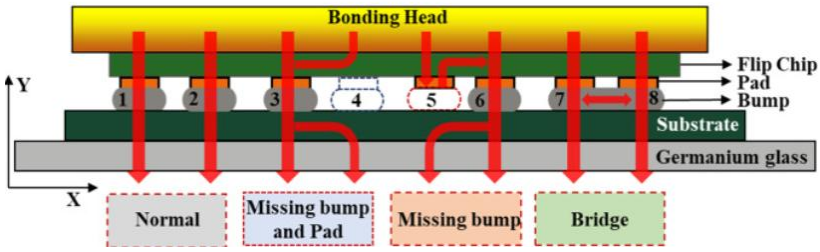


Fig. 5b – Flip-Chip package with different defects.

c) Chip packing with lead frames on PCB

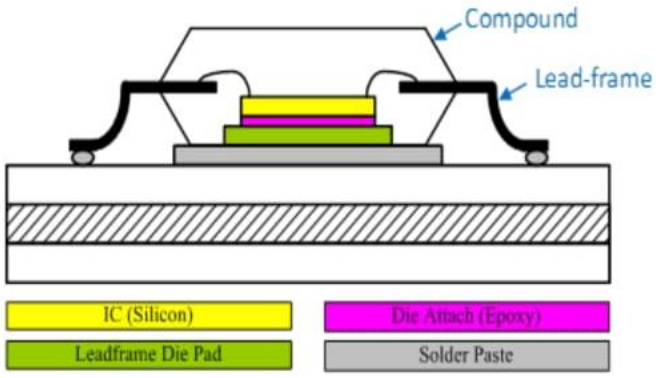


Fig. 5c – Cross-sectional view of chip package on PCB

d) Chip package on PCB with thermal vias, leading to conduction heat transfer in both vertical and horizontal directions.

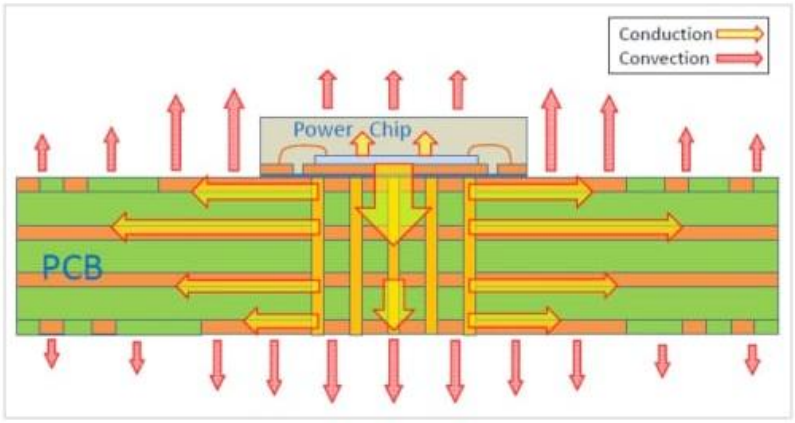


Fig. 5d – Chip package mounted on PCB

Ques 6. – Figures 6a & 6b show the different chip packing methods. Construct an equivalent thermal resistance model for these packages.

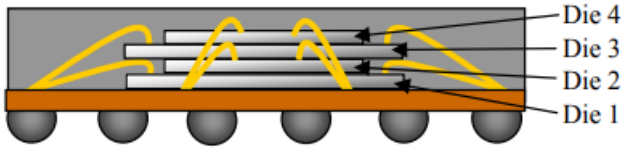


Fig. 6a – Typical 4-Die Stacked Chip Scale Package (SCSP)

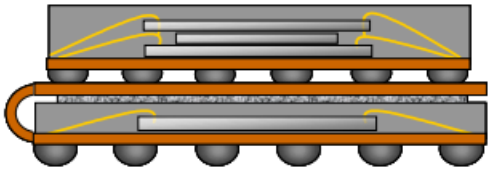


Fig. 6b – A schematic of the package showing stacked-die and stacked-package

Ques 7. – Figure 7 illustrates the typical schematic of chiplet 2.5D integration, whereby two chiplets are mounted to an interposer via micro bumps, and the interposer is bonded to the substrate using C4 bumps. The underfill is filled in between the chiplets and the interposer, as well as between the interposer and the substrate. A Cu heat sink as the lid is attached to the top surface of the chiplets and the substrate via TIM and adhesive. This type of cooling scheme is called near-chip cooling. Draw an equivalent thermal model for this chip package.

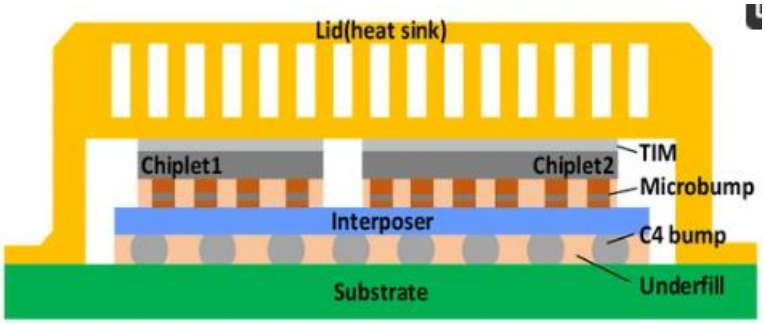


Fig. 7 - Schematic of near-chip cooling for chiplet 2.5D integration

Ques 8. - Consider a 50 mm × 50 mm × 5 mm silicon block sandwiched between two different composite layers as shown in a representative cross-section below. The composite layer on the right consists of a 0.5 mm thick thermal paste with a thermal conductivity of 10 W/m °C and a 1 mm-thick copper spreader with a thermal conductivity of 395 W/m °C. The composite layer on the left is made of 25 pairs of 1 mm × 1 mm × 50 mm solder with thermal conductivity of 40 W/m °C, and 1 mm × 1 mm × 50 mm underfill with thermal conductivity of 1 W/m °C that are connected to a 2 mm-thick PCB. The PCB is made of glass epoxy with a thermal conductivity of 0.35 W/m °C and four copper layers, each 0.035 mm thick. The convection heat transfer coefficient on the left and right sides of this composite layer is 30 W/m^2 °C and 5 W/ m^2 °C, respectively.

a. What is the normal thermal resistance of the PCB?

b. Calculate thermal resistance between the left side of the silicon layer and the fluid at temperature $T_{\infty,1}$, and the right sides of the silicon layer and the fluid at temperature $T_{\infty,2}$

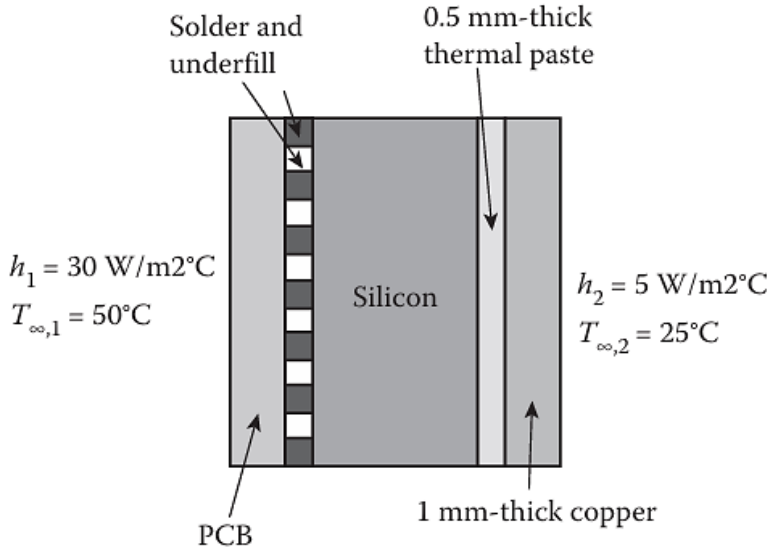


Fig. 8 – Cross-sectional view of the sandwiched silicon block

Ques 9. - Consider a 50 mm × 50 mm × 2 mm electronic device with junction-to-case thermal resistance of 5°C/W and junction-to-board thermal resistance of 15°C/W. This device is mounted on a 50 mm × 50 mm printed circuit board (PCB) with a thickness of 2 mm. The PCB is made of glass epoxy with a thermal conductivity of 0.35 W/m °C. However, 20 copper fillings with a diameter of 0.5 mm are added to the PCB to increase its normal thermal conductivity. The convection heat transfer coefficient over the top of the device and the bottom of the PCB is 25 W/m^2 °C and 5 W/m^2 °C, respectively, and the thermal conductivity of copper is 390 W/m °C.

a. What is the case-to-air thermal resistance of this device?

b. What is the normal thermal resistance of the PCB?

c. What is the thermal resistance between the bottom of the PCB and air?

d. Sketch the total resistance network between the junction of this device and air and obtain the junction-to-air thermal resistance of this device.

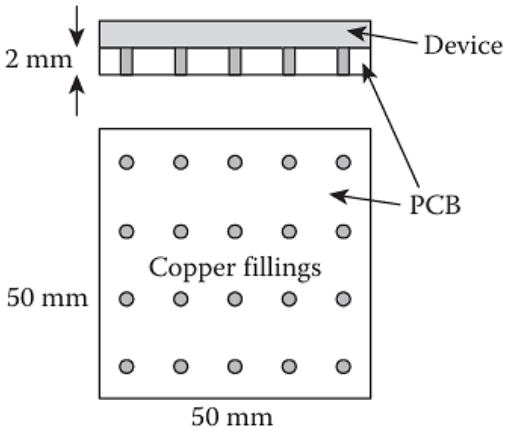


Fig. 9 – Front and Top view of PCB with thermal vias

Ques 10. Consider an electronic package in which a 12 mm × 12 mm × 0.8 mm silicon die is attached to a 35 mm × 35 mm × 1 mm copper cap through a 0.25 mm thick thermal interface material (TIM) as shown below. This package is mounted on a PCB and air with a laminar velocity of U∞ = 2 m/s is flowing over the package. If thermal conductivity of silicon, TIM, and copper are 125 W/m °C, 10 W/m °C, and 390 W/m °C, respectively, calculate junction-to-case and case-to-air thermal resistances of this package.

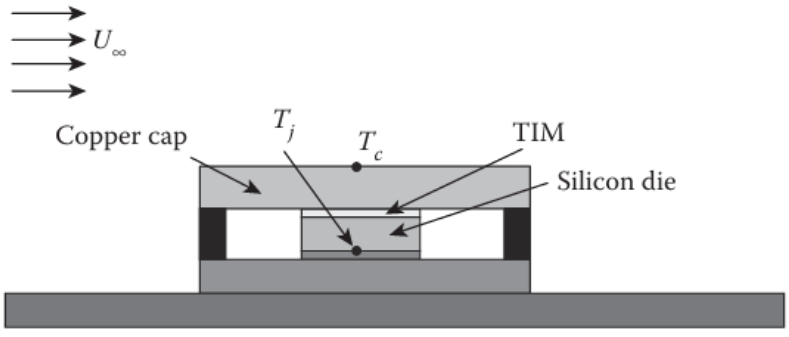
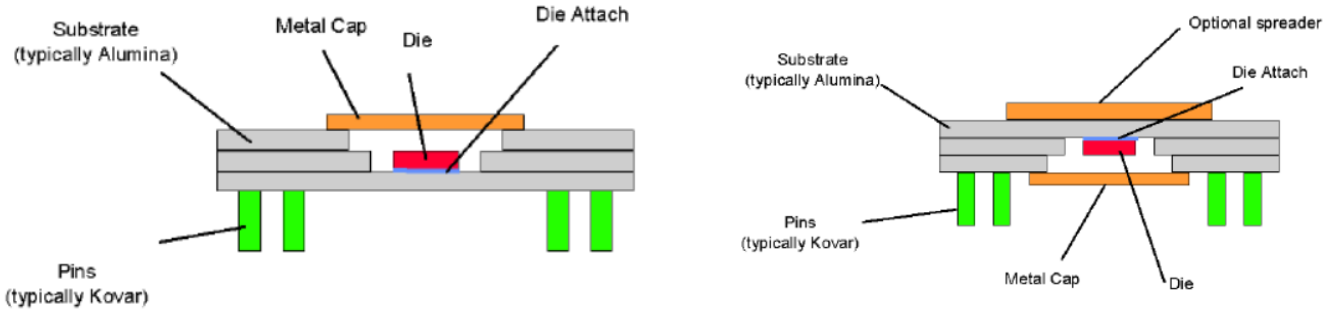


Fig. 10 – Schematic picture of electronic package

Ques 11. Figure 11 shows two configurations of the electronic package of Ceramic Pin Grid Array (CPGA). Construct an equivalent thermal resistance model for these packages.



(a) (b)

Fig. 11 – Different Electronic Packages of CPGA (a) Cavity-Up CPGA, (b)Cavity-Down CPGA

Solved problems related to Equivalent Thermal Network of Chip Packages.

Ques 12. – Construct an equivalent thermal resistance network of a PCB in a half-bridge configuration shown in figure 10 below.

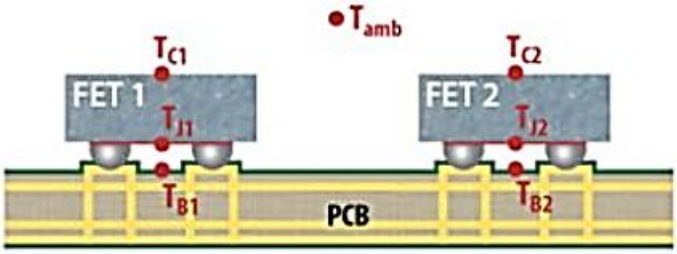
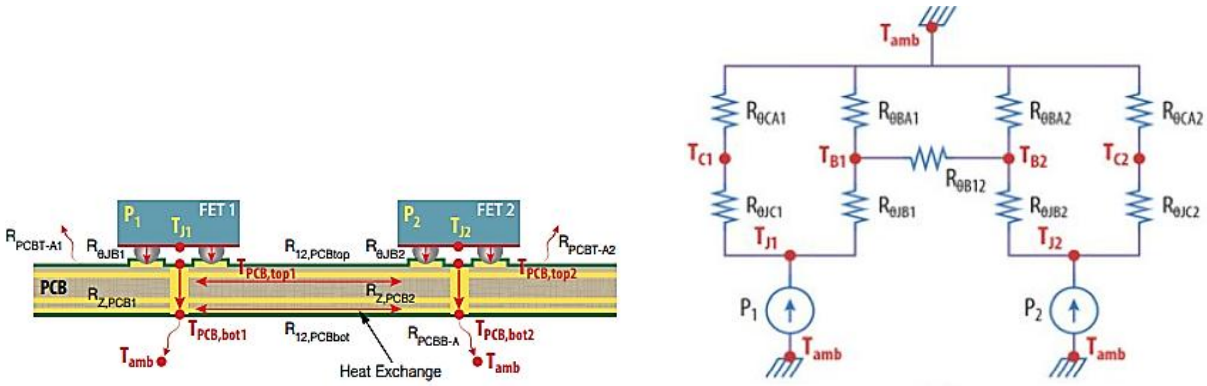


Fig. 12 - Cross-section view of GaN devices mounted on a PCB in a half-bridge configuration

Solution –



(a) (b)

Fig. 13 – (a) Heat transfer path in PCB with Half-Bridge Configuration, (b) Equivalent thermal network for half-bridge configuration PCB.

The PCB shown above is a half-bridge configuration PCB provided with two chip packages. The heat generated at the junction will travel upward directly to the ambient environment. whereas in the downward direction, it first travels through the vias and PCB board before entering the ambient. The resistances encountered in the heat transfer process are shown in the equivalent thermal network, and the solution of this network will ultimately help in the reduction of overall thermal resistance.

Ques 13. – Figure 14 shows a chip packaging provided with a heat sink, indicating the heat flow path. Using the heat flow direction, develop a thermal resistance network to determine the overall resistance encountered in the heat transfer process.

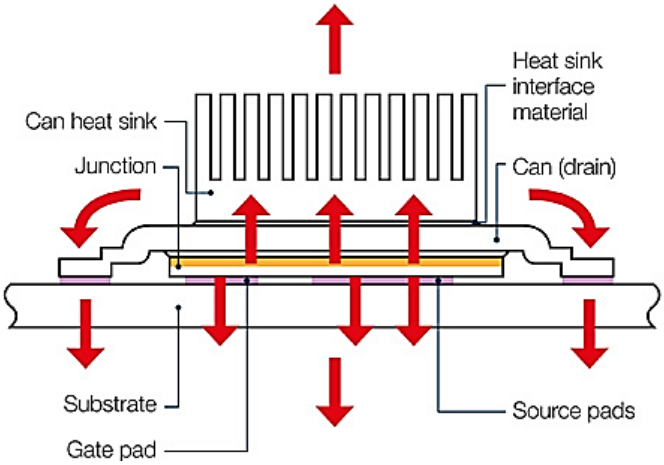


Fig. 14 – Cross-sectional View of Chip package provided with a heat sink.

Solution –

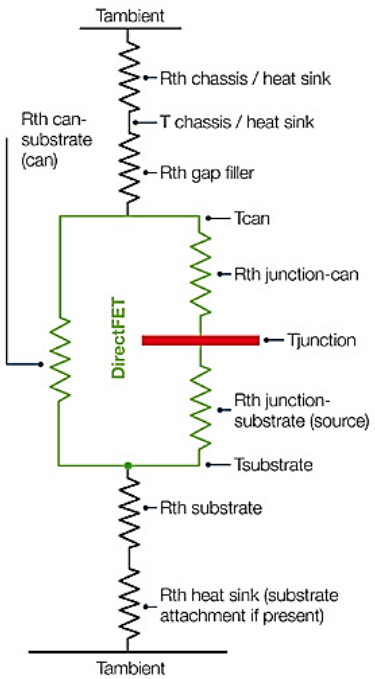
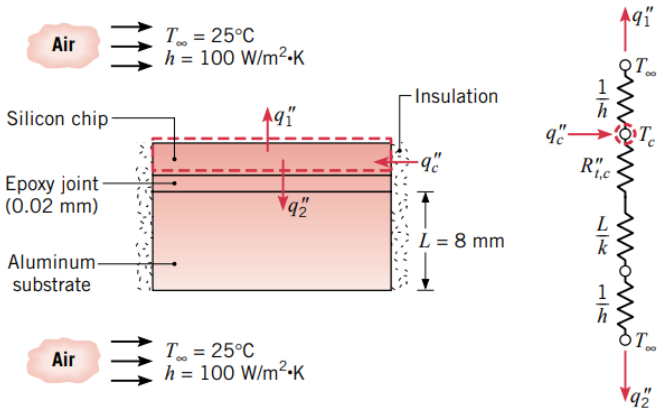


Fig. 15 – Thermal resistance network of a chip package with heat sink

As shown in Fig. 14, the heat generated at the chip junction moves parallelly in upward and downward directions. In the upward direction, heat will move through the can, heat sink interface material, and heat sink before entering the ambient. Similarly, heat moving downward will pass through the substrate, etc., and move towards the ambient. After considering all the resistances, an equivalent thermal resistance network is developed for this package, which is shown in Fig 15.

Ques 14. - A thin silicon chip and an 8-mm-thick aluminium substrate are separated by a 0.02-mm thick epoxy joint. The chip and substrate are each 10 mm on a side, and their exposed surfaces are cooled by air, which is at a temperature of 25°C and provides a convection coefficient of 100 W/m2 K. If the chip dissipates 104 W/m2 under normal conditions, will it operate below a maximum allowable temperature of 85°C?



Solution - Heat dissipated in the chip is transferred to the air directly from the exposed surface and indirectly through the joint and substrate. Performing an energy balance on a control surface about the chip, it follows that, on the basis of a unit surface area

$$q_c'' = q_1'' + q_2''$$

$$q_c'' = \frac{T_c - T_\infty}{(1/h)} + \frac{T_c - T_\infty}{R_{t,c}'' + (L/k) + (1/h)}$$

To conservatively estimate Tc, the maximum possible value of $R_{t,c}^{"} = 0.9\ 104\ m^2$K/W is used

$$T_c = T_\infty + q_c''\left[h + \frac{1}{R_{t,c}'' + (L/k) + (1/h)}\right]^{-1}$$

$$T_c = 25°C + 10^4\ W/m^2 \times \left[100 + \frac{1}{(0.9 + 0.33 + 100) \times 10^{-4}}\right]^{-1} m^2 \cdot K/W$$

$$T_c = 25°C + 50.3°C = 75.3°C$$

Hence the chip will operate below its maximum allowable temperature.

Ques 15. - A chip is dissipating 0.6 W of power in a DIP with 12 pin leads. The materials and the dimensions of various sections of this electronic device are as given in the table below. If the temperature of the leads is 40°C, estimate the temperature at the junction of the chip.

Section and Material	Thermal Conductivity, W/m · °C	Thickness, mm	Heat Transfer Surface Area
Junction constriction	-	-	diameter 0.4 mm
Silicon chip	120	0.4	3 mm x 3 mm
Eutectic bond	296	0.03	3 mm x 3 mm
Copper Lead frame	386	0.25	3 mm x3 mm
Plastic separator	1	0.25	12 x 1mm x 0.25mm
Copper leads	386	5	12 x 1mm x 0.25mm

Solution - The dimensions and power dissipation of a chip are given. The junction temperature of the chip is to be determined.

Assumptions

1 Steady operating conditions exist.

2 Heat transfer through various components is one-dimensional.

3 Heat transfer through the air gap and the lid on top of the chip is negligible because of the very large thermal resistance involved along this path.

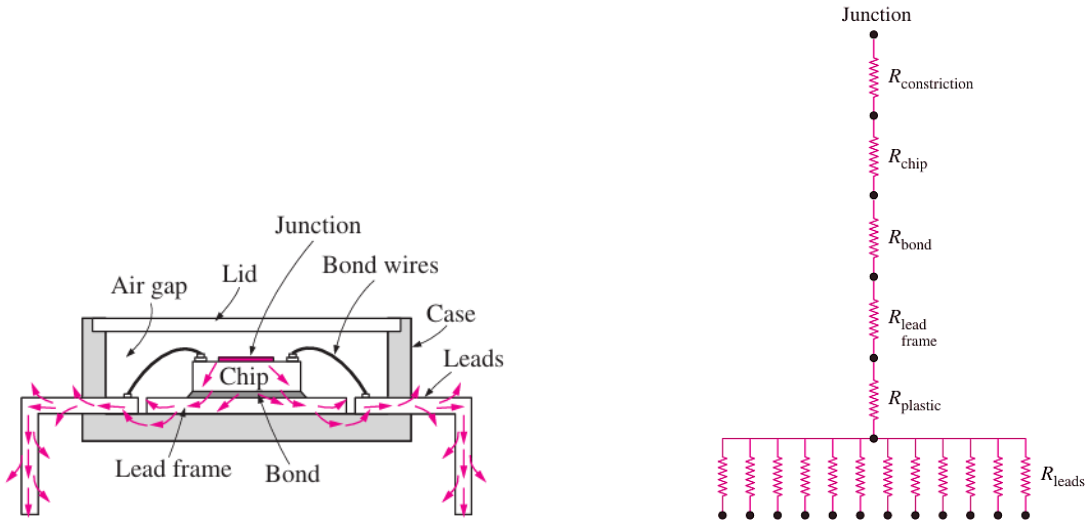


Fig. 16 - Heat generated at the junction of an electronic device flows through the path of least resistance, and its equivalent thermal circuit

The geometry of the device is as shown in Figure 14. We take the primary heat flow path to be the chip, the eutectic bond, the lead frame, the plastic insulator, and the 12 leads. When the constriction resistance between the junction and the chip is considered, the thermal resistance network for this problem becomes as shown in Figure 14. The various thermal resistances on the path of primary heat flow are determined as follows.

$$R_{\text{constriction}} = \frac{1}{2\sqrt{\pi}dk} = \frac{1}{\sqrt{\pi}(0.4 \times 10^{-3}\ \text{m})(120\ \text{W/m}\cdot\ ^\circ\text{C})} = 5.88^\circ\text{C/W}$$

$$R_{\text{chip}} = \left(\frac{L}{kA}\right)_{\text{chip}} = \frac{0.4 \times 10^{-3}\ \text{m}}{(120\ \text{W/m}\cdot\ ^\circ\text{C})(9 \times 10^{-6}\ \text{m}^2)} = 0.37^\circ\text{C/W}$$

$$R_{\text{bond}} = \left(\frac{L}{KA}\right)_{\text{bond}} = \frac{0.03 \times 10^{-3}\ \text{m}}{(296\ \text{W/m}\cdot\ ^\circ\text{C})(9 \times 10^{-6}\ \text{m}^2)} = 0.01^\circ\text{C/W}$$

$$R_{\text{lead frame}} = \left(\frac{L}{kA}\right)_{\text{lead frame}} = \frac{0.25 \times 10^{-3}\ \text{m}}{(386\ \text{W/m}\cdot\ ^\circ\text{C})(9 \times 10^{-6}\ \text{m}^2)} = 0.07^\circ\text{C/W}$$

$$R_{\text{plastic}} = \left(\frac{L}{kA}\right)_{\text{plastic}} = \frac{0.2 \times 10^{-3}\ \text{m}}{(1\ \text{W/m}\cdot\ ^\circ\text{C})(12 \times 0.25 \times 10^{-6}\ \text{m}^2)} = 66.67^\circ\text{C/W}$$

$$R_{\text{leads}} = \left(\frac{L}{kA}\right)_{\text{leads}} = \frac{5 \times 10^{-3}\ \text{m}}{(386\ \text{W/m}\cdot\ ^\circ\text{C})(12 \times 0.25 \times 10^{-6}\ \text{m}^2)} = 4.32^\circ\text{C/W}$$

Note that for heat transfer purposes, all 12 leads can be considered as a single lead whose cross-sectional area is 12 times as large. The alternative is to find the resistance of a single lead and to calculate the equivalent resistance for 12 such resistances connected in parallel. Both approaches give the same result. All the resistances determined here are in series. Thus, the total thermal resistance between the junction and the leads is determined by simply adding them up:

$$\begin{aligned} R_{\text{total}} &= R_{\text{junction-lead}} = R_{\text{constriction}} + R_{\text{chip}} + R_{\text{bond}} + R_{\text{lead frame}} + R_{\text{plastic}} + R_{\text{leads}} \\ &= (5.88 + 0.37 + 0.01 + 0.07 + 66.67 + 4.32)^\circ\text{C/W} \\ &= 77.32^\circ\text{C/W} \end{aligned}$$

Heat transfer through the chip can be expressed as

$$\dot{Q} = \left(\frac{\Delta T}{R}\right)_{\text{junction-leads}} = \frac{T_{\text{junction}} - T_{\text{leads}}}{R_{\text{junction-leads}}}$$

Solving for T_i and substituting the given values, the junction temperature is determined to be

$$T_{\text{junction}} = T_{\text{leads}} + \dot{Q}R_{\text{junction-leads}} = 40^\circ\text{C} + (0.6\ \text{W})(77.32^\circ\text{C/W}) = \mathbf{86.4^\circ C}$$