New Curriculum for M.Tech. in Integrated Electronic Circuits (IEC)

Overall credit structure

Category	PC	PE	OC	Total
Credits	24	18	6	48

Semester wise distribution of credits

Semester	Courses				Lecture Courses	Contact hours/week				Credits
						L	T	P	Total	
I	(PC) ELL732 *Micro/Nanoelectronics* **(3-0-0)**	(PC) ELL735 *Analog Circuits* **(3-0-0)**	(PC) ELL734 *MOS VLSI* **(3-0-0)**	(PC) ELP831 *IEC Lab I* **(0-0-6)**	3	9	0	6	15	12
II	PE **(3-0-0)**	(PC) ELP832 *IEC Lab II* **(0-0-6)**	(PC) ELL730 *IC Technology* **(3-0-0)**	PE / OE **(3-0-0)**	3	9	0	6	15	12
SUMMER MAJOR PROJECT/INTERNSHIP REGISTRATION MANDATORY										
III	(PC) ELD831 *Major Project Part 1* **(0-0-12)**		PE / OE **(3-0-0)**	PE / OE **(3-0-0)**		3	6	0	12	18	12
IV (Project based)	(PE) ELD832 *Major Project Part 2* **(0-0-24)**					0	0	0	24	24	12
IV (Course based)	PE / OE **(3-0-0)**	PE / OE **(3-0-0)**	PE / OE **(3-0-0)**	PE / OE **(3-0-0)**		4	12	0	0	12	12

Programme Core (PC)

Course Number	Title	L-T-P	Credit
ELD831	Major Project Part-I (Integrated Electronic Circuits)	0-0-12	6
ELL732	Micro/Nanoelectronics	3-0-0	3
ELL734	MOS VLSI	3-0-0	3
ELL735	Analog Integrated Circuits	3-0-0	3
ELL730	IC Technology	3-0-0	3
ELP831	IEC Laboratory-I	0-0-6	3
ELP832	IEC Laboratory-II	0-0-6	3

Programme Electives (PE)

Stream: VLSI Design

Course Number	Title	L-T-P	Credit
ELD830	Minor Project	0-0-6	3
ELD832	Major Project Part-II	0-0-24	12
ELL731	Mixed Signal Circuit Design	3-0-0	3
ELL733	Digital ASIC Design	3-0-2	4
ELL736	Solid State Imaging Sensors	3-0-0	3
ELL737	Flexible Electronics	3-0-0	3
ELL740	Compact Modeling of Semiconductor Devices	3-0-0	3
ELL741	Neuromorphic Engineering	3-0-0	3
ELL747	Active and Passive Filter Design	3-0-0	3
ELL748	System-on-Chip Design and Test	3-0-0	3
ELL749	Semiconductor Memory Design	3-0-0	3
ELL830	Issues in Deep Submicron VLSI Design	3-0-0	3
ELL831	CAD for VLSI, MEMS, and Nanoassembly	3-0-0	3
ELL832	Selected Topics in IEC-I	3-0-0	3
ELL833	CMOS RF IC Design	3-0-0	3
ELL834	Selected Topics in IEC-II	3-0-0	3
ELL720	Digital Signal Processing-I	3-0-0	3
ELL 782	Computer Architecture	3-0-0	3
ELL797	Neural Systems and Learning Machines	3-0-2	4
CSL719	Synthesis of Digital Systems	3-0-0	3
ELP830	Semiconductor Processing Laboratory	0-0-6	3
ELV734	Special Module in Scientific Writing for Research	1-0-0	1
ELV830	Special Module in Low Power IC Design	1-0-0	1
ELV831	Special Module in VLSI Testing	1-0-0	1
ELV832	Special Module in Machine Learning	1-0-0	1

Stream: Nanoelectronics and Photonics

Course Number	Title	L-T-P	Credit
ELD830	Minor Project	0-0-6	3
ELD832	Major Project Part-II	0-0-24	12
ELL737	Flexible Electronics	3-0-0	3
ELL738	Micro and Nano Photonics	3-0-0	3
ELL739	Advanced Semiconductor Devices	3-0-0	3
ELL740	Compact Modeling of Semiconductor Devices	3-0-0	3
ELL741	Neuromorphic Engineering	3-0-0	3
ELL742	Introduction to MEMS Design	3-0-0	3
ELL743	Photovoltaics	3-0-0	3
ELL744	Electronic and Photonic Nanomaterials	3-0-0	3
ELL745	Quantum Electronics	3-0-0	3
ELL746	Biomedical Electronics	3-0-0	3
ELL749	Semiconductor Memory Design	3-0-0	3
ELL797	Neural Systems and Learning Machines	3-0-2	4
ELL830	Issues in Deep Submicron VLSI Design	3-0-0	3
ELL832	Selected Topics in IEC-I	3-0-0	3
ELL834	Selected Topics in IEC-II	3-0-0	3
ELP830	Semiconductor Processing Laboratory	0-0-6	3

ELP833	Device and Materials Characterization Laboratory	0-0-6	3
ELV734	Special Module in Scientific Writing for Research	1-0-0	1
ELV833	Special Module in Semiconductor Business Management	1-0-0	1
ELV834	Special Module in Nanoelectronics	1-0-0	1

Stream: Embedded Intelligent Systems

Course Number	Title	L-T-P	Credit
ELD830	Minor Project	0-0-6	3
ELD832	Major Project Part-II	0-0-24	12
ELL731	Mixed Signal Circuit Design	3-0-0	3
ELL733	Digital ASIC Design	3-0-2	4
ELL736	Solid State Imaging Sensors	3-0-0	3
ELL748	System-on-Chip Design and Test	3-0-0	3
ELL830	Issues in Deep Submicron VLSI Design	3-0-0	3
ELL831	CAD for VLSI, MEMS, and Nanoassembly	3-0-0	3
ELL832	Selected Topics in IEC-I	3-0-0	3
ELL834	Selected Topics in IEC-II	3-0-0	3
ELL720	Digital Signal Processing-I	3-0-0	3
ELL782	Computer Architecture	3-0-0	3
ELL784	Introduction to Machine Learning	3-0-0	3
ELL787	Embedded Systems and Applications	3-0-0	3
ELL789	Intelligent Systems	3-0-0	3
ELL797	Neural Systems and Learning Machines	3-0-2	4
ELL883	Embedded Intelligence	3-0-0	3
CSL719	Synthesis of Digital Systems	3-0-0	3
CSL788	Embedded Computing	3-0-0	3
ELV734	Special Module in Scientific Writing for Research	1-0-0	1
ELV831	Special Module in VLSI Testing	1-0-0	1
ELV832	Special Module in Machine Learning	1-0-0	1

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	IC Technology
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL730
6.	**Status** (*category* for *program*)	PG

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem -

11.	**Faculty who will teach the course** Dr. Anuj Dhawan, Dr. Manan Suri, Dr. Jagadesh Kumar, Dr. Madhusudan Singh, Dr. Bhaskar Mitra

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** This course will introduce the student to the world of semiconductor IC technology fabrication. Emphasis will be laid on covering the basics of all key process-flow steps in advanced CMOS fabrication. The course will also provide a comprehensive flavor of advanced device fabrication techniques, trade-offs and key considerations/constraints in developing a device/circuit process flow.

14.	**Course contents (about 100 words) (Include laboratory/design activities):**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Course Introduction, Modern Semiconductor IC fabrication Industrial/Academic Landscape	2
2	Overview of modern CMOS process flow – basic steps	3
3	Crystal growth and wafer basics	3
4	Cleanroom basics – environment, infrastructure, advanced MOS cleaning, getering etc	1.5
4	Lithography	3
5	Oxidation	3
6	Diffusion	3
7	Ion-Implantation	3
8	Thin-Film Deposition	4.5
9	Etching	3
10	Backend processes	2
11	Process Simulation- tools, techniques and methods	3
12	Advanced device fabrication concepts – I (SOI, FDSOI, etc)	2.5
13	Advanced device fabrication concepts – II (organic, PV, hetero)	2.5
14	Advanced device fabrication concepts – III (CNTs, Self-assembly etc)	3
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Plummer, Deal, Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, 1,Prentice Hall, 2000.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Matlab, Silvaco TCAD, TSUPREME
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	Mixed signal circuits
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL731
6.	**Status** (*category* for *program*)	PE for EEN, Stream core for JVL, and DE for EE1

7.	**Pre-requisites** (course no./title)	ELL782

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	None

10.	**Frequency of offering**	☐Every sem ☐1st sem ☒ 2nd sem ☐Either sem

11.	**Faculty who will teach the course** G, S. Visweswaran, Shouri Chatterjee, Basabi Bhaumik, Mukul Sarkar	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** To familiarize students with data converters, switched capacitor circuits, phase locked loops.

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** **Switched capacitor circuit principles and applications in filter design; issues of clock feedthrough, charge injection and other non-idealities; design of switches; data converters: characteristics, static and dynamic; types of ADCs; track and hold, and sample and hold circuits; comparators; flash ADCs; pipelined ADCs; successive approximation register type ADCs; discrete-time and continuous time delta-sigma ADCs; higher order delta-sigma design; MASH structure; multi-bit delta-sigmas; decimation filtering – sinc and comb filters; digital to analog conversion; voltage-based DACs; charge-based DACs; current-based DACs – binary and thermometer currents; linearizing techniques for DACs; delta-sigma DACs; interpolation filtering; phase-locked loop basics; PLL dynamics; frequency synthesis; all-digital PLLs.**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Switched capacitor circuits	4
2	Data conversion characteristics	2
3	Sample and holds, comparators	3
4	Flash ADCs	2
5	Pipelined ADCs	4
6	SAR and slope ADCs	3
7	Sigma delta ADCs	9
8	Decimation filters	2
9	Voltage and charge based DACs	3
10	Current steering DACs, DAC linearization	2
11	Sigma delta DACs, interpolation filtering	3
12	PLL basics, APLL, ADPLL	3
13	Frequency synthesis	2
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - The students will be given design assignments to be carried out from concept to post layout simulation.

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. David A. Johns, Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.
2. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Inter-Science, 2003.
3. R. Gregorian, G. C. Temes, "Analog MOS Integrated Circuits for Signal Processing", John Wiley and Sons, 1986.
4. P.E. Allen, Doug Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2011.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	**Software**	Cadence spectre, ngspice
19.2	**Hardware**	Computers
19.3	**Teaching aides (videos, etc.)**	NIL
19.4	**Laboratory**	NA
19.5	**Equipment**	NIL
19.6	**Classroom infrastructure**	A classroom with a projector and large black/white board.
19.7	**Site visits**	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	**Design-type problems**	10%
20.2	**Open-ended problems**	10%
20.3	**Project-type activity**	20%
20.4	**Open-ended laboratory work**	N/A
20.5	**Others (please specify)**	None

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**Micro/Nanoelectronics**
3.	**L-T-P structure**	**3-0-0**
4.	**Credits**	**3**
5.	**Course number**	**ELL732**
6.	**Status** (*category* for *program*)	M.Tech

7.	**Pre-requisites** (course no./title)	None

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐1stsem

11.	**Faculty who will teach the course: M. Jagadesh Kumar, Madhusudan Singh, Anuj Dhawan, Manan Suri**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** To familiarize the students with the modeling and the physical concepts behind the operation of microelectronic and nanoelectronic devices and enhance your appreciation for the field of high performance, high speed semiconductor devices used in VLSI systems.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** This course will help the students think about the design, performance and limitations of microelectronic and nanoelectronic devices including both homo-junction and hetero-junction electronic devices. Innovative new devices and their operation and modeling will be introduced.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Semiconductor fundamentals: Carrier transport phenomena, Recombination and generation	5 Lectures
2	Physics & models related to PN junctions: Schottky junctions, Ohmic contacts	5 Lectures
3	MOSFET Design and Modeling: MOS Capacitance fundamentals, interface and frequency effects, MOSFET Operation and modeling, Short and narrow channel effects, Radiation and hot-carrier effects, Breakdown, LDD, NBTI, CMOS latch-up, CMOS Device design considerations & performance factors, Brief overview of MOSFET CAD SPICE models- different levels and BSIM series.	10 Lectures
4	Bipolar Junction transistors: Bipolar device Design and Modeling, Small and large signal models, Non-ideal effects, breakdown voltage, charge storage, Multidimensional effects, Bipolar Device optimization & performance factors for digital and analog circuits, Brief overview of BJT CAD SPICE model and VBIC model introduction.	10 Lectures
5	Modern VLSI Devices: Poly silicon emitter transistors, Heterojunctions, 2D electron gas, band alignment, SiGe HBTs, SOI MOSFETs, Floating body effect, Source/drain engineering, Brief introduction to HEMTs, MESFETs and MODFETs. Steep subthreshold transistors – TFETs, IMOS etc.,	10 Lectures
6	Current topics in Nanoelectronics: Nanowire Electronics, challenges and future trends.	2 Lectures
COURSE TOTAL *(14 times 'L')*		**42 lectures**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours
	Home work	
	Quizzes	
	Research report	
	Seminar	

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

- Donald A. Neaman, *Semiconductor Physics and Devices,* Tata McGraw-Hill, 2014
- J.Singh, *Semiconductor Devices-Basic Principles*, Wiley, 2014
- Taur and Ning, *Fundamentals of Modern VLSI Devices*, Cambridge Press, 2014
- Muller and Kamins, *Device electronics for Integrated circuits*, Wiley, 2014.
    - Journals such as *IEEE Transactions on Electron Devices, IEEE Electron Device Letters* and *Solid-state Electronics*

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	50 %
21.2	Open-ended problems	20 %
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/~~Centre~~ proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	Digital ASIC Design
3.	**L-T-P structure**	3-0-2
4.	**Credits**	5
5.	**Course number**	ELL733
6.	**Status** (*category* for *program*)	B.Tech. Dept. Elective

7.	**Pre-requisites** (course no./title)	EEL308

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	CSL316
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem - **3rd Yr, 1st Sem**.

11.	**Faculty who will teach the course**	Dr. Shouri Chatterjee, Dr. Turbo Majumder, Prof G.S. Visweswaran, Prof. Basabi Bhaumik, Dr. Anuj Dhawan, and Prof. Jayadeva.
12.	**Will the course require any visiting faculty?**	No

13.	**Course objectives** *(about 50 words)***:** To equip students with understanding of advanced digital systems design: finite state machine design and optimization, hardware description languages, synthesis of data and control paths, technology considerations and design for testability.

14.	**Course contents (about 100 words) (Include laboratory/design activities):**
	Technology basics and digital logic families such as static CMOS, pass transistor, transmission gate, dynamic and domino logic. Advanced sequential logic elements with latch-based design and timing and clocking concepts. Power and delay of digital circuits. Physical and logical synthesis for ASICs and FPGAs. Verilog and VHDL with design examples. Design for testability with fault models.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction: Technology basics, static CMOS, transistor characteristics refresher	4
2	Digital logic families: Ratio-ed logic, pass-transistor, transmission gate, dynamic logic, domino logic	4
3	Advanced sequential logic elements; latch-based design; timing concepts	3
4	Advanced FSM theory; clocking concepts	5
5	Power and delay of digital circuits	4
6	ASIC; FPGA; Design flow; Logical synthesis; Physical synthesis	8
7	VHDL with design examples	2
8	Datapath and control path design with Verilog	5
9	DFT: Testability, fault models, scan, JTAG, BIST, MISR	7
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities: **Tutorials are embedded in the Lectures.**

17. Brief description of laboratory activities

1	Introduction to RTL based design using Verilog (Icarus)	2 X 4
2	Circuit design using different logic families using ngspice	2 X 4

3	Synopsys based design flow	2 X 4
4	Xilinx FPGA programming	4 X 4
5	Design project	4 X 4
	Total	14 X 4

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. FPGA-BASED System Design by Wayne Wolf, Prentice Hall, 2004, ISBN 0-13-142461-0
2. Analysis and Design of Digital Integrated Circuits by Hodges, Jackson and Saleh, Third Edition, McGraw hill, ISBN 0-07-228365-3
3. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V. D. Agrawal, Boston: Springer, 2005, ISBN 0-7923-7991-8

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	Synopsys DC, Cadence Spectre, CMOS 65 nm standard libraries, Ngspice, Icarus
19.2	Hardware	Workstations
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	II-401
19.5	Equipment	FPGA kits
19.6	Classroom infrastructure	Projector
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	60%
20.2	Open-ended problems	
20.3	Project-type activity	40%
20.4	Open-ended laboratory work	30%
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/~~Centre~~ proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	MOS VLSI
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL734
6.	**Status** (*category* for *program*)	M.Tech. Programme core for IEC and VDTT

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	EEL329 (80%), EEL324(20%)
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem - **1st Sem**.

11.	**Faculty who will teach the course** Prof. Basabi Bhaumik, Prof G.S. Visweswaran, Prof. Jayadeva, Dr. Turbo Majumder and Dr. Shouri Chatterjee.	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objectives** *(about 50 words)***:** To equip students with understanding of MOS VLSI design, Optimizing power dissipation and delay in a design, Timimg issues in synchronous design, Effect of parasitics on circuit performance.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Digtal integrated circuit design pespective. Basic static and dynamic MOS logic families. Sequential Circuits. Power dissipation and delay in circuits. Arithmetic Building blocks, ALU. Timimg Issues in syncronous design. Interconnect Parasitics.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Issues in Digital Integrated Circuit Design, MOS Transistor basics –Static and Dynamic Behavior, Secondary effects.	4 hours
2	CMOS Inverter Static and Dynamic Behavior, Noise Margin, Power Consumption and Power Delay Product, Latch up, Technology Scaling.	7 hours
3	Logic gates- Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: basic principles, performance of dynamic logic, Noise consideration, Power consumption in CMOS gates – switching activity, Glitches.	10 hours
4	Sequential Circuits: Bistability, CMOS static flip-flop, Pseudostatic latch, Dynamic two-phase flip-flop, C^2MOS latch, NORA (no race)-CMOS logic design style, Schmitt Trigger, Astable and monostable circuits.	8 hours
5	Arithmetic Building blocks: Adder, Multiplier and Shifters. ALU	5 hours
6	Timimg Issues in syncronous design.	4 hours
7	Interconnect Parasitics: Resistance, Capacitance and Inductance.	4 hours
8		
9		
COURSE TOTAL *(14 times 'L')*		42

16.	**Brief description of tutorial activities: Tutorials are embedded in the Lectures.**	
	Not applicable	

17. Brief description of laboratory activities

1	Not applicable	
2		
3		
4		
5		

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Digital Integrated Circuits: A Design Perspective by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson Education, 2003. ISBN 81-7808-991-2
2. CMOS VLSI Design : A Circuit and System Perspective by Neil H.E. Weste, David harris and Ayan Banerjee, Pearson Education, 2005. ISBN 0321149017/9780321149015

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**EE**
2.	**Course Title** *(< 45 characters)*	**Analog Integrated Circuits**
3.	**L-T-P structure**	**3-0-0**
4.	**Credits**	**3**
5.	**Course number**	**ELL735**
6.	**Status** (*category* for *program*)	PC

7.	**Pre-requisites** (course no./title)	EEL 204

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NIL
8.2	Overlap with any UG/PG course of other Dept./Centre	NIL
8.3	Supersedes any existing course	NIL

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1stsem ☒2ndsem ☐Either sem -

11.	**Faculty who will teach the course** **Prof. G.S. Visweswaran, Prof. M Jagadesh Kumar, Dr. Shouribrata Chaterjee, Dr. Mukul Sarkar**

12.	**Will the course require any visiting faculty? (yes/no)**	NO

13.	**Course objectives** *(about 50 words)*: To give a comprehensive overview of single stage, multistage, differential and operational amplifiers.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Introduction to MOSFETs, Single stage amplifiers, Biasing circuits, Voltage and Current reference circuits, Feedback analysis, Multistage amplifiers, Mismatch and noise analysis, Differential amplifiers, High speed and low noise amplifiers, Output stage amplifiers, Oscillators.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction to MOSFETs	3
2	Single stage amplifiers	7
3	Cascode and multistage amplifiers	5
4	Biasing circuits and feedback	8
5	Noise and mismatch analysis	3
6	High frequency response	3
7	Differential amplifiers	6
8	High speed, low noise differential amp. and constant Gm circuits	5
9	Oscillators	2
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours
1	MOSFET Theory, operation, small signal analysis	4
2	Single stage amplifiers	4
3	High frequency behavior	4
4	Feedback and biasing	3
5	Multistage, differential amplifiers	6
6	VCO, Power amplifiers	6

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

B. Razavi, Design of Analog Integrated Circuits, McGraw Hill Education, 2000.

Gray, Hurst, Lewis, Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.

P. E. Allen, D. R. Holberg, CMOS Analog Circuit Design, 3rd Edition, Oxford University Press, 2013.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	NIL

20.2	Hardware	NIL
20.3	Teaching aides (videos, etc.)	NIL
20.4	Laboratory	NIL
20.5	Equipment	NIL
20.6	Classroom infrastructure	LCD, Blackboard
20.7	Site visits	NIL
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	50%
21.2	Open-ended problems	30%
21.3	Project-type activity	20%
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: 12/02/2015 (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Department of Electrical Engineering
2.	**Course Title** *(< 45 characters)*	SOLID STATE IMAGING SENSORS
3.	**L-T-P structure**	*3-0-0*
4.	**Credits**	**3**
5.	**Course number**	**ELL736**
6.	**Status** (*category* for *program*)	Open Elective

7.	**Pre-requisites** (course no./title)	EEL204/EEL782

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NO
8.2	Overlap with any UG/PG course of other Dept./Centre	NO
8.3	Supersedes any existing course	NO

9.	**Not allowed for** (indicate program names)	Electronics Basics is required

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** 1. Dr. Mukul Sarkar 2. Dr. Shouribrata Chaterjee 3. Prof. Visweswaran

12.	**Will the course require any visiting faculty? (yes/no)**	NO

13.	**Course objectives** *(about 50 words)*:
	Understanding the electronics behind the cameras and the images.

14.	**Course contents (about 100 words) (Include laboratory/design activities):**
	Radiometry and Photometry (Light radiation, photometry, light source, light units), Introduction to properties of silicon and photon absorption, Imager formats, Basics of image sensors (fundamental definition of image sensors, pixels, photo-conversion principles, Charge coupled devices (operational principles, types and performance metrics), CMOS image sensors (operational principles, types and performance metrics), Noise, quantum efficiency, dynamic range and modulation transfer function analysis in image sensors, High speed image sensors, Back side illumination, Electron multiplication CCDs and CMOS, Colour detection in silicon, 3D imaging, machine vision cameras, polarization detection and scientific applications.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Radiometry and Photometry	2
2	Properties of Silicon and Photon absorption	3
3	Basics of image sensors	4
4	Charge coupled devices	5
5	CMOS image sensors	5
6	Noise in image sensors	3
7	Image sensor characterization	4
8	High speed low noise imagers	3
9	Back side illumination/EM-CCD and EM-CMOS	4
10	Colour detection in silicon	3
11	3D imaging	3
12	Polarization detection and machine vision	3
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours
	No tutorials proposed	

17. Brief description of laboratory activities

Module no.	Description	No. of hours
	Not applicable - No Lab activities proposed	

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours
1	Basic of analog circuit design	10
2	Basic device structures	10

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

Albert J.P. Theuwissen, *Solid State Imaging with Charged Couple Devices* , Dordrecht, Kluwer Academic Publishers, 1995.

Jun Ohta , *Smart CMOS Image sensors and Applications*, CRC press, 2007.

O. Yadid Pecht and R. E. Cummings, *CMOS imagers: From Photo transduction to Image processing*, Springer, 2004.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	NIL
20.2	Hardware	NIL
20.3	Teaching aides (videos, etc.)	NIL
20.4	Laboratory	NIL
20.5	Equipment	NIL

20.6	Classroom infrastructure	Projector, Black board
20.7	Site visits	NIL
20.8	Others (please specify)	NIL

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	Yes, 10-15% of the student time
21.2	Open-ended problems	NO
21.3	Project-type activity	Yes, Writing review paper on the current trends in technology related to imaging, approx. 20% of the student time
21.4	Open-ended laboratory work	NO
21.5	Others (please specify)	NIL

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	Flexible Electronics
3.	**L-T-P structure**	**(3-0-0)**
4.	**Credits**	**3**
5.	**Course number**	**ELL737**
6.	**Status** (*category* for *program*)	Program Elective

7.	**Pre-requisites** (course no./title)	EEL218/ELL111 (UG) or EEL732 (PG) or equivalent

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Madhusudan Singh, Anuj Dhawan**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** Recent advances in flexible electronics have revolutionized traditional technologies in lighting and display technology, energy generation systems like solar cells, infrastructural and biological sensors, and intelligent control systems. This has paralleled ongoing improvements in materials compatible with flexible substrates and low-temperature processing methods like printing methods and roll to roll methods that permit their use.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Introduction to displays and lighting technologies, solar cells, and sensors. Flexible substrates. Low cost materials. Solution-processed fabrication methods. Printing methods. Flexible displays. Flat panel lighting. Flexible solar cells. Low-cost sensors.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction: display and lighting technology	4
2	Introduction: solar cells	4
3	Introduction: sensors	4
4	Flexible substrates and low cost materials	4
5	Solution-processed materials and fabrication methods	7
6	Printing methods	5
7	Flexible displays technologies	4
8	Flat panel lighting technologies	3
9	Flexible solar cells	4
10	Low cost sensors	3
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. W. Wong, A. Salleo. Flexible Electronics: Materials and Applications. Springer. 2009.
2. I. Hutchings, G. D. Martin. Inkjet Technology for Digital Fabrication. Wiley. 2012.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Electronic projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	Micro- and Nano- Photonics
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL738
6.	**Status** (*category* for *program*)	Nano Electronics and Photonics stream (PG Course, Open to UG students)

7.	**Pre-requisites** (course no./title)	PHL100, EEL207 (or any equivalent course on engineering electromagnetics)

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	PHL795 (Less than 20% overlap)
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐ Every sem ☐ 1st sem ☐ 2nd sem ☒ Either sem

11.	**Faculty who will teach the course** Dr. Anuj Dhawan	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** The motivation for the course is to make the students understands the fundamentals of photonics with focus on micro-photonic and nano-photonic devices and physics.

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Ray Optics; Wave Optics: Plane Waves, Spherical Waves, Interference, Diffraction; Paraxial Waves; Beam Optics; Fabry Perot Cavity; Microresonators - Ring Resonators, Disc Resonators; Review of Electromagnetic (EM) Theory; Boundary Conditions; and some relevant EM problems; FDTD and FEM modeling; Fundamentals of Plasmonics - Surface Plasmon Resonance, Dispersion relation, Plasmon coupling conditions, Plasmonic gratings, Models describing the refractive index of metals; Localized Surface Plasmon Resonance; Plasmonic Sensors and Devices; Surface-enhanced Raman Scattering; Plasmonic Waveguides and Interconnects; Photonic Crystals and Devices

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Ray Optics; Wave Optics (Plane Waves, Spherical Waves, Interference, Diffraction)	5
2	Paraxial Waves; Beam Optics	3
3	Fabry Perot Cavity	2
4	Microresonators - Ring Resonator and Disc Resonator Devices	6
5	Review of Electromagnetic (EM) Theory, Boundary Conditions, Some relevant EM problems, FDTD and FEM modeling	4
6	Fundamentals of Plasmonics - Surface Plasmon Resonance, Dispersion relation, Coupling Conditions, Plasmonic Gratings, Models describing the refractive index of metals	5
7	Localized Surface Plasmon Resonance	3
8	Plasmonic Sensors and Devices	4
9	Surface-enhanced Raman Scattering	2
10	Plasmonic Waveguides and Interconnects	5
11	Photonic Crystals and Devices	3
11		
12		
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - None

Suggested texts and reference materials

18. STYLE: Author name and initials, Title, Edition, Publisher, Year.

B. E. A. Saleh and M. C. Teich, Fundamentals of Photonics, Second Edition, Wiley, 2007
S. Maier, Plasmonics - Fundamentals and Applications, First Edition, Springer, 2007
L. Novotny and B. Hecht, Principles of Nano-optics, Second Edition, Cambridge University Press, 2012

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	FDTD Software (Lumerical), FEM Software (COMSOL)
19.2	Hardware	NIL
19.3	Teaching aides (videos, etc.)	NIL
19.4	Laboratory	NA
19.5	Equipment	NIL
19.6	Classroom infrastructure	A big classroom with a projector and large black board.
19.7	Site visits	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	10%
20.3	Project-type activity	10%
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	**Advanced Semiconductor Devices**
3.	**L-T-P structure**	**(3-0-0)**
4.	**Credits**	**3**
5.	**Course number**	**ELL739**
6.	**Status** (*category* for *program*)	Program Elective

7.	**Pre-requisites** (course no./title)	EEL218/ELL111 (UG) or EEL732 (PG)

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☒2ndsem ☐Either sem -

11.	**Faculty who will teach the course** **Madhusudan Singh, Manan Suri, Anuj Dhawan, Bhaskar Mitra, Mukul Sarkar**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** The course will equip students with an understanding of devices like LEDs, lasers, light detectors, photovoltaics, memory devices, sensors and MEMS which are essential to an understanding of contemporary technology.

14.	**Course contents (about 100 words) (Include laboratory/design activities): Solid state device physics, generation and recombination processes, radiation basics, density of states, gain and absorption, LEDs, OLEDs, heterojunction LEDs, lasers, population inversion, photodetectors, CCDs, image sensors, photocurrent, solar cells, efficiency measures, multijunction PVs, organic solar cells, economics, memory devices, sensors, MEMS devices**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction: solid state device physics, generation and recombination processes	3
2	Radiation basics	2
3	Density of states, gain and absorption	3
4	LEDs, OLEDs, heterojunction LEDs	5
5	Lasers and population inversion	5
6	Photodetectors, CCDs	4
7	Solar cells and power conversion efficiency	5
8	Thin film fabrication processes and materials	2
9	Multijunction PVs and organic solar cells, economics of PVs	4
10	Memory devices	6
11	Sensors and MEMS devices	3
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Jasprit Singh, Physics of Semiconductors and their Heterostructures. 1st, McGraw-Hill, 1993.
2. Pallab Bhattacharya, Semiconductor Optoelectronic Devices, 2nd Ed, Prentice-Hall, 1996.
3. Peter Wurfel, Physics of Solar Cells – From Basic Principles to Advanced Concepts, 1st, Wiley, 2009.
4. Silicon Non-Volatile Memories: Paths of Innovation, Wiley-ISTE, 2009

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Electronic projector

20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/~~Centre~~ proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	Compact Modeling of Semiconductor Devices
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL740
6.	**Status** (*category* for *program*)	B.Tech. /M.Tech. Dept. Elective

7.	**Pre-requisites** (course no./title)	Any one course on MOS devices or Microelectronics or Physical Electronics or VLSI Technology

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem - **M. Tech. 2nd Yr, B. Tech. and D.D. 4th Yr**

11.	**Faculty who will teach the course** Dr. Abhisek Dixit, Prof. M. Jagadesh Kumar	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objectives** *(about 50 words)***:** To equip students with understanding of silicon foundry, process design kit (PDK) and its components, role of compact models in PDK, compact models for front end of line passives and MOSFETs, VT and surface potential based MOSFET core dc models, compact modeling methodologies for layout and statistical effects, including corners, mismatch and process variations, MOSFET p-cell based RF modeling.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Introduction to AMS enablement and PDK elements, Basics of semiconductor devices, Device modeling tools- TCAD and SPICE, Diode modeling, Resistor modeling, FEOL capacitor modeling, Advanced CMOS Technology, MOS transistor modeling, modeling of process variations, Mismatch and corners

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction to AMS enablement and PDK elements	2
2	Basics of semiconductor devices	2
3	Device modeling tools- TCAD and SPICE	2
4	Diode modeling	4
5	Resistor modeling	4
6	FEOL capacitor modeling	4
7	Advanced CMOS Technology	6
8	MOS transistor modeling	12
9	Modeling of process variations, mismatch, corners	6
COURSE TOTAL *(14 times 'L')*		42

16.	**Brief description of tutorial activities: Tutorials are embedded in the Lectures.**	

17. Brief description of laboratory activities

1		

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Compact Modeling: Principles, Techniques and Applications by Gennady Gildenblat, ISBN 978-90-481-8613-6, Springer 2010.
2. MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4 by William Liu, ISBN 0-471-39697-4, John Wiley & Sons, 2001.
3. The MOS Transistor, 3rd Edition by Yannis Tsividis, ISBN 978-0-19-809737-2, Oxford University Press, 2012.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	Cadence Spectre, Agilent ICCAP, Example PDK
19.2	Hardware	Workstations
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	VDTT
19.5	Equipment	None
19.6	Classroom infrastructure	Projector
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	10%
20.2	Open-ended problems	
20.3	Project-type activity	20%
20.4	Open-ended laboratory work	5%
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	Neuromorphic Engineering
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL741
6.	**Status** (*category* for *program*)	PG

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☒Every sem ☐1stsem ☐2ndsem ☐Either sem -

11.	**Faculty who will teach the course** Dr. Manan Suri, Dr. Sumeet Aggarwal, and Dr. Jayadeva

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** To introduce students to the area of Neuromorphic Engineering, implementations and Bio-Inspired Computing Systems. Provide essentials on key hardware building blocks, system design and practical real-world applications of Neuromorphic Systems.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** This course offers an introduction to the highly inter-disciplinary and rapidly growing area of Neuromorphic Computing. A Neuromorphic engineer requires knowledge of several domains – namely electrical engineering, nano-electronics, elementary computational neuroscience, basic biology and neural networks. The course will cover all fundamentals applicable to the field as well as some advanced case studies to understand the full system design approach starting from individual nano-devices to final applications.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Motivation and field Introduction, Emerging computing trends and roadmap, non-von Neumann computing approach	3
2	Basic Biology – 1: Neuron, Synapse, Synaptic Plasticity	3
3	Basic Biology -2 : Learning rules, Retina, Cochlea, STDP	3
4	Mathematical/Electrical modeling of Neurons - LIF, IF, HH	3
5	Hardware Implementation of Neuron circuits – VLSI Digital/Analog	3
6	Advanced Nanodevices for Neuron Implementation	3
7	Hardware Implementation of Synaptic and Learning circuits – VLSI Digital/Analog	3
8	Advanced Nanodevices for Synaptic emulation – 1 (NVM, Flash etc)	3
9	Advanced Nanodevices for Synaptic emulation – 2 (RRAM, memristors, CNT etc)	3
10	Synaptic programming methodology optimization	3
11	Nanodevice specific bio-inspired learning rule optimization	3
12	Full Network design example -1: Visual Application	3
13	Full Network design example -2: Auditory Application	3
14	Full system level power/energy dissipation considerations and course conclusion	3
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours
	Extensive scientific journal/conference paper reading/bibliography	
	End semester term paper	
	End semester presentation	
	Design assignment	
	Group wise discussions	

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Shih-Chii Liu, Analog VLSI: Circuits and Principles, The MIT Press, 2002
2. Robert Kozma, Advances in Neuromorphic Memristor Science, Vol 4, Springer, 2012
3. Manan Suri "Emerging Resistive Memory Technology for Neuromorphic Systems and Applications", Thesis Archive – CEA-LETI, France, 2013
4. Several IEEE and other relevant research journal/conference papers
5. Course Lecture Handouts

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Matlab, Python, C
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	20% Home work problems
21.2	Open-ended problems	20% Extended homework requiring simulation
21.3	Project-type activity	25% - Students do a term paper or design project
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	**Introduction to MEMS Design**
3.	**L-T-P structure**	**(3-0-0)**
4.	**Credits**	**3**
5.	**Course number**	**ELL742**
6.	**Status** (*category* for *program*)	PG Elective, Stream Elective for UG

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	CRL726 (RF MEMS)
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐ 2ndsem ☒ Either sem -

11.	**Faculty who will teach the course** **Bhaskar Mitra, Madhusudan Singh, Anuj Dhawan**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** To introduce students to the area of MEMS and Microsystems, provide essential information for them to be able to design simple microsensors and systems.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** This course is an introduction to the multi-disciplinary and rapidly growing area of MEMS. A MEMS design engineer requires knowledge of several domains –namely mechanical, electrical, fluidic and thermal, as well as knowledge of circuits and microfabrication techniques. This course will cover the fundamentals as applicable to MEMS, as well as several case studies to understand the design process.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Motivation and examples, benefits of scaling, transduction process	1
2	Lithography and Etching and Wafer Bonding for MEMS	2
3	Diffusion, Oxidation and Film Deposition	2
4	Bulk Micromachining process and examples	1.5
5	Sacrifical films and release, surface micromaching MUMPS	1.5
6	Mechanics of Materials, design of flexures, Energy methods	9
7	Equivalent Circuit modelling of mechanical elements	2
8	Electrostatic Actuation and capacitive sensing	4
9	Piezoresistive sensing	1
10	Piezoelectric actuation and sensing	3
11	Mechanical Resonance for MEMS	3
12	RF MEMS Devices – Oscillators, Filters, Switches, Capacitors, Inductors	5
13	Inertial MEMS Devices – Accelerometers, Gyroscopes, Pressure Sensors	5
14	Introduction to Microfluidics	2
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Chang Liu, Foundations of MEMS, 2nd Edition, Pearson/Prentice Hall, 2010
2. Stephen D. Senturia, Microsystem Design, 2nd Ed. Kluwer Academic Publishers, 2000
3. Gregory T.A. Kovacs, Micromachined Transducers Sourcebook, McGraw Hill, 1998

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Comsol, MATLAB, Mathematica
20.2	Hardware	Workstations
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	20% - Home work problems
21.2	Open-ended problems	20% - Extended homework requiring simulation
21.3	Project-type activity	25% - Term Paper or Design Project
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	**Photovoltaics**
3.	**L-T-P structure**	**(3-0-0)**
4.	**Credits**	**3**
5.	**Course number**	**EEL743**
6.	**Status** (*category* for *program*)	Departmental Elective

7.	**Pre-requisites** (course no./title)	EEL218/ELL111 (UG) or EEL732 (PG) or equivalent

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	EEL739 (25%)
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Madhusudan Singh, Abhisek Dixit**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** The course will equip students with an understanding of the solid state device physics and p-n junction operation in solar cells. Different solar cell architectures and materials (c-Si, a-Si:H, multijunction III-Vs, chalcogenides, organic, DSSCs) will be covered. Related topics like light management, solar panel economics and policy issues will also be discussed.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Solid state device physics, p-n and p-i-n junctions. Homojunctions and heterojunctions. Generation and recombination processes. Radiation basics. Photon absorption. Photovoltaic efficiency. Thin film fabrication processes. Silicon-based solar cells. III-V and chalcogenide-based solar cells. Multijunction architectures. Dye-sensitized solar cells. Organic solar cells. Plasmonic structures. Solar cell economics and policy.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction: solid state devices physics, p-n junctions	4
2	p-i-n structures, homojunctions and heterojunction devices.	4
3	Radiation basics, generation and recombination processes. Efficiency limits.	6
4	Thin-film fabrication processes.	8
5	PV materials.	2
6	Silicon-based solar cells. Light trapping schemes.	5
7	III-V materials and chalcogenides. Multijunction devices.	3
8	Dye-sensitized solar cells	3
9	Organic solar cells and plasmonic structures.	4
10	Solar cell economics and policy	3
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Peter Wurfel, Physics of Solar Cells – From Basic Principles to Advanced Concepts, 1st, Wiley, 2009.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Electronic projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	Electronic and Photonic Nanomaterials
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL744
6.	**Status** (*category* for *program*)	Nano Electronics and Photonics stream (PG Course, Open to UG students)

7.	**Pre-requisites** (course no./title)	PHL100 (or any equivalent course)

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	EPL444, (Less than 25% overlap) PHL726 (Less than 25% overlap)
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐ Every sem ☐ 1st sem ☐ 2nd sem ☒ Either sem

11.	**Faculty who will teach the course** Dr. Anuj Dhawan, Prof. Jagadesh Kumar	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** The motivation for the course is to make the students understands the physics of electronic and optical nanomaterials, the electronic and optical properties of nanomaterials, as well as the development and characterization of nanomaterials

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** 1D, 2D and 3D confinement; Density of states; Excitons; Coulomb blockade; Optical properties of semiconducting nanoparticles: Fluorescence of semiconductor nanocrystals, core-shell nanocrystals, effect of nanocrystal size; Optical properties of metallic nanoparticles: Surface Plasmons, Localized Surface Plasmons, Surface-enhanced Raman scattering; Electronic Applications of Nanomaterials: Nanowire transistors, Memory Devices, Single electron devices, Biosensors; Optical Applications of Nanomaterials - Quantum well, wire, and dot Diodes, Lasers and Detectors, Chemical sensors, Gas sensors, Biosensors; Development of Electronic and Optical Nanomaterials: Epitaxial Growth, Deposition of Nanomaterials, Self-Assembly of Nanomaterials, Nanofabrication techniques; Characterization of Nanomaterials: Electron microscopic techniques (scanning and transmission), Atomic Force Microscopy, X-Ray Diffraction, Characterization of optical and electronic properties of nanomaterials

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	1D, 2D and 3D confinement; Density of states; Excitons; Coulomb blockade	10
2	Optical properties of semiconducting nanoparticles: Fluorescence of semiconductor nanocrystals, Core-shell nanocrystals, Effect of nanocrystal geometry	5
3	Optical properties of metallic nanoparticles: Surface Plasmons, Localized Surface Plasmons, Surface-enhanced Raman scattering	5
4	Electronic Applications of Nanomaterials - Single electron devices, Nanowire transistors, Memory Devices, Biosensors	4
5	Optical Applications of Nanomaterials - Quantum well, wire, and dot Diodes, Lasers and Detectors, Chemical sensors, Gas sensors, Biosensors	4
6	Development of Electronic and Optical Nanomaterials: Epitaxial Growth, Nanomaterial Deposition Techniques, Self-Assembly of Nanomaterials, Nanofabrication techniques	8
7	Characterization of Nanomaterials: Electron microscopic techniques (Scanning and Transmission), Atomic Force Microscopy, X-Ray Diffraction, Characterization of optical and electronic properties of nanomaterials	6
8		
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - None

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

G. Cao, Nanostructures and Nanomaterials, Second Edition, Imperial College Press, 2011.

D. Feng and G. Jin, Introduction to Condensed Matter Physics, First Edition, World Scientific Publishing Co., 2005. Chap 14.

T. Tsusumi, H. Hirayama, M. Vacha, T. Taniyama, Nanoscale Physics for Materials Science, First Edition, CRC Press, 2010.

L. Novotny and B. Hecht, Principles of Nano-optics, Second Edition, Cambridge University Press, 2012.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	NIL
19.2	Hardware	NIL
19.3	Teaching aides (videos, etc.)	NIL
19.4	Laboratory	NA
19.5	Equipment	NIL
19.6	Classroom infrastructure	A big classroom with a projector and large black board.
19.7	Site visits	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	10%
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	**Quantum Electronics**
3.	**L-T-P structure**	**(3-0-0)**
4.	**Credits**	**3**
5.	**Course number**	**EEL745**
6.	**Status** (*category* for *program*)	Departmental Elective

7.	**Pre-requisites** (course no./title)	EEL218/ELL111 (UG) or EEL732 (PG) or equivalent

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	PHL727 PHL793
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Madhusudan Singh, M. Jagadesh Kumar, Anuj Dhawan, Uday Khankhoje**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** Provide students a detailed understanding of the role of quantum physical processes in design and operation of modern semiconductor devices.

14.	**Course contents (about 100 words) (Include laboratory/design activities): Newtonian mechanics, wavepackets, brief history of quantum mechanics, blackbody radiation, photoelectric effect, wave-particle duality, second quantization, Semiconductor materials, crystal structure and defects, Bravais lattices, Brillouin zones, Miller indices, periodic potentials, Kronig-Penney model, bandstructure in bulk semiconductors, Bloch theorem, direct and indirect bandgap semiconductors, effective mass, effect of alloying, carrier statistics, superlattices and quantum wells, density of states in 0,1,2 and 3 dimensions, bandstructure in lower dimensional systems, heterojunctions, effect of strain on bandstructure, excitonic effects in semiconductors, tunneling, perturbation theory, scattering and collisions, phonons, high-field transport, Boltzmann transport theory, spin transport, excitons, optical processes in semiconductors and quantum wells, absorption, gain, spontaneous and stimulated emission, fluorescence and phosphorescence, photophysics of organic molecules and polymers.**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Newtonian mechanics, wavepackets, brief history of quantum mechanics, blackbody radiation, photoelectric effect, wave-particle duality, second quantization.	4
2	Semiconductor materials, crystal structure and defects, Bravais lattices, Brillouin zones, Miller indices, periodic potentials, Kronig-Penney model, bandstructure in bulk semiconductors, Bloch theorem, direct and indirect bandgap semiconductors, effective mass, effect of alloying, carrier statistics.	8
3	Superlattices and quantum wells, density of states in 0,1,2 and 3 dimensions, bandstructure in lower dimensional systems, heterojunctions, effect of strain on bandstructure, excitonic effects in semiconductors.	7
4	Tunneling, perturbation theory, scattering and collisions, phonons, high-field transport, Boltzmann transport theory, spin transport.	8
5	Excitons, optical processes in semiconductors and quantum wells, absorption, gain, spontaneous and stimulated emission.	9
6	Fluorescence and phosphorescence, photophysics of organic molecules and polymers.	6
COURSE TOTAL *(14 times 'L')*		**42**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Jasprit Singh, Physics of Semiconductors and their Heterostructures. 1st, McGraw-Hill, 1993.
2. Neil W. Ashcroft and N. David Mermin, Solid State Physics, 1st, Cengage Learning, 1976.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Electronic projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/~~Centre~~ proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	Biomedical Electronics
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL746
6.	**Status** (*category* for *program*)	UG specialisation elective / PG elective

7.	**Pre-requisites** (course no./title)	EEL201

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem - **3rd Yr, 1st Sem**.

11.	**Faculty who will teach the course** Dr. Rehman, Dr. Anuj Dhawan	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objectives** *(about 50 words)***:** To equip students with the basic ideas involved in biomedical instrumentation, electronic and optical biosensors, bioimaging, and different kinds of biomedical devices

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Introduction to Biomedical Instrumentation: Constraints, Regulations and health economics, Basic sensors, amplifiers and signal processing, Origin of bio potentials and electrode systems, Bio potential amplifiers, sources of noise and their Remedies, Blood pressure and heart sound systems, Measurement of flow and volume of blood Measurement of respiratory system, Ultrasonography, CAT, PET and MRI overview, Fuzzy Logic and its application medical instruments, Embedded system in medical electronics with selection of one microprocessor and then design tips, Overview of pace maker, defibrllator, hemodialysis and infant incubators. Safety codes and standards, Electro-chemical sensor, Ion Selective FET, Immunologically sensitive FET, Spectrophotometry, Optical biosensors, Fibre-optic sensors, blood glucose sensor, smell sensor, SAW devices, Sensor neural network, Expert systems and case studies of design examples.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction to Biomedical Instrumentation: Constraints, Regulations and health economics	2
2	Basic sensors, amplifiers and signal processing	2.5
3	Origin of bio potentials and electrode systems	2
4	Bio potential amplifiers, sources of noise and their remedies	2.5
5	Blood pressure and heart sound systems	2
6	Measurement of flow and volume of blood	2
7	Measurement of respiratory system	2
8	Ultrasonography, CAT, PET and MRI overview	2
9	Fuzzy Logic and its application medical instruments	2
10	Embedded system in medical electronics with selection of one microprocessor and then design tips	4
11	overview of pace maker, defibrllator, hemodialysis and infant incubators. Safety codes and standards	2
12	Electro-chemical sensor, Ion Selective FET, Immunologically sensitive FET	3
13	Spectrophotometry, Optical biosensors, Fibre-optic sensors	6
14	Blood glucose sensor, Smell sensors, SAW devices	3
15	Sensor neural network	1.5
16	Expert systems and case studies of design examples	1.5
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities: Tutorials are embedded in the Lectures.

17. Brief description of laboratory activities None

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Ed. Tuan Vo-Dinh, Biomedical Photonic Handbook, 2nd Edition, CRC Press, 2015
2. John G. Webster, Medical Instrumentation: Application and Design, 4th Edition, John Wiley and Sons, 2009
3. B. E. A. Saleh and M. C. Teich, Fundamentals of Photonics, Second Edition, Wiley, 2007
4. R. Khandpur, Handbook of Biomedical Instrumentation, Second Edition, Tata McGraw Hill, 2012
5. Research papers

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	
19.5	Equipment	

19.6	Classroom infrastructure	Projector
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	15%
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	Active and passive filter design
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL747
6.	**Status** (*category* for *program*)	PE for EEN, JVL, and DE for EE1, EE3

7.	**Pre-requisites** (course no./title)	ELL112 / Circuit Theory for EE1, EE3

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	None

10.	**Frequency of offering**	☐Every sem ☐1st sem ☒ 2nd sem ☐Either sem

11.	**Faculty who will teach the course** Shouri Chatterjee, Mukul Sarkar, G.S. Visweswaran, R.K. Patney	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** Enable students to design analog filters using passive and active components. Studying approximation theory, classical filter design, and active filters, will allow them to design any custom filter that an application may require.

14.	**Course contents: Review of network theorems such as reciprocity, Tellegen's theorem, scattering parameters, properties of lossless passive networks; Butterworth approximation; Chebyshev approximation; synthesis of Butterworth and Chebyshev filters; odd versus even order filters; sensitivity of lossless LC ladder filters; frequency transformations; inverse Chebyshev and elliptic approximations; synthesis of inverse Chebyshev and elliptic filters; review of properties of p.r. functions; Darlington synthesis; signal flow graphs of ladder filters; opamp-RC implementation; Gm-C implementation; switched-capacitor implementation; minimum required performance of active components; tuning of filters; transmission line based filters: using high-Z low-Z technique, using Kuroda's identities; bi-quad based design approaches and drawbacks; Tow-Thomas biquad, Sallen-Key biquad.**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Review of network theorems, scattering parameters	4
2	Butterworth approximation and synthesis	3
3	Frequency transformations	2
4	Chebyshev approximation and synthesis	3
5	Even order filters	2
6	Inverse Chebyshev approximation and Brune synthesis	4
7	Review of p.r. Functions, and Darlington synthesis	5
8	Elliptic approximation	5
9	Signal flow graph and opamp-RC implementation	3
10	Gm-C, switched-capacitor implementations	2
11	Tuning of filters	2

12	Transmission line based filters: high-Z, low-Z; Kuroda's identities	5
13	Biquad based designs	2
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - The students will be given design assignments to be carried out from concept to design.

18. Suggested texts and reference materials

1. Mac E. Van Valkenburg, "Analog Filter Design", Oxford Univesity Press, USA, 2001.
2. Y.P. Tsividis, J.O. Voorman, "Integrated Continuous-Time Filters: Principles, Design, and Applications", IEEE, 1993.
3. Herbert J. Carlin, "Wideband Circuit Design", CRC Press, 1997.
4. Omar Wing, "Classical Circuit Theory", Springer, 2009.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	**Software**	Cadence spectre, ngspice
19.2	**Hardware**	Computers
19.3	**Teaching aides (videos, etc.)**	NIL
19.4	**Laboratory**	NA
19.5	**Equipment**	NIL
19.6	**Classroom infrastructure**	A classroom with a projector and large blackboard.
19.7	**Site visits**	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	**Design-type problems**	40%
20.2	**Open-ended problems**	20%
20.3	**Project-type activity**	40%

20.4	**Open-ended laboratory work**	N/A
20.5	**Others (please specify)**	None

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/~~Centre~~ proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	System-on-Chip Design and Test
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL748
6.	**Status** (*category* for *program*)	UG specialisation elective / PG elective

7.	**Pre-requisites** (course no./title)	EEL201

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem - **3rd Yr, 1st Sem**.

11.	**Faculty who will teach the course** Dr. Turbo Majumder, Dr. Shouri Chatterjee, Prof G.S. Visweswaran, Prof. Basabi Bhaumik and Prof. Jayadeva.	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objectives** *(about 50 words)***:** To equip students with the basic ideas involved in system-on-chip, platform-based design, interconnects, low-power systems-on-chip and digital testing of systems-on-chip.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Design trends in deep submicron (DSM) era, including scaling trend, clock cycle and power issues; Role of interconnects in contemporary SoC Design – delay in long wires and performance limitations, interconnect coupling capacitance and its effect on wire delay, crosstalk avoidance coding schemes (CAC), fault modelling in presence of crosstalk, interconnect inductance; System-on-chip and Platform-based design – IP-based design and reusability, Multiprocessor SoC platform design, 3D integration, on-chip optical and wireless communication, Design for testability (DFT), Test Access Mechanism (TAM), concept of core-based test & IEEE P1500 standard for SoC test; Importance of Power and Low power SoC design methodology – physics of power dissipation in CMOS, design and test of low-voltage CMOS circuits, Multiple Threshold CMOS (MTCMOS), Variable Threshold CMOS and other related methodologies for leakage power reduction, coding for low power, power minimisation through architecture level optimisation.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Overview of system-on-chip	3
2	Physical design issues, capacitance, inductance	5
3	Global interconnects, clock, power grid	5
4	SoC testing, JTAG, P1500	5
5	Fault model, test pattern generation and detection	4
6	IDDQ test, parametric test, yield	6
7	Power consumption and low power design (circuit, physical, interconnect, memory)	7
8	Dynamic power management	4
9	Low power test	3
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities: Tutorials are embedded in the Lectures.

17. Brief description of laboratory activities

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Analysis and Design of Digital Integrated Circuits - In Deep Submicron Technology, Hodges, Jackson and Saleh, McGraw-Hill, Third Edition, 2004.
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, M. L. Bushnell and V. D. Agrawal, Boston: Springer, 2005.
3. Research papers

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	Synopsys DC, Cadence Spectre, CMOS 65 nm standard libraries, Ngspice, Icarus
19.2	Hardware	Workstations
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	II-401, VDTT
19.5	Equipment	
19.6	Classroom infrastructure	Projector
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	60%
20.2	Open-ended problems	
20.3	Project-type activity	40%

20.4	Open-ended laboratory work	30%
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	Semiconductor Memory Design
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL749
6.	**Status** (*category* for *program*)	PE for M.Tech in IEC (PG Course, Open to UG students) and OE for others

7.	**Pre-requisites** (course no./title)	MOS VLSI

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	None

10.	**Frequency of offering**	☐Every sem ☐1st sem ☒2nd sem ☐Either sem

11.	**Faculty who will teach the course** G, S. Visweswaran, Mannan Suri, Shouri Chatterjee	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** The motivation for the course is to make the students understands the fundamentals of Semiconductor memory and Memory Design.

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Memory hierarchy in digital systems; Static RAM: Types, Overall architecture, SRAM Cell - Design, Layout, Noise Issues and Margins and Assembly of Core, Peripheral Circuitry - Decoding, Array conditioning for read/write, Sensing, Writing, Synchronization; Dynamic RAM: Types, Cell design, Assembly of core, Core architectures, Peripheral circuitry - Sensing, Elevated voltage supplies; Modern high speed DRAM - EDO, SDR, DDR; Non Volatile Memories: ROM - Array Design, EPROM - Cell and Array Design, EEPROM - Tunneling Phenomena, EEPROM Cell both Hot Carrier based operation and Tunneling based Operation; Flash Memories: Cell operation and design, Types of modern high density flash memories - NOR Flash, NAND Flash.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Memory hierarchy in digital systems	2
2	Static RAM Cell including Design, Layout, Noise Issues and Margins and assemble of Cores	6
3	SRAM Peripheral Circuit including Decoding, Array conditioning for Read/Write, Sensing, Writing and Synchronization	6
4	Dynamic RAM Types, Cell Design and Core Architecture	4
5	DRAM Peripheral Circuits including Sensing and High Voltage Supply	5
6	Modern High Speed DRAM: EDO, SDR and DDR	2
7	ROM: Array Design	2
8	EPROM: Cell and Array Design	3
9	EEPROM: Tunneling Phenomena	2
10	EEPROM Cell: Hot Carrier and Tunneling based operations	5
11	Flash Memories: Cell Operation and Design3	3
11	Types of Modern High Density Flash Memories: NOR and NAND Flash	2
12		
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - The students will be given design assignments to be carried out from concept to post layout simulation.

Suggested texts and reference materials

18. STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Betty Prince, "Semiconductor Memories: A Handbook of Design, Manufacture and Application", 2nd Edition-, John Wiley, ISBN: 978-0-471-94295-5.
2. Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs – Evolution and Function", Johm Wiley, ISBN: 978-0-471-98610-2.
3. Kiyoo Itoh, Masashi Horiguchi and Hitoshi Tanak, "Ultra-Low Voltage Nano-Scale Memories"' Springer Internationa Edition, ISBN: 13 978-0-387-33398-4.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	**Software**	CADENCE/MENTOR/SYNOPSYS Tool
19.2	**Hardware**	Computers
19.3	**Teaching aides (videos, etc.)**	NIL
19.4	**Laboratory**	NA
19.5	**Equipment**	NIL
19.6	**Classroom infrastructure**	A classroom with a projector and large black/white board.
19.7	**Site visits**	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	**Design-type problems**	10%
20.2	**Open-ended problems**	10%
20.3	**Project-type activity**	20%
20.4	**Open-ended laboratory work**	N/A
20.5	**Others (please specify)**	None

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICA ENGINEERING
2.	**Course Title** *(< 45 characters)*	Issues in Deep Submicron VLSI Design
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL830
6.	**Status** (*category* for *program*)	PE for M.Tech in IEC and VDTT

7.	**Pre-requisites** (course no./title)	EEL 734

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	None

10.	**Frequency of offering**	☐Every sem ☒1st sem ☐ 2nd sem ☐Either sem

11.	**Faculty who will teach the course** G, S. Visweswaran, Shouri Chatterjee, Mukul Sarkar

12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** The motivation for the course is to make the students understands the fundamentals of Semiconductor memory and Memory Design.

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** VLSI Scaling rules and their impact: Short channel effect, Sub threshold leakage current, Gate leakage, V_{TH} and body bias; Low power design:: Technology level: 3D and 4 terminal MOSFETs, PDSOI, FDSOI, FINFET; Sub threshold leakage control: Transistor stacking in digital logic Multiple V_{TH}, V_{DD} designs, Dynamically adjustable V_{TH}; Digital Circuit Design: Digital Sub-threshold Logic, Noise Immunity, Clock gating, Switching activity minimization; Analog Circuit Design: g_m/I_D Methodology for Design, Low power, low voltage opamp design, Subthreshold operation of opamps; Architecture level: Array Based Architectures, Parallel and Pipelined Architectures; Interconnects & Noise: Capacitive & Inductive coupling Analysis & Optimization, Power/Ground Noise, L*di/dt noise, Power/Ground Placement Optimization, Decoupling

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	VLSI Scaling rules and their impact: Short channel effect, Sub threshold leakage current, Gate leakage, V_{TH} and body bias	4
	Low power design:	
2	Technology level: 3D and 4 terminal MOSFETs, PDSOI, FDSOI, FINFET	6
3	Sub threshold leakage control: Transistor stacking in digital logic Multiple V_{TH}, V_{DD} designs, Dynamically adjustable V_{TH}	6
4	Digital Circuit Design: Digital Sub-threshold Logic, Noise Immunity, Clock gating, Switching activity minimization.	6
5	Analog Circuit Design: g_m/I_D Methodology for Design, Low power, low voltage opamp design, Subthreshold operation of opamps.	6
6	Architecture level: Array Based Architectures, Parallel and Pipelined Architectures	6
7	Interconnects & Noise: Capacitive & Inductive coupling Analysis & Optimization, Power/Ground Noise, L*di/dt noise, Power/Ground Placement Optimization, Decoupling	8
COURSE TOTAL		42

16. Brief description of tutorial activities - None

17. Brief description of Design activities - The students will be given design assignments to be carried out from concept to post layout simulation.

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Design of High-Performance Microprocessor Circuits, edited by A. Chandrakasan, W. Bowhill, F. Fox, Wiley Blackwee, 2000.
2. Flip-Flop Design in Nanometer CMOS: From High Speed to Low Energy By Massimo Alioto, Springer, 2015.
3. The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches, Paul Jespers, Springer 2010.
4. Power Aware Design Methodologies, Pedram M., Rabaey J (eds), Kluwer academic publisher, 2002.
5. Low Power Design Essentials, Jan Rabaey, Springer, 1st edition, 2009.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	**Software**	CADENCE/MENTOR/SYNOPSYS Tool
19.2	**Hardware**	Computers
19.3	**Teaching aides (videos, etc.)**	NIL
19.4	**Laboratory**	VLSI Design Laboratory for Design Activities
19.5	**Equipment**	NIL
19.6	**Classroom infrastructure**	A classroom with a projector and large black/white board.
19.7	**Site visits**	NA

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	**Design-type problems**	10%
20.2	**Open-ended problems**	10%
20.3	**Project-type activity**	30%
20.4	**Open-ended laboratory work**	N/A
20.5	**Others (please specify)**	None

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	EE
2.	**Course Title** *(< 45 characters)*	CAD for VLSI, MEMS, and Nanoassembly
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL831
6.	**Status** (*category* for *program*)	PG Elective

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	
8.3	Supercedes any existing course	No

9.	**Not allowed for** (indicate program names)	
10.	**Frequency of offering**	☐ Every sem ☐ 1st sem ☐ 2nd sem ☒ Either sem
11.	**Faculty who will teach the course** Prof. Jayadeva, Prof. Basabi Bhaumik	
12.	**Will the course require any visiting faculty?**	No
13.	**Course objective** *(about 50 words)*: To acquaint students with computer aided design for VLSI, MEMS, and nanoassembly; how to design, model, and simulate large scale systems	

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Algorithms for design, modelling, and simulation ranging from VLSI, MEMS, to nanoassembly; computer aided nano-design for materials

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Algorithms and complexity	6
2	Upper, lower and exact bounds	3
3	Algorithms for bottom up and top down design in VLSI, MEMS	8
4	Self organization at the nanoscale; computer aided nano-engineering	10
5	Modelling and Simulation for VLSI, MEMS, and the nanoscale	6
6	Optimization methods for systems design	6
7	Current Trends and Future Directions	3
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities - None

17. Brief description of laboratory activities - None

18. Suggested texts and reference material

1. VLSI Physical Design Automation: Theory and Practice, S. M. Sait & H. Youssef, World Scientific, 1999.
2. Combinatorial Algorithms for Integrated Circuit Layout, T. Lengauer, John Wiley & Sons, 1990.
3. An Introduction to VLSI Physical Design, M. Sarrafzadeh & C. K. Wong, McGraw Hill, 1996.

4. Senturia, Stephen D. Microsystem Design. New York, NY: Springer, 2004.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	
19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	10%
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**Semiconductor Processing Laboratory**
3.	**L-T-P structure**	**0-0-6**
4.	**Credits**	**3**
5.	**Course number**	**ELP830**
6.	**Status** (*category* for *program*)	Elective for M.Tech. IEC and VDTT

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Dr. Anuj Dhawan, Dr. M. Suri, Prof. M. Jagadesh Kumar, Dr. Bhaskar Mitra, Dr. Madhusudan Singh**

12.	**Will the course require any visiting faculty? (yes/no)**	no

13.	**Course objectives** *(about 50 words)***:** In response to national policy on ESDM, our country is gearing up to answer the global challenge of high-end manufacturing. “Make in India” mission by the Hon’ble prime minister of India revolves around availability of engineering talent pool and abundance of natural resources in India. At this critical juncture, our IEC and VDTT students have

	to be readied to take up roles in the upcoming semiconductor manufacturing sector. This course it targeted to impart necessary semiconductor fabrication skills to help our graduates recognize the opportunity and stand up to the challenge.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Deposition of Semiconductor Materials and Metals: Sputter Deposition, E-Beam Deposition, and Thermal Evaporation; Photolithography; Electron-Beam Lithography; Epitaxial Growth of Semiconductors, Materials Characterization

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities: Tutorials are embedded in the Lab.

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours
1	Deposition of Semiconductor Materials and Metals: Sputter Deposition, E-Beam Deposition, and Thermal Evaporation	9
2	Photolithography	6
3	Electron-Beam Lithography	6
4	Epitaxial Growth of Semiconductors	8
5	Materials Characterization	4
6	Lab Project	9
	Total Hours	**42**

18. Description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours

19. Suggested texts and reference materials: to be provided by the instructor

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Plummer, Deal, Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, 1,Prentice Hall, 2000.
2. C. S. Solanki, Solar Photovoltaics, Second Edition, PHI, 2011
3. D. Schroder, Semiconductor Material and Device Characterization, Wiley, 2006

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Synopsys-Sentaurus, Keysight-ICCAP
20.2	Hardware	Equipment for Sputter Deposition, E-Beam Deposition, and Thermal Evaporation, Photolithography, Electron-Beam Lithography, Epitaxial Growth of Semiconductors, and Materials Characterization
20.3	Teaching aides (videos, etc.)	none
20.4	Laboratory	Nanoscale Research Facility
20.5	Equipment	Equipment for Sputter Deposition, E-Beam Deposition, and Thermal Evaporation, Photolithography, Electron-Beam Lithography, Epitaxial Growth of Semiconductors, and Materials Characterization
20.6	Classroom infrastructure	None
20.7	Site visits	none
20.8	Others (please specify)	none

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	25%
21.2	Open-ended problems	25%
21.3	Project-type activity	20%
21.4	Open-ended laboratory work	30%
21.5	Others (please specify)	0

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**IEC Laboratory-I**
3.	**L-T-P structure**	**0-0-6**
4.	**Credits**	**3**
5.	**Course number**	**ELP831**
6.	**Status** (*category* for *program*)	Core for M.Tech. IEC and VDTT

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Dr. Jayadeva, Dr. Shouri Chaterjee**

12.	**Will the course require any visiting faculty? (yes/no)**	no

13.	**Course objectives** *(about 50 words)***:** Our IEC and VDTT students have to be readied to take up roles in the upcoming VLSI design sector. This course it targeted to impart necessary practical VLSI design skills, using Cadence, Synopsys, and Xilinx tools, to our students.

14.	**Course contents (about 100 words) (Include laboratory/design activities):**
	Introduction to Cadence, Learning Cadence design framework and Virtuoso environment, Design with Virtuoso schematic editor, Layouts, Learning and applying Synopsys and Xilinx tools, Circuit simulation and SPICE

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities: Tutorials are embedded in the Lab.

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours
1	Introduction to Cadence	6
2	Learning Cadence design framework and Virtuoso environment	6
3	Design with Virtuoso schematic editor	6
4	Learning and applying Synopsys and Xilinx tools	4
5	Circuit simulation and SPICE	4
6	Lab Project	16
	Total Hours	**42**

18. Description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours

19. Suggested texts and reference materials: to be provided by the instructor

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Digital Integrated Circuits: A Design Perspective by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson Education, 2003. ISBN 81-7808-991-2
2. CMOS VLSI Design : A Circuit and System Perspective by Neil H.E. Weste, David harris and Ayan Banerjee, Pearson Education, 2005. ISBN 0321149017/9780321149015

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Synopsys, Cadence, and Xilinx Software Tools
20.2	Hardware	None
20.3	Teaching aides (videos, etc.)	none
20.4	Laboratory	IEC Laboratories
20.5	Equipment	None
20.6	Classroom infrastructure	None
20.7	Site visits	none
20.8	Others (please specify)	none

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	20%
21.2	Open-ended problems	20%
21.3	Project-type activity	40%
21.4	Open-ended laboratory work	20%
21.5	Others (please specify)	0

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**IEC Laboratory-II**
3.	**L-T-P structure**	**0-0-6**
4.	**Credits**	**3**
5.	**Course number**	**ELP832**
6.	**Status** (*category* for *program*)	Core for M.Tech. IEC and VDTT

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Dr. Jayadeva, Dr. Shouri Chaterjee**

12.	**Will the course require any visiting faculty? (yes/no)**	no

13.	**Course objectives** *(about 50 words)***:** Our IEC and VDTT students have to be readied to take up roles in the upcoming VLSI design sector. This course it targeted to impart necessary practical VLSI design skills, using Cadence, Synopsys, and Xilinx tools, to our students.

14.	**Course contents (about 100 words) (Include laboratory/design activities):**
	Introduction to Cadence, Learning Cadence design framework and Virtuoso environment, Design with Virtuoso schematic editor, Layouts, Learning and applying Synopsys and Xilinx tools, Circuit simulation and SPICE

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities: Tutorials are embedded in the Lab.

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours
1	Learning Cadence design framework and Virtuoso environment	4
2	Design with Virtuoso schematic editor	4
3	Layouts	8
4	Learning and applying Synopsys and Xilinx tools	4
5	Circuit simulation and SPICE	4
6	Lab Project	18
	Total Hours	**42**

18. Description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours

19. Suggested texts and reference materials: to be provided by the instructor

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. Digital Integrated Circuits: A Design Perspective by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson Education, 2003. ISBN 81-7808-991-2
2. CMOS VLSI Design : A Circuit and System Perspective by Neil H.E. Weste, David harris and Ayan Banerjee, Pearson Education, 2005. ISBN 0321149017/9780321149015

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Synopsys, Cadence, and Xilinx Software Tools
20.2	Hardware	None
20.3	Teaching aides (videos, etc.)	none
20.4	Laboratory	IEC Laboratories
20.5	Equipment	None
20.6	Classroom infrastructure	None
20.7	Site visits	none
20.8	Others (please specify)	none

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	20%
21.2	Open-ended problems	20%
21.3	Project-type activity	40%
21.4	Open-ended laboratory work	20%
21.5	Others (please specify)	0

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	Electrical Engineering
2.	**Course Title** *(< 45 characters)*	**Scientific Writing for Research**
3.	**L-T-P structure**	**(1-0-0)**
4.	**Credits**	**1**
5.	**Course number**	**ELV734**
6.	**Status** (*category* for *program*)	Open Elective

7.	**Pre-requisites** (course no./title)	None

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	None
8.2	Overlap with any UG/PG course of other Dept./Centre	None
8.3	Supersedes any existing course	None

9.	**Not allowed for** (indicate program names)	-

10.	**Frequency of offering**	☐Every sem ☐1stsem ☐2ndsem ☒Either sem -

11.	**Faculty who will teach the course** **Madhusudan Singh, Mukul Sarkar, G. Visweswaran, Uday Khankhoje, Turbo Majumder, Kushal Shah, Shouri Chatterjee, Sumeet Agrawal**

12.	**Will the course require any visiting faculty? (yes/no)**	No

13.	**Course objectives** *(about 50 words)***:** The course will equip students with an understanding of the process of writing a good scientific article, scientific English, work with bibliographies, and be aware of ethical considerations.

14.	**Course contents (about 100 words) (Include laboratory/design activities): Tools needed for scientific writing, ethics of publication, plagiarism, attribution, copyrights, writing impactful papers, writing theses, writing a technical disclosure or patent.**

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Introduction. Copyrights. Measures of scientific productivity.	1
2	Tools: scientific graphics, e-resources	3
3	Attribution and author identity. Typesetting, English and citation management.	3
4	Collaborative writing	1
5	Ethics and plagiarism	2
6	Impactful papers	2
7	Theses	1
8	Patents and technical disclosures	1
COURSE TOTAL *(14 times 'L')*		**14**

16. Brief description of tutorial activities:

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study

component (mandatory for 700 / 800 level courses)

As per the lecture modules, assignments, reading journal papers, and class projects are given as self-study

Module no.	Description	No. of hours

19. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

1. William Strunk Jr. and E. B. White, Elements of Style, Macmillan/Springer, 1959
2. A. M. Coghill and L. R. Garson, Eds., The ACS Style Guide, ACS, 2006
3. Edward Tufte, Visual Display of Quantitative Information, Graphics Press.
4. Best Practice Guidelines on Publication Ethics: A Publisher's Perspective, Wiley.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	
20.2	Hardware	
20.3	Teaching aides (videos, etc.)	
20.4	Laboratory	
20.5	Equipment	
20.6	Classroom infrastructure	Electronic projector
20.7	Site visits	
20.8	Others (please specify)	

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	
21.2	Open-ended problems	
21.3	Project-type activity	
21.4	Open-ended laboratory work	
21.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICAL ENGINEERING DEPARTMENT
2.	**Course Title** *(< 45 characters)*	SPECIAL MODULE IN LOW POWER IC DESIGN
3.	**L-T-P structure**	1-0-0
4.	**Credits**	1
5.	**Course number**	ELV830
6.	**Status** (*category* for *program*)	PE

7.	**Pre-requisites** (course no./title)	EEL 734, EEL 782 or EEL329

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NONE
8.2	Overlap with any UG/PG course of other Dept./Centre	NONE
8.3	Supercedes any existing course	NONE

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1st sem ☐2nd sem ☒Either sem

11.	**Faculty who will teach the course**	INVITED VISITORS FROM INDUSTRIES
12.	**Will the course require any visiting faculty?**	YES

13.	**Course objective** *(about 50 words)***:** TO INTRODUCE STUDENTS, including both UG and PG, TO CURRENT ISSUES IN LOW POWER IC DESIGN

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Special Module that focuses on special topics, development and Research problems of importance in the area of Low Power IC Design.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities

17. Brief description of laboratory activities

Module no.	Experiment description	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
COURSE TOTAL *(14 times 'P')*		

18. Suggested texts and reference materials

STYLE: Sonntag, R. E., Borgnakke, C., and Van Wylen, G. J., *Fundamentals of Thermodynamics*, 5th Ed., John Wiley, 2000.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	

19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICAL ENGINEERING DEPARTMENT
2.	**Course Title** *(< 45 characters)*	SPECIAL MODULE IN VLSI TESTING
3.	**L-T-P structure**	1-0-0
4.	**Credits**	1
5.	**Course number**	ELV831
6.	**Status** (*category* for *program*)	PE

7.	**Pre-requisites** (course no./title)	EEL 734 and EEL 782 or EEL329

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NONE
8.2	Overlap with any UG/PG course of other Dept./Centre	NONE
8.3	Supercedes any existing course	NONE

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1st sem ☐2nd sem ☒Either sem

11.	**Faculty who will teach the course**	INVITED VISITORS FROM INDUSTRIES
12.	**Will the course require any visiting faculty?**	YES

13.	**Course objective** *(about 50 words)***:** TO INTRODUCE UG AND PG STUDENTS TO CURRENT ISSUES IN TESTING

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Special Module that focuses on special topics, development and Research problems of importance in the area of VLSI Testing

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities

17. Brief description of laboratory activities

Module no.	Experiment description	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
COURSE TOTAL *(14 times 'P')*		

18. Suggested texts and reference materials

STYLE: Sonntag, R. E., Borgnakke, C., and Van Wylen, G. J., *Fundamentals of Thermodynamics*, 5th Ed., John Wiley, 2000.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	

19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICAL ENGINEERING DEPARTMENT
2.	**Course Title** *(< 45 characters)*	SPECIAL MODULE IN MACHINE LEARNING
3.	**L-T-P structure**	1-0-0
4.	**Credits**	1
5.	**Course number**	ELV832
6.	**Status** (*category* for *program*)	PE

7.	**Pre-requisites** (course no./title)	

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	small overlap with Neural Networks (EEL 781) and Statistical Pattern Recognition (EEL 754)
8.2	Overlap with any UG/PG course of other Dept./Centre	NONE
8.3	Supercedes any existing course	NONE

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1st sem ☐2nd sem ☒Either sem

11.	**Faculty who will teach the course**	INVITED VISITORS FROM INDUSTRIES AND/OR EE FACULTY
12.	**Will the course require any visiting faculty?**	POSSIBLY

13.	**Course objective** *(about 50 words)***:** TO INTRODUCE UG AND PG STUDENTS TO CURRENT ISSUES IN MACHINE LEARNING, AND CONNECTIONS BETWEEN MACHINE LEARNING AND VLSI

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Special Module that focuses on special topics, development and Research problems of importance in this area.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1		
2		
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5		
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7		
8		
9		
10		
11		
12		
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities

17. Brief description of laboratory activities

Module no.	Experiment description	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
COURSE TOTAL *(14 times 'P')*		

18. Suggested texts and reference materials

STYLE: Sonntag, R. E., Borgnakke, C., and Van Wylen, G. J., *Fundamentals of Thermodynamics*, 5th Ed., John Wiley, 2000.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	

19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICAL ENGINEERING DEPARTMENT
2.	**Course Title** *(< 45 characters)*	SPECIAL MODULE IN NANO ELECTRONICS
3.	**L-T-P structure**	1-0-0
4.	**Credits**	1
5.	**Course number**	ELV834
6.	**Status** (*category* for *program*)	PE

7.	**Pre-requisites** (course no./title)	EEL 732, and EEL 784 or EEL 218 and EEL329

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NONE
8.2	Overlap with any UG/PG course of other Dept./Centre	NONE
8.3	Supercedes any existing course	NONE

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1st sem ☐2nd sem ☒Either sem

11.	**Faculty who will teach the course**	INVITED VISITORS FROM INDUSTRIES
12.	**Will the course require any visiting faculty?**	YES

13.	**Course objective** *(about 50 words)***:** TO INTRODUCE UG AND PG STUDENTS TO CURRENT ISSUES IN INDUSTRIES IN NANO ELECTRONICS

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Special Module that focuses on special topics, development and Research problems of importance in the area of Nano Electronics.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1		
2		
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7		
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9		
10		
11		
12		
COURSE TOTAL *(14 times 'L')*		

16. Brief description of tutorial activities

17. Brief description of laboratory activities

Module no.	Experiment description	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
COURSE TOTAL *(14 times 'P')*		

18. Suggested texts and reference materials

STYLE: Sonntag, R. E., Borgnakke, C., and Van Wylen, G. J., *Fundamentals of Thermodynamics*, 5th Ed., John Wiley, 2000.

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	

19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	ELECTRICAL ENGINEERING DEPARTMENT
2.	**Course Title** *(< 45 characters)*	CMOS RF IC DESIGN
3.	**L-T-P structure**	3-0-0
4.	**Credits**	3
5.	**Course number**	ELL833
6.	**Status** (*category* for *program*)	PG Elective

7.	**Pre-requisites** (course no./title)	EEL 734 and EEL 782

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	NONE
8.2	Overlap with any UG/PG course of other Dept./Centre	NONE
8.3	Supercedes any existing course	NONE

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1st sem ☒2nd sem ☐Either sem

11.	**Faculty who will teach the course** Dr. S. Chatterjee, Dr. G. S. Visweswaran	
12.	**Will the course require any visiting faculty?**	No

13.	**Course objective** *(about 50 words)***:** TO INTRODUCE STUDENTS TO CURRENT ISSUES IN ANALOG AND MIXED SIGNAL RF IC DESIGN

14.	**Course contents** *(about 100 words) (Include laboratory/design activities)***:** Historical Aspects – From Maxwell to Current Wireless standards; The bridge between communication system designer and RF IC Designer: a) Comm. system characterization, b)RF System Characterization ; Transceiver Architectures – Motivation for the individual blocks; Lumped, passive RLC, RF properties of MOS, Tuned Amplifiers; ; LNAs: Noise sources, Cascades and LNA Design; Mixers – passive and active mixers ; Oscillators: Analysis Fundamentals, Inductors, LC Oscillators and VCOs; Frequency synthesizers:Principles, Integer N vs Fractional PLL, Design Concepts

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Historical Aspects – From Maxwell to Current Wireless standards	3
2	The bridge between communication system designer and RF IC Designer: Comm. System characterization, RF System characterization	5
3	Transceiver Architectures – Motivation for the individual blocks	3
4	Lumped, passive RLC, RF properties of MOS, Tuned Amplifiers	5
5	Low Noise Amplifiers: Noise Sourcse	3
6	Low Noise Amplifiers: Cascades	3
7	Low Noise Amplifiers: Design Example	2
8	Mixers: Introduction	2
9	Mixers: Active and Passive	4
10	Oscillators: Analysis Fundamentals and Inductors	3
11	Oscillators: LC Oscillators and VCOs	3
12	Frequency Synthesizers: Principles,Design, Integer N vs. Fractional PLL	6
COURSE TOTAL *(14 times 'L')*		42

16. Brief description of tutorial activities

17. Brief description of laboratory activities

Module no.	Experiment description	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
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10		
COURSE TOTAL *(14 times 'P')*		

18. Suggested texts and reference materials

STYLE: Sonntag, R. E., Borgnakke, C., and Van Wylen, G. J., *Fundamentals of Thermodynamics*, 5th Ed., John Wiley, 2000.

(1) "The Design of Radio-Frequency Integrated Circuits", Thomas H. Lee, Cambridge University Press, 2004. ISBN 0521613892
(2) "VLSI for Wireless Communication", Bosco Leung, Personal Education Electronics and VLSI series, Ed: Chharles G. Sodini, Pearson Education, 2002. ISBN 812970403X..
(3) "RF Microelectronics", Behzad Razavi, Prentice Hall PTR, 1998. ISBN 013887571X

19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	
19.2	Hardware	
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	
19.5	Equipment	
19.6	Classroom infrastructure	
19.7	Site visits	

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	
20.2	Open-ended problems	10%
20.3	Project-type activity	
20.4	Open-ended laboratory work	
20.5	Others (please specify)	

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**Device and Materials Characterization Laboratory**
3.	**L-T-P structure**	**0-0-6**
4.	**Credits**	**3**
5.	**Course number**	**ELP833**
6.	**Status** (*category* for *program*)	Elective for M.Tech. IEC and VDTT

7.	**Pre-requisites** (course no./title)	Microelectronics, Compact Modeling

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☐1stsem ☒2ndsem ☐Either sem -

11.	**Faculty who will teach the course** **Dr. Abhisek Dixit, Dr. Anuj Dhawan, Dr. M. Suri, Prof. M. Jagadesh Kumar**

12.	**Will the course require any visiting faculty? (yes/no)**	no

13.	**Course objectives** *(about 50 words)***:** In response to national policy on ESDM, our country is gearing up to answer the global challenge of high-end manufacturing. “Make in India” mission by the Hon’ble prime minister of India revolves around availability of engineering talent pool and abundance of natural resources in India. At this critical juncture, our IEC and VDTT students have to be readied to take up roles in the upcoming semiconductor manufacturing sector.

	This course it targeted to impart necessary semiconductor characterization skills to help our graduates recognize the opportunity and stand up to the challenge.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** Skill development in semiconductor modeling and characterization through hands on electrical characterization experiments. This includes wafer-level DC and RF characterization of p-n junction diode, MOS capacitor and transistor, photo-electric characterization of solar cells, TCAD and compact modeling of these devices, Materials Characterization (SEM, AFM, TEM, etc.)

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
	COURSE TOTAL *(14 times 'L')*	

16. Brief description of tutorial activities: Tutorials are embedded in the Lab.

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours
1	TCAD Modeling Experiments	4.5
2	Compact Modeling Experiments	4.5
3	Characterization of Solar Cells	5
4	DC Characterization	7
5	RF Characterization	5
6	Materials Characterization (SEM, AFM, TEM, etc.)	10
7	Lab Project	6
	Total Hours	**42**

18. lescription of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours
1	TCAD Modeling Experiments	9
2	Compact Modeling Experiments	9
3	Characterization of Solar Cells	12
4	DC Characterization	14

5	RF Characterization	10
6	Materials Characterization (SEM, AFM, TEM, etc.)	20
7	Lab Project	18

19. Suggested texts and reference materials: to be provided by the instructor (STYLE: Author name and initials, Title, Edition, Publisher, Year)

1. C. K. Sarkar, Technology Computer Aided Design, CRC Press, 2013
2. G. Gildenblat, Compact Modeling, Springer, 2010
3. C. S. Solanki, Solar Photovoltaics, Second Edition, PHI, 2011
4. Nicollian and Brews, MOS Physics and Technology, Wiley, 2002
5. D. Schroder, Semiconductor Material and Device Characterization, Wiley, 2006
6. M. J. Deen, CMOS RF Modeling, Characterization, and Applications, World Scientific, 2002

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Synopsys-Sentaurus, Keysight-ICCAP
20.2	Hardware	Wafer probing station, Parameter Analyzer, CV measurement unit, VNA, Sun simulator
20.3	Teaching aides (videos, etc.)	none
20.4	Laboratory	Wafer-level characterization lab, computational lab
20.5	Equipment	None
20.6	Classroom infrastructure	LCD needed
20.7	Site visits	none
20.8	Others (please specify)	none

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	25%
21.2	Open-ended problems	25%
21.3	Project-type activity	15%
21.4	Open-ended laboratory work	35%
21.5	Others (please specify)	0

Date: (Signature of the Head of the Department)

COURSE TEMPLATE

1.	**Department/Centre proposing the course**	**Electrical Engineering**
2.	**Course Title** *(< 45 characters)*	**Special Module in Semiconductor Business Management**
3.	**L-T-P structure**	**1-0-0**
4.	**Credits**	**1**
5.	**Course number**	**ELV833**
6.	**Status** (*category* for *program*)	M.Tech. and B.Tech. Elective

7.	**Pre-requisites** (course no./title)	none

8.	**Status vis-à-vis other courses** *(give course number/title)*	
8.1	Overlap with any UG/PG course of the Dept./Centre	No
8.2	Overlap with any UG/PG course of other Dept./Centre	No
8.3	Supersedes any existing course	No

9.	**Not allowed for** (indicate program names)	

10.	**Frequency of offering**	☐Every sem ☒1stsem ☐2ndsem ☐Either sem -

11.	**Faculty who will teach the course** **Dr. Abhisek Dixit, Dr. Bhaskar Mitra, Dr. M. Singh**

12.	**Will the course require any visiting faculty? (yes/no)**	no

13.	**Course objectives** *(about 50 words)***:** In response to national policy on ESDM, our country is gearing up to answer the global challenge of high-end manufacturing. “Make in India” mission by the Hon’ble prime minister of India revolves around availability of engineering talent pool and abundance of natural resources in India. At this critical juncture, our IEC and VDTT students have to be readied to take up leadership roles in the upcoming semiconductor

	manufacturing sector. This course it targeted to impart necessary business acumen to help our graduates recognize the opportunity and stand up to the leadership challenge.

14.	**Course contents (about 100 words) (Include laboratory/design activities):** To educate students about semiconductor business. This includes business domains in semiconductors, latest business challenges, market trends and forecasts, business planning and incubation, execution and delivery, technical and financial analysis of R&D , business and finance models of chip manufacturing units (or fabs.), foundries, and solar power plants.

15. Lecture Outline *(with topics and number of lectures)*

Module no.	Topic	No. of hours
1	Alignment: Global Electronics Industry and Players at a glance	1
2	The Semiconductor Industry: Challenges, trends, and forecasts	1
3	Planning and Incubation: Business Plan, Incubation Process	2
4	Execution and Delivery: AGILE, LEAN	2
5	R&D: Techno-financial analysis	1
6	Models: Chip Manufacturing, Foundries, Solar Power Plants, and others	5
7	Case study: presentations by students	2
COURSE TOTAL *(14 times 'L')*		**14**

16. Brief description of tutorial activities: Tutorials are embedded in the Lectures.

Module no.	Description	No. of hours

17. Brief description of laboratory activities

Module no.	Description	No. of hours

18. Brief description of module-wise activities pertaining to self-study component (mandatory for 700 / 800 level courses)

Module no.	Description	No. of hours

19. Suggested texts and reference materials: to be provided by the instructor

STYLE: Author name and initials, Title, Edition, Publisher, Year.

20. Resources required for the course *(itemized & student access requirements, if any)*

20.1	Software	Matlab, MS-EXCEL, SAM
20.2	Hardware	none
20.3	Teaching aides (videos, etc.)	none
20.4	Laboratory	Any computer lab
20.5	Equipment	None
20.6	Classroom infrastructure	LCD needed

20.7	Site visits	none
20.8	Others (please specify)	none

21. Design content of the course *(Percent of student time with examples, if possible)*

21.1	Design-type problems	15%
21.2	Open-ended problems	15%
21.3	Project-type activity	30%
21.4	Open-ended laboratory work	0
21.5	Others (please specify)	0

Date: (Signature of the Head of the Department)