

COURSE TEMPLATE

1.	Department / Centre proposing the course	ELECTRICAL ENGINEERING
2.	Course Title (< 45 characters)	ELECTRONICS LABORATORY I
3.	L-T-P structure	0 - 0 - 3
4.	Credits	1 . 5
5.	Course number	EEP 201
6.	Status (category for program)	Departmental Core

7.	Pre-requisites (course no./title)	EEL 101
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8.	Status vis-à-vis other courses (give course number/title)	
8.1	Overlap with any UG/PG course of the Dept./Centre	NIL
8.2	Overlap with any UG/PG course of other Dept./Centre	NIL
8.3	Supercedes any existing course	NIL

9.	Not allowed for (indicate program names)	NONE
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10.	Frequency of offering	☒ Every sem ☐ 1 st sem ☐ 2 nd sem ☒ Either sem
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11.	Faculty who will teach the course G. S. Visweswaran, Anuj Dhawan, S. Chatterjee, Jayadeva, B. Bhaumik	
12.	Will the course require any visiting faculty?	NO

13.	Course objective (about 50 words): To introduce the students to the world of digital electronics and Design with	
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	gates as well as FPGAs.
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14.	Course contents <i>(about 100 words) (Include laboratory/design activities):</i> Experiment on the bread-board, and in VHDL for combinational logic gates. Gate-level description. Experiments on the bread-board, and in VHDL for MUXs, adders. System-level description. Implementation of flip-flops – on the bread-board and in VHDL. Counters as FSMs, both synchronous and asynchronous, and their implementation both on the bread-board and on the FPGA. Shift registers, sequence detectors and sequence generators and related experiments both on the bread-board and on the FPGA. Design and demonstrate a small project on the FPGA.
15.	Lecture Outline <i>(with topics and number of lectures)</i>

Module no.	Topic	No. of hours
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
COURSE TOTAL (14 times 'L')		

16. Brief description of tutorial activities

NA

17. Brief description of laboratory activities

Moduleno.	Experiment description	No. of hours
1	Experiment on the bread-board, and in VHDL for combinational logic gates. Gate-level description.	3
2	Experiment on the bread-board, and in VHDL for muxs, adders. System-level description.	6
3	Implementation of flip-flops – on the bread-board and in VHDL.	6
4	Counters as FSMs. Both synchronous and asynchronous. Implementation both on the bread-board and on the FPGA.	6
5	Shift registers, sequence detectors and sequence generators. Experiments both on the bread-board and on the FPGA.	12
6	Shift registers, sequence detectors and sequence generators. Experiments both on the bread-board and on the FPGA.	9
7		
8		
9		
10		
COURSE TOTAL (14 times 'P')		42

18. Suggested texts and reference materials

STYLE: Author name and initials, Title, Edition, Publisher, Year.

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19. Resources required for the course *(itemized & student access requirements, if any)*

19.1	Software	Xilinx
19.2	Hardware	Desktop Computer, FPGA kits
19.3	Teaching aides (videos, etc.)	
19.4	Laboratory	UG Electronics Laboratory
19.5	Equipment	Power Supply, Signal Generator and Oscilloscope
19.6	Classroom infrastructure	Projection system
19.7	Site visits	none

20. Design content of the course *(Percent of student time with examples, if possible)*

20.1	Design-type problems	65%
20.2	Open-ended problems	
20.3	Project-type activity	15%
20.4	Open-ended laboratory work	
20.5	Others (please specify)	20% (routine testing)

Date: March 25, 2013

(Signature of the Head of the Department)