**Indian Institute of Technology, Delhi**
**EEL 101: Fundamentals of Electrical Engineering**
**Tutorial 9, 17th April, 2008**

1. Fig. (a) shows a CMOS inverter, typically used in all modern digital circuits. Both the nMOS device behaves in the following fashion:

   $$i_D = K(v_{GS} - V_T)^2$$

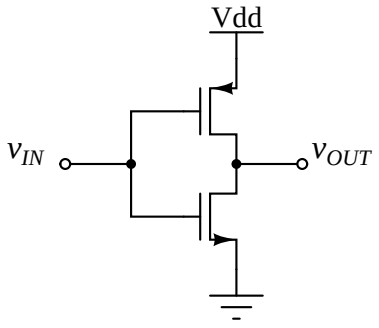
   for $v_{DS} > v_{GS} - V_T$ (saturation region), and

   $$i_D = 2K((v_{GS} - V_T)v_{DS} - v_{DS}^2/2)$$

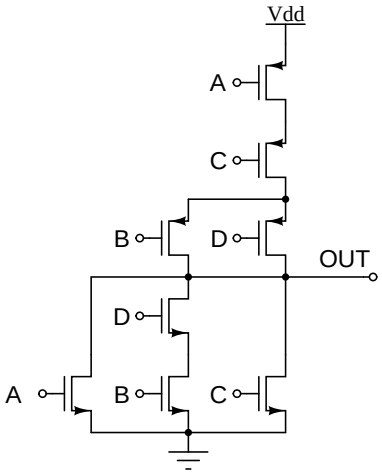
   for $v_{DS} < v_{GS} - V_T$ (linear region). The pMOS device also behaves in an identical fashion, except that the equations are for $v_{SG}$ and $v_{SD}$. For both of the devices assume $V_T$ to be 0.5 Volt, $K$ to be 10 mA/V$^2$. Assume $VDD$ to be 3 Volts. Write out the expression for $v_{OUT}$ when the pMOS is in saturation and the nMOS is in the linear region. Write out an expression for $v_{OUT}$ when the nMOS is in saturation and the pMOS is in the linear region. What does the input have to be when both the nMOS and the pMOS are in saturation?

2. Draw the linear small signal model for the CMOS inverter of Fig. (a). Evaluate $g_m$ of both the nMOS and the pMOS devices when the input is biased at 1.5 Volts. If $r_{ds}$ of both the nMOS and the pMOS devices is 100 k$\Omega$, what will be the slope of the $v_{OUT}$ versus $v_{IN}$ curve when both the nMOS and the pMOS devices are in the saturation region?

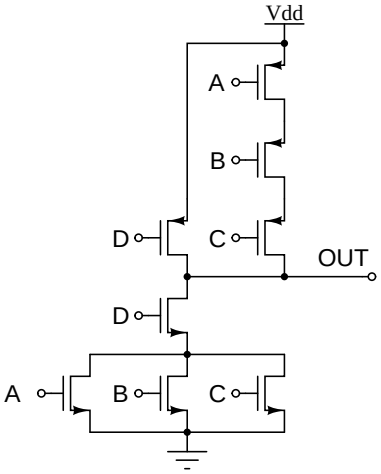
3. Analyze the logic functions implemented by the circuits in Figures (b), (c), (d) and (e).


Vdd
$v_{IN}$
$v_{OUT}$

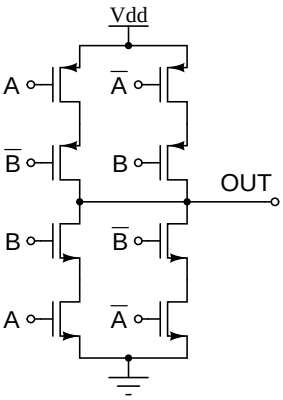
(a)


Vdd
A
C
B
D
OUT
D
A
B
C

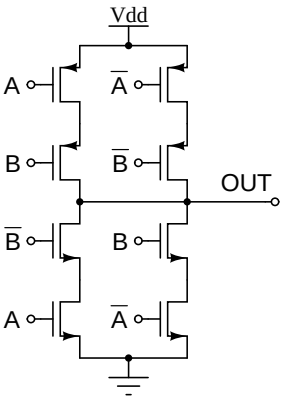
(b)


Vdd
A
B
D
C
OUT
D
A
B
C

(c)


Vdd
A
$\overline{A}$
$\overline{B}$
B
OUT
B
$\overline{B}$
A
$\overline{A}$

(d)


Vdd
A
$\overline{A}$
B
$\overline{B}$
OUT
$\overline{B}$
B
A
$\overline{A}$

(e)