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1. Half adders generate P_i, G_i (2ns)
2. CLA (1st layer) $\longrightarrow P_I, G_I$ (4ns)
3. CLA (2nd layer) $\longrightarrow C_0, C_4, C_8, C_{12}$ (6ns)
4. CLA (1st layer) $\longrightarrow C_1, C_2, C_3$ etc. (8ns)
5. Layer of half adders $\longrightarrow S_i$ (10ns)

$$C_4 = G_I + P_I C_0$$

$$C_5 = G_4 + P_4 C_4$$



$$C_4 = G_I + P_I C_0$$

$$C_8 = G_{II} + P_{II} G_I + P_{II} P_I C_0$$

$$C_{12} = G_{III} + P_{III} G_{II} + P_{III} P_{II} G_I + P_{III} P_{II} P_I C_0$$

$$C_{16} = G_{IV} + P_{IV} G_{III} + P_{IV} P_{III} G_{II} + P_{IV} P_{III} P_{II} G_I + P_{IV} P_{III} P_{II} P_I C_0$$

$$G_1^2$$

$$+ P_{IV} P_{III} P_{II} P_I C_0$$

$$P_1^2$$

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$$C_{16} = G_1^2 + P_1^2 C_0$$

$$C_{32} = G_2^2 + P_2^2 G_1^2 + P_2^2 P_1^2 C_0$$

$$C_{48} = G_3^2 + P_3^2 G_2^2 + P_3^2 P_2^2 G_1^2 + P_3^2 P_2^2 P_1^2 C_0$$

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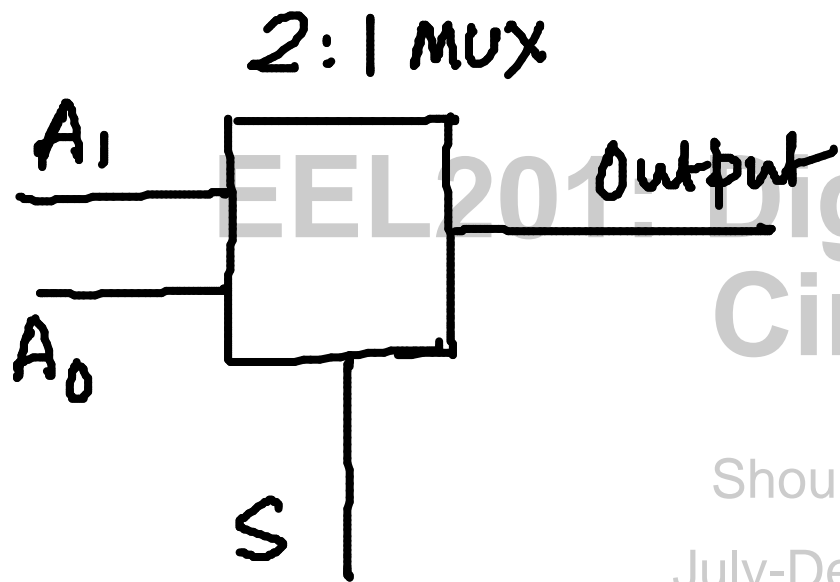
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- | | | |
|---|--------------------------------------|-----|
| 1. Layer of half adders | $\rightarrow P_i, G_i$ | 2d |
| 2. Layer 1 of CLA (16x) | $\rightarrow P_I, G_I$ | 4d |
| 3. Layer 2 of CLA (4x) | $\rightarrow P_i^2, G_i^2$ | 6d |
| 4. Layer 3 of CLA (C_0) ^{1x} | $\rightarrow C_{16}, C_{32}, C_{48}$ | 8d |
| 5. Layer 2 of CLA | $\rightarrow C_4, C_8, C_{12}$ | 10d |
| 6. Layer 1 of CLA \rightarrow all other carries | C_{20}, C_{24}, C_{28} | 12d |
| | C_{36}, C_{40}, C_{44} | |
| 7. Half adders $\rightarrow S_i$ | C_{52}, C_{56}, C_{60} | 14d |



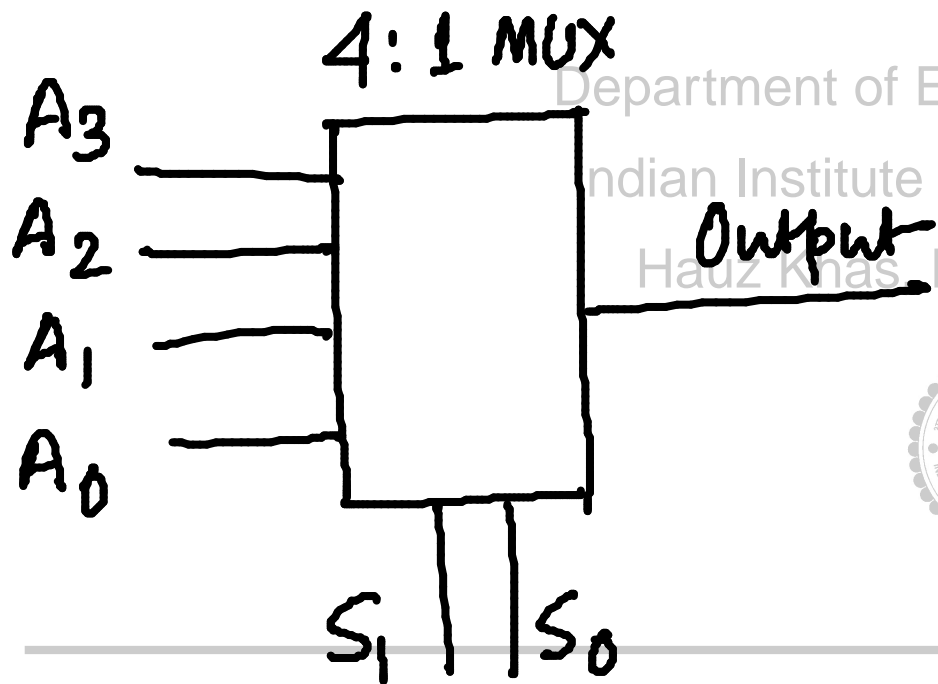
Multiplexers



if \bar{S} , Output = A₀

if S, Output = A₁

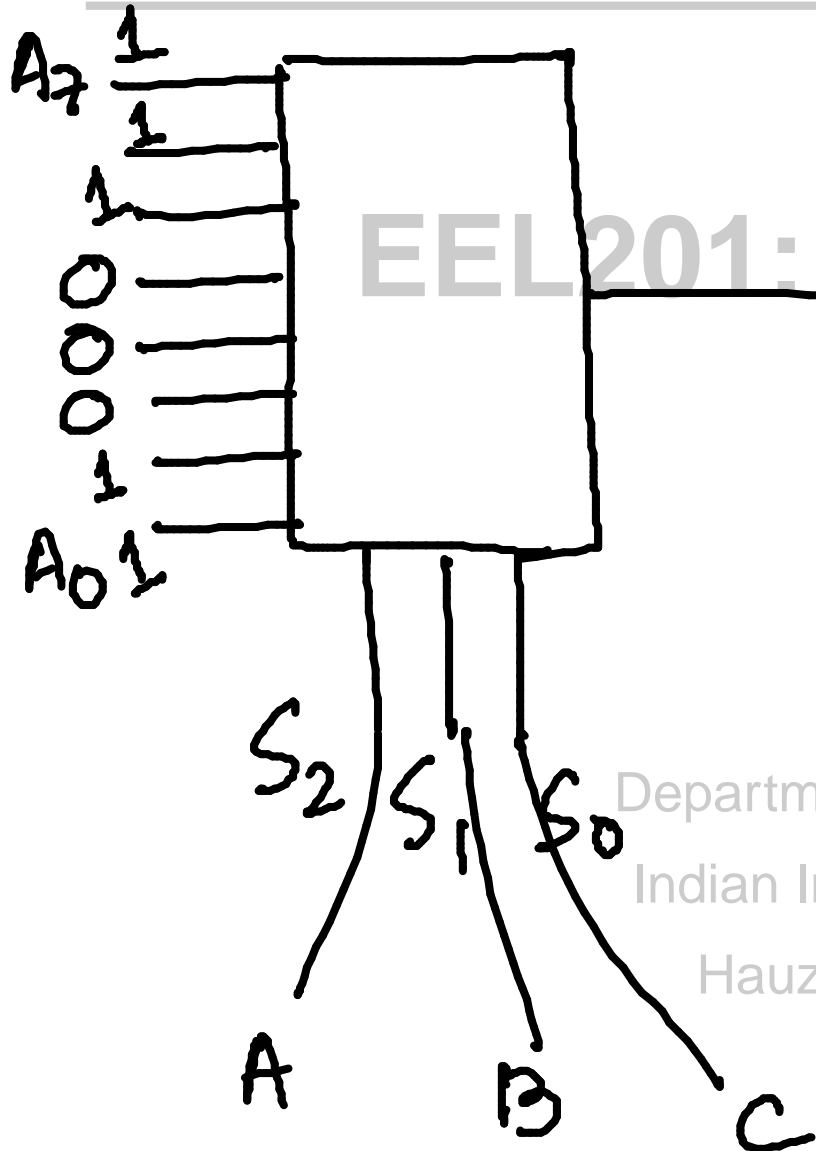
$$\text{Output} = A_1 S + A_0 \bar{S}$$



$$\begin{aligned} \text{Output} = & \bar{S}_1 \bar{S}_0 A_0 + \bar{S}_1 S_0 A_1 \\ & + S_1 \bar{S}_0 A_2 + S_1 S_0 A_3 \end{aligned}$$



8:1 MUX



$$f = \sum 0, 1, 5, 6, 7$$

EEL201: Digital Electronic Circuits

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