

Shouri Chatterjee

July-December 2009

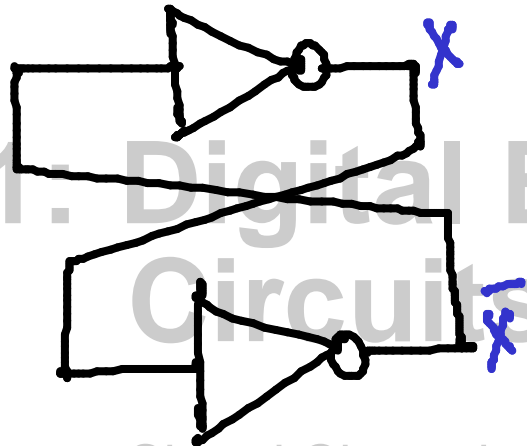
"Oscillator"

Period = $6d$

Memory cell (SRAM)



EEL201: Digital Electronic Circuits

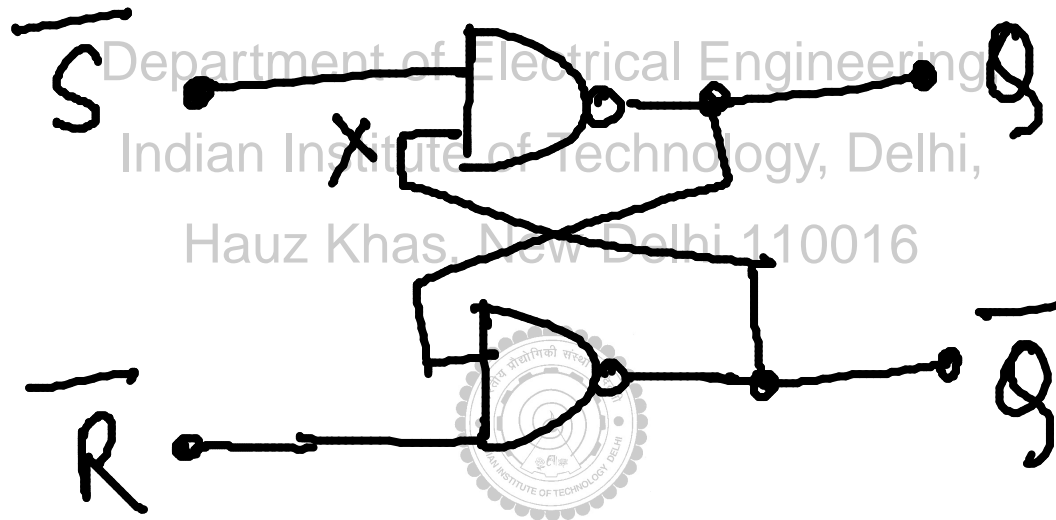


SRAM cell

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"race condition"



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EEL201: Digital Electronic Circuits

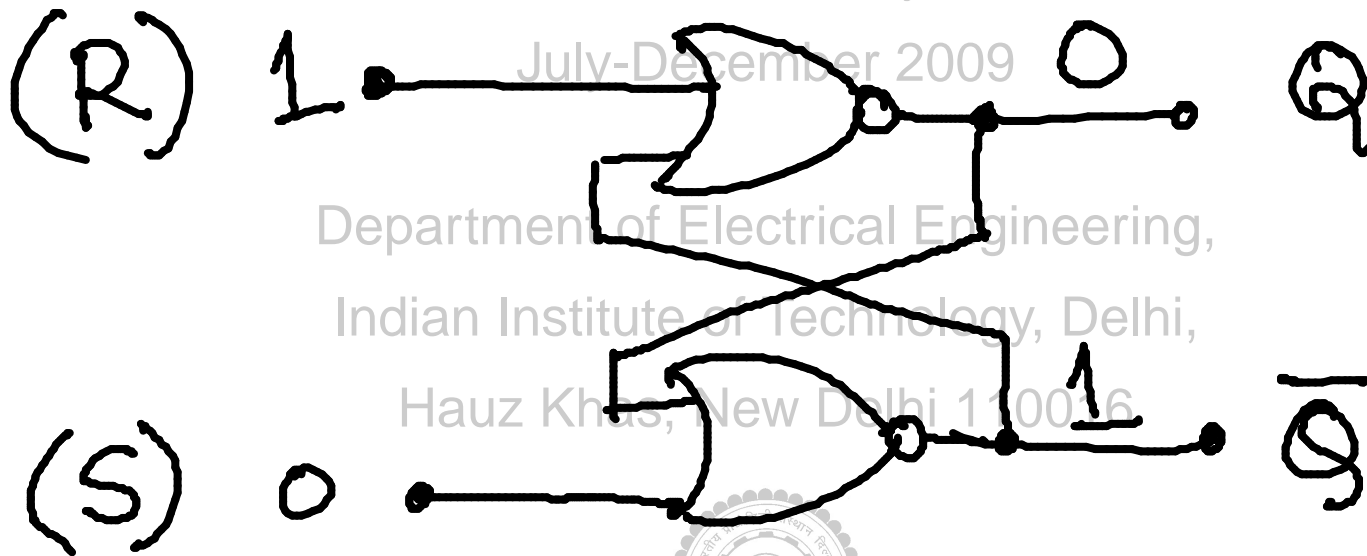
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Set - Reset latch

S	R	Q	\bar{Q}
0	0	Q	\bar{Q}
0	1	0	1
1	0	1	0
1	1	0/1	0/1

← invalid state

