Hardware description languages

VHDL

Verilog

Statements
- Concurrent
- Sequential

Datatypes
- Wire
- reg

0, 1, X, Z

Combinational logic

```
and  inst_name (output, inputs, ...);
or
nand
nor
xor
xnor
not
```

probably a wire


```
assign A = B & C;
       A = (~B & C) | (~C & B);
       A = B + C;
```

Sequential statements

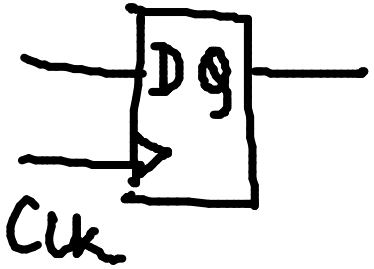
```
always @(X3,X2,X1,X0,S1,S0)
begin
  case(S1,S0)
    00: Out = X0;
    01: Out = X1;
    10: Out = X2;
    11: Out = X3;
end
```

case/switch/break

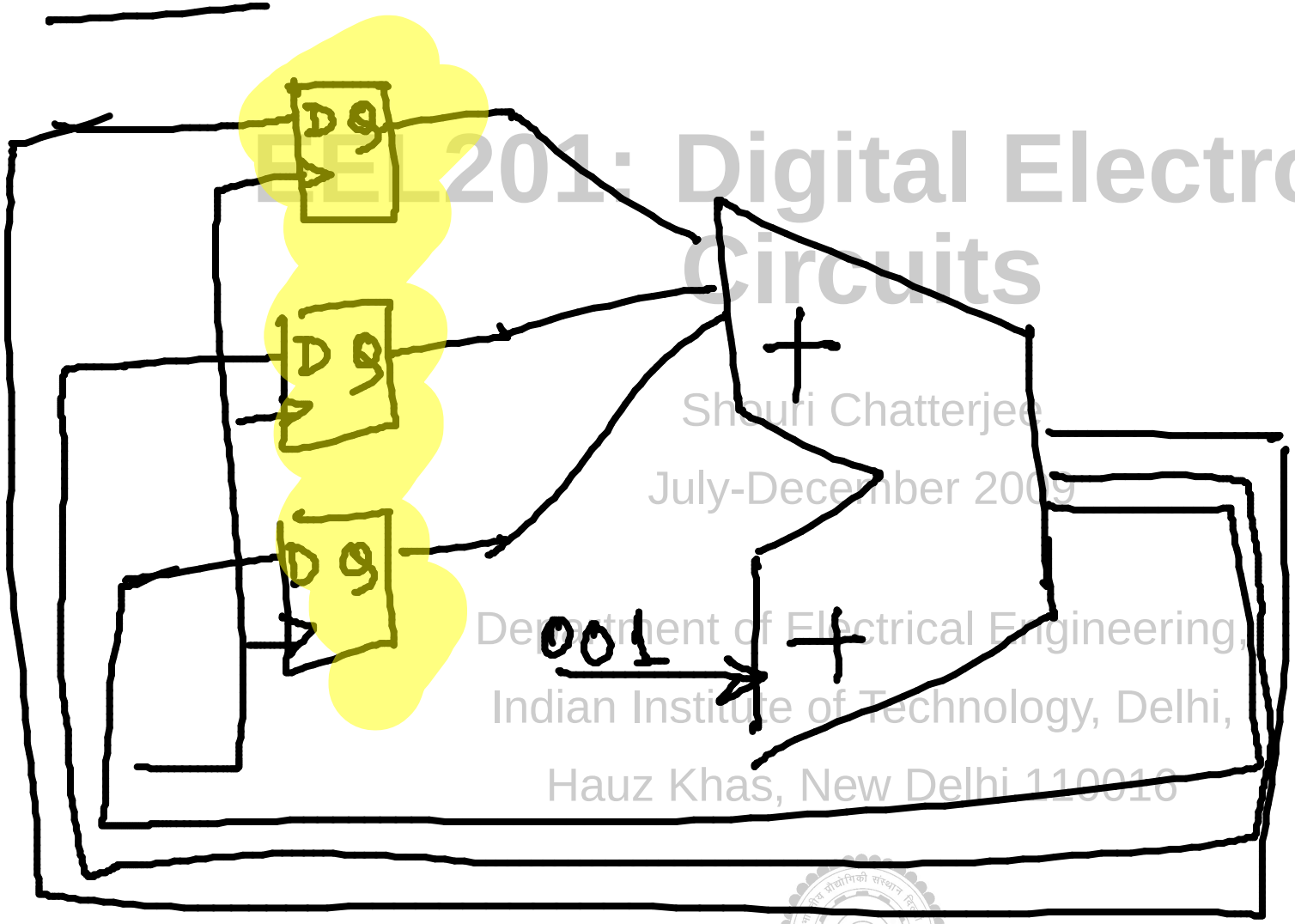
if/then/else

D-Flip-flops

```
always @ ( pos. edge of clk
         edge of clk and clk = 1 )
{
    Current state = next state;
}
```



Counter



Q[2:0], D[2:0]

```
{ always @(posedge of clk)
      Q = D;
  always @( Q )
      D = Q + 1; }
```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RTL — Register transfer level coding style

Not recommended → Behavioral programming

EEL201: Digital Electronic Circuits

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