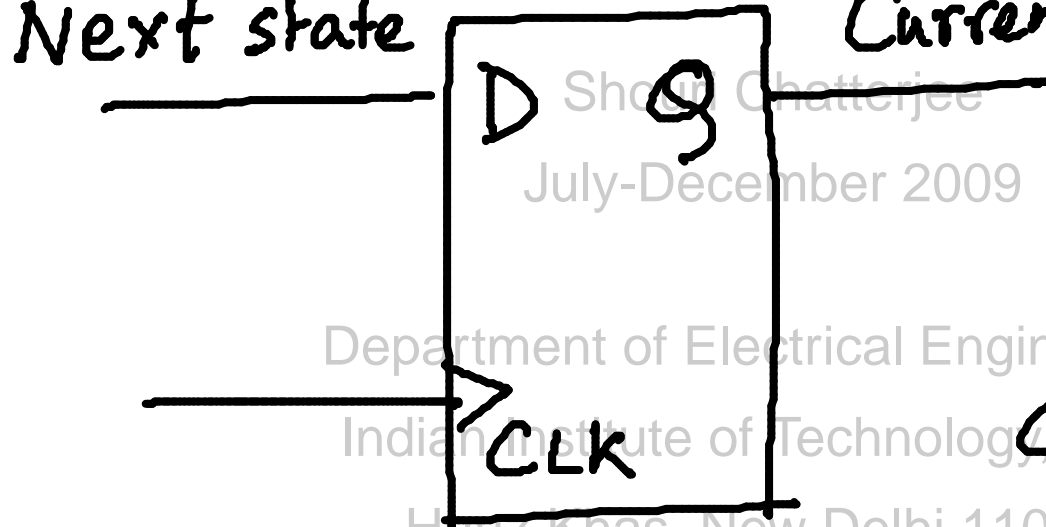


1) Current and next state

2) Timing

Next state Current state

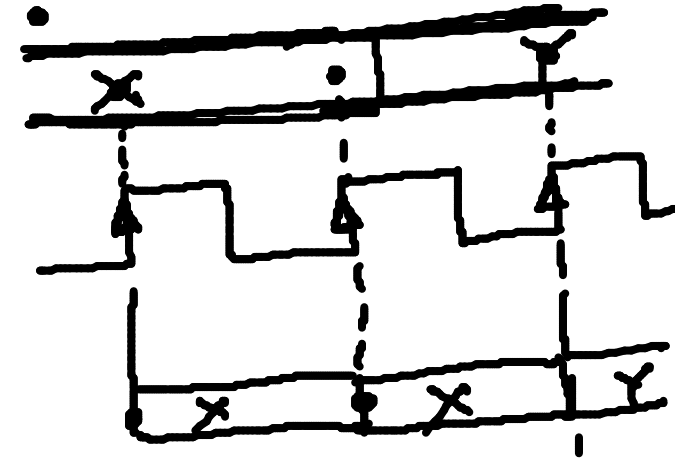


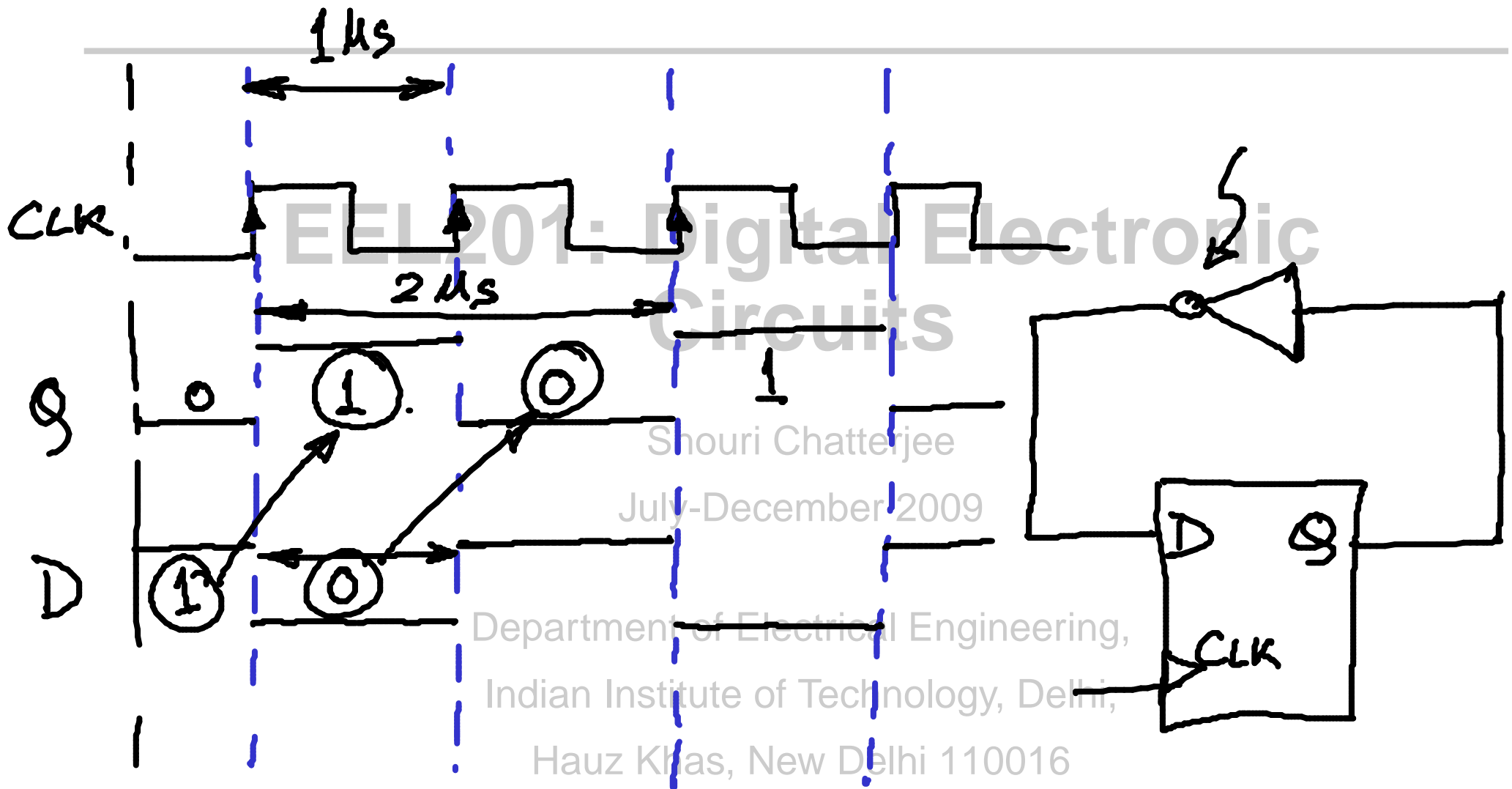
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D

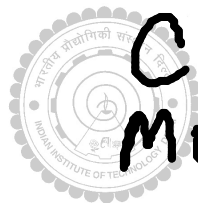
CLK

Q





freq $\div 2$



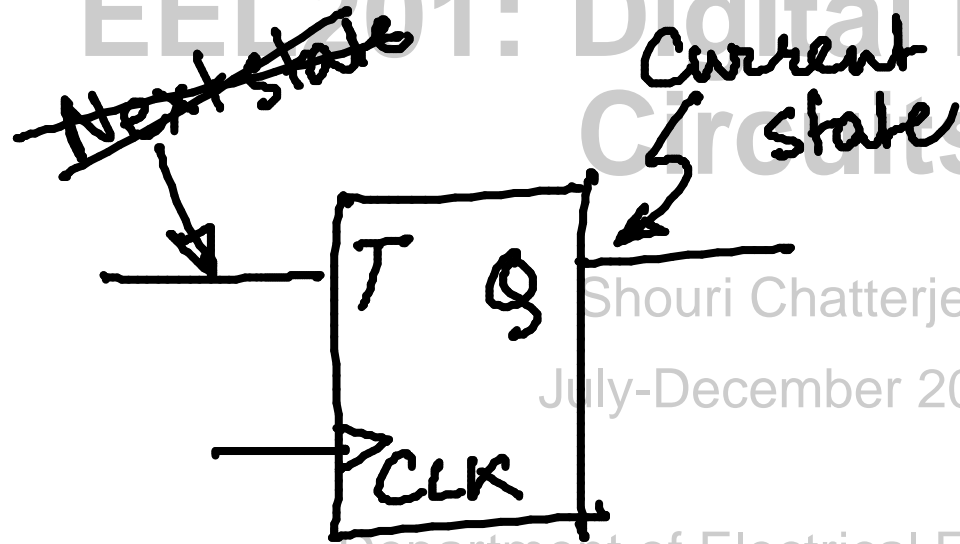
Clock divider
Modulo-2 counter

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D → current input ↔ next state

Q → previous input ↔ current state

EEL 201: Digital Electronic Circuits



T	Q
0	0
1	1

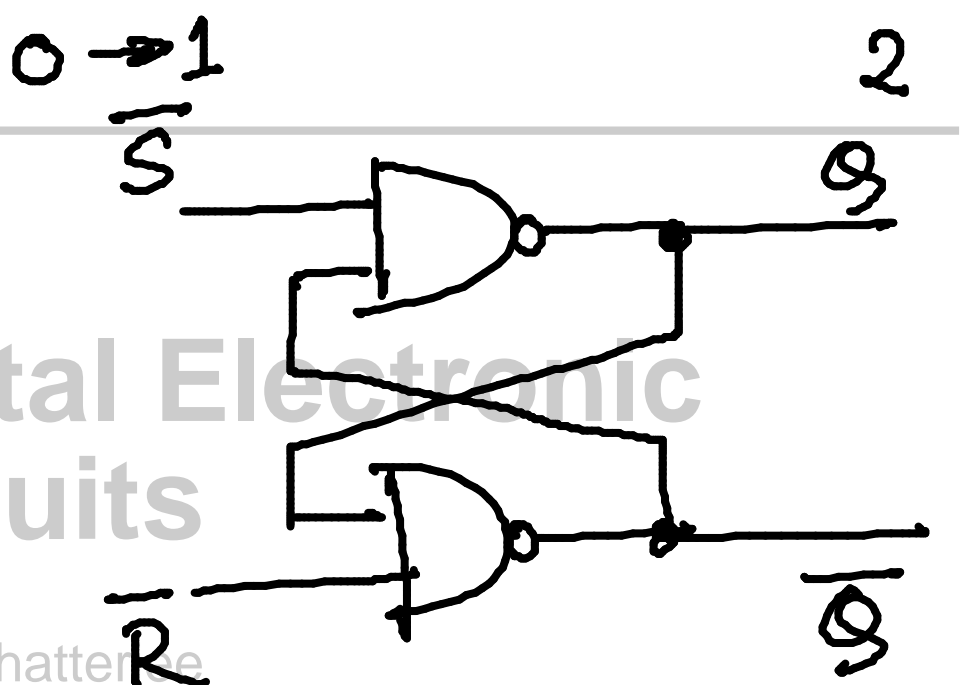
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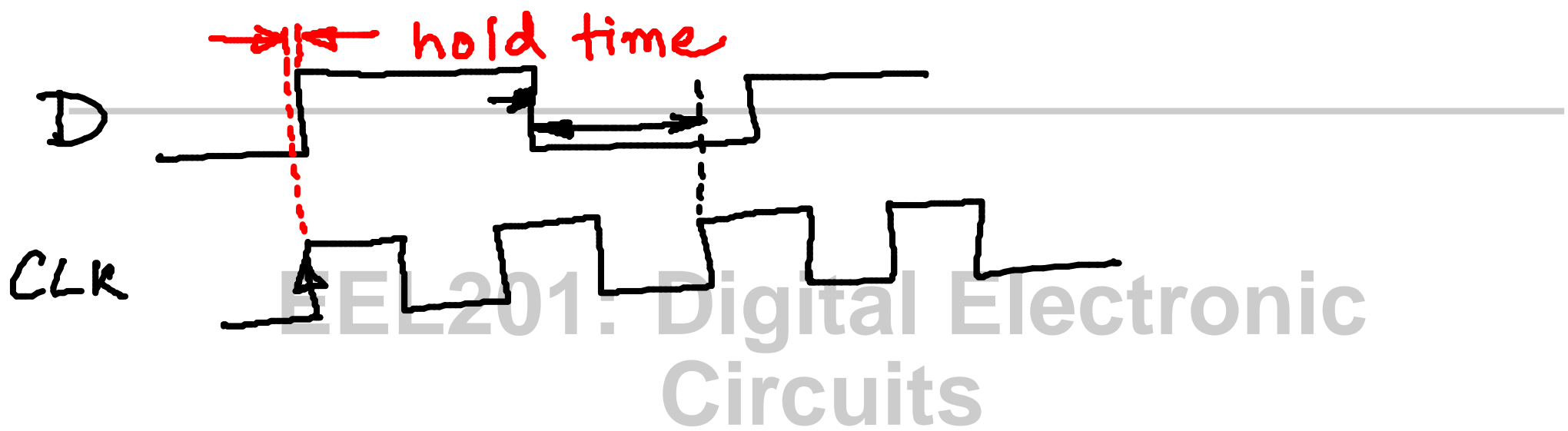
Setup time
 ✓ Hold time

SR latches, level sensitive
 f/f s,
 edge trig f/f s



What is the min time I have the hold
 the inputs to a constant value so that I
 get correct outputs?

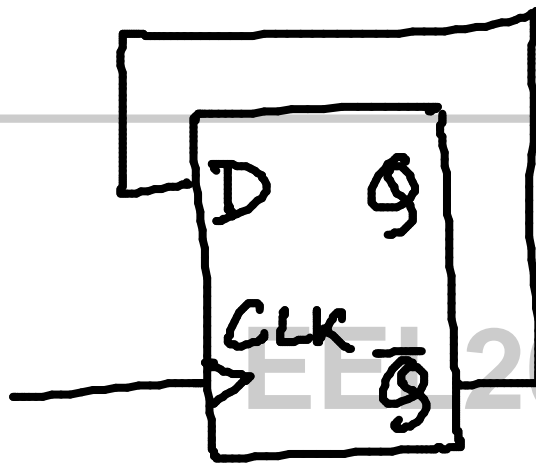




Setup time

What is the min time I have to keep the input constant before the edge of the clock, so that I get correct output?





EEET 201: Digital Electronic Circuits



Modulo-4 Counter

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1. How many states ?

2. How many flip-flops ?



State table

Current State

Next State

$Q_1 Q_0$

$D_1 D_0$

0 0

0 1

0 1

1 0

1 0

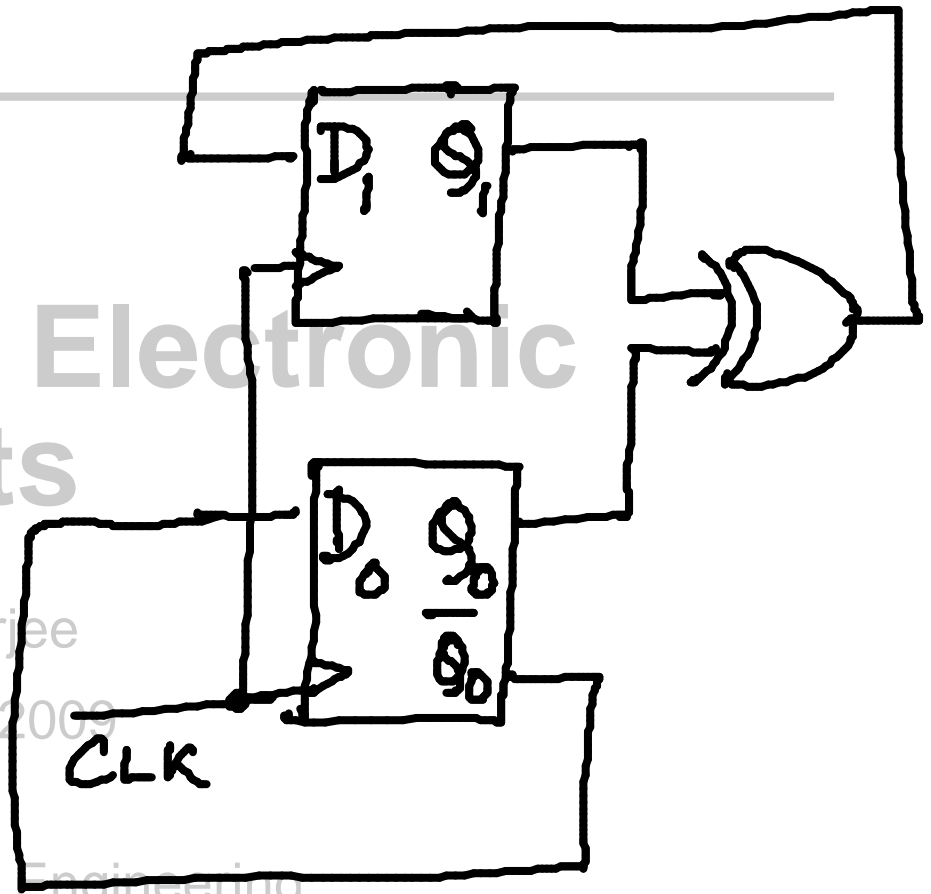
1 1

1 1

0 0

$$D_1 = Q_1 \oplus Q_0$$

$$D_0 = Q_0$$



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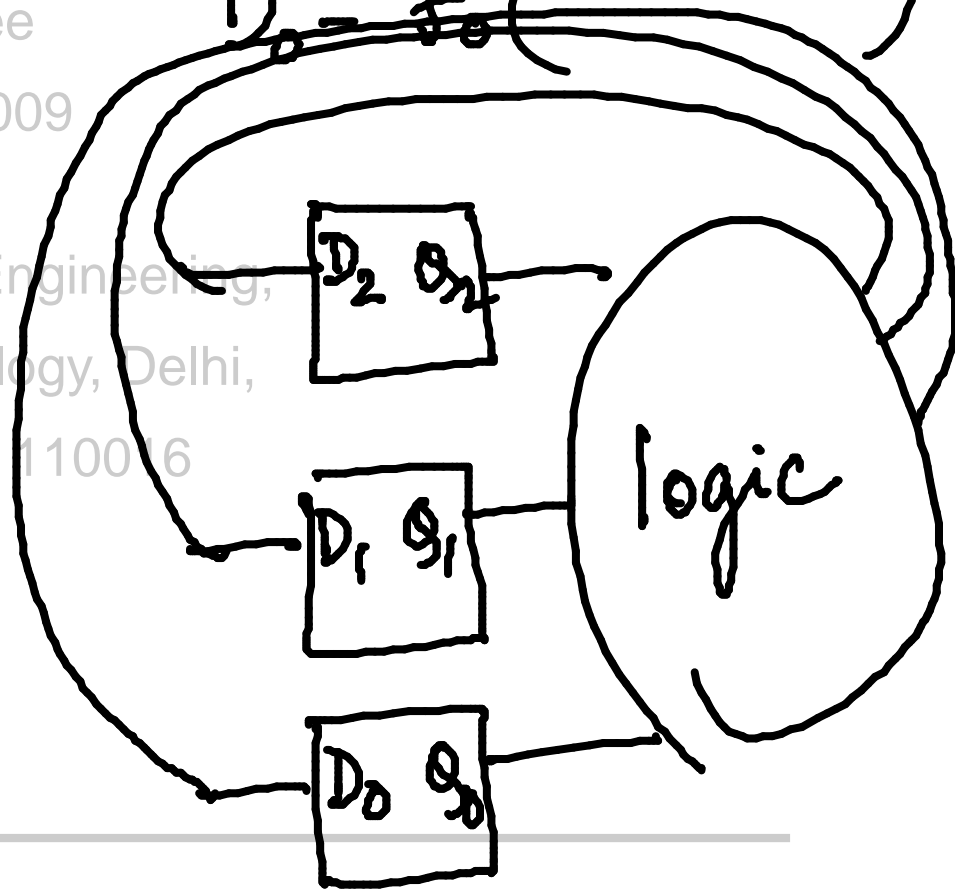
Mod - 7 counter

Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	X	X	X

$$D_2 = f_2(Q_2, Q_1, Q_0)$$

$$D_1 = f_1(Q_2, Q_1, Q_0)$$

$$D_0 = f_0(Q_2, Q_1, Q_0)$$



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