

# Synchronous circuits

✓ Memory cell

✓ Clocks

✓ R-S Latch

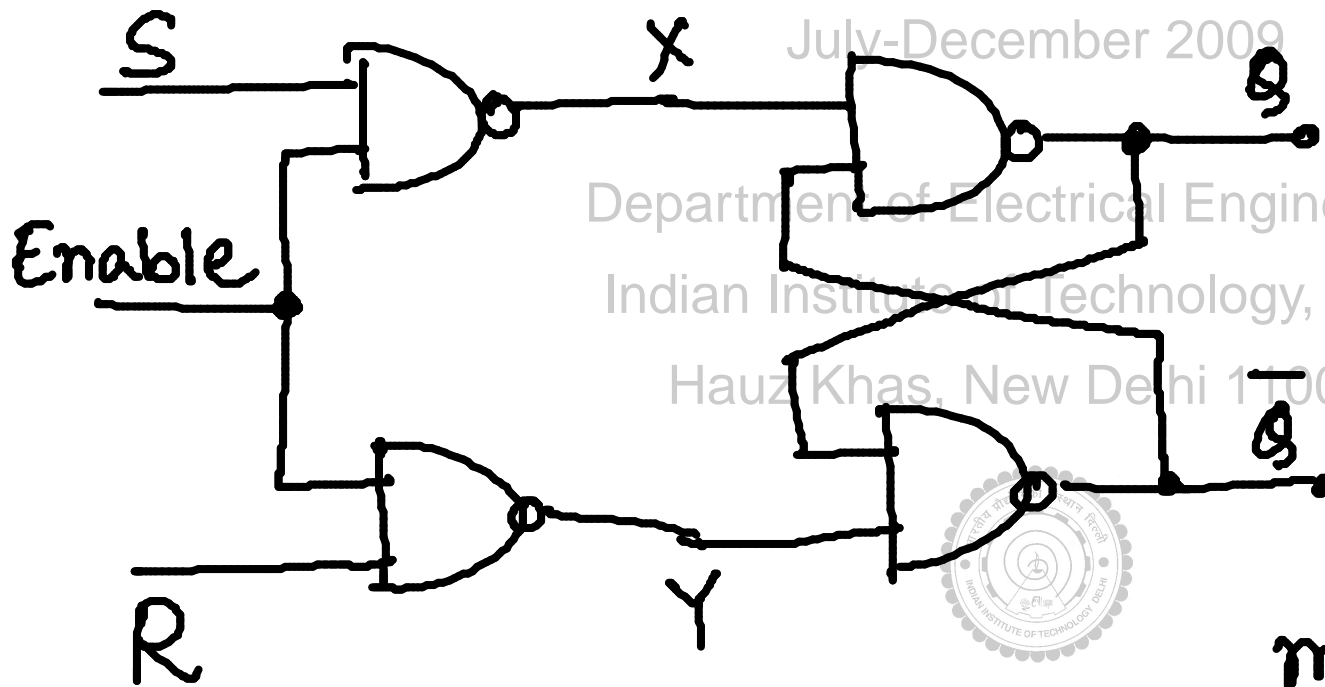
EEL 201: Digital Electronic Circuits

## Level sensitive flip-flops / latches

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July-December 2009

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Hauz Khas, New Delhi 110016

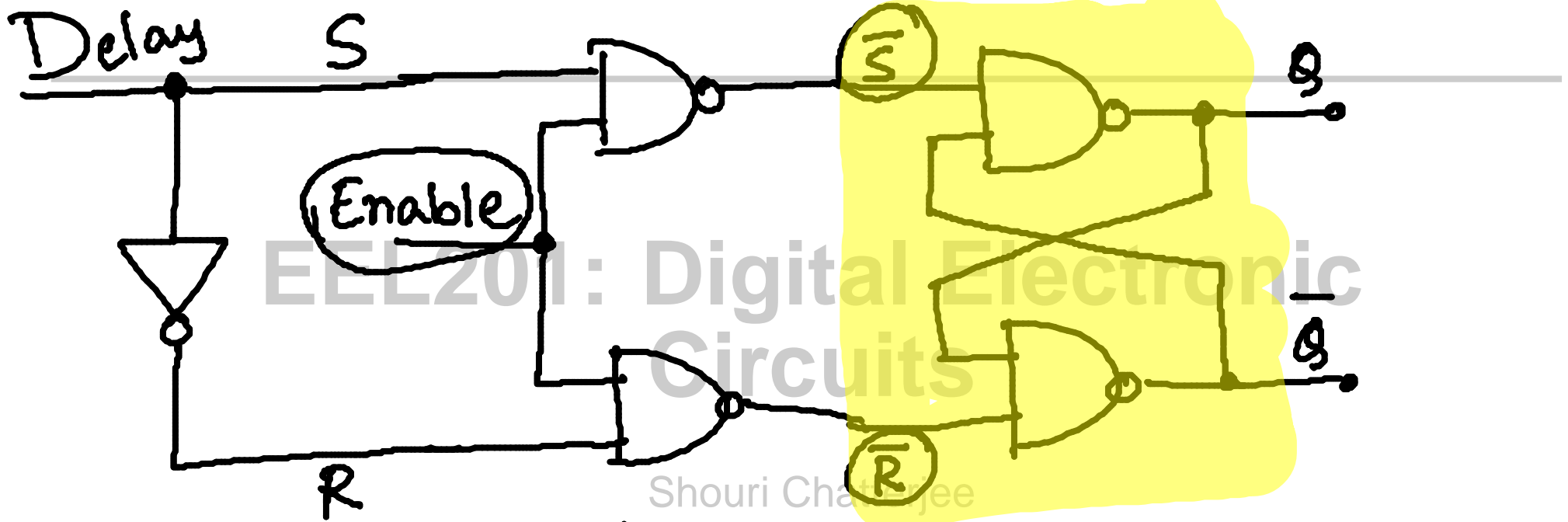


Enable = 1

$$\begin{aligned} X &= S \\ Y &= R \end{aligned}$$

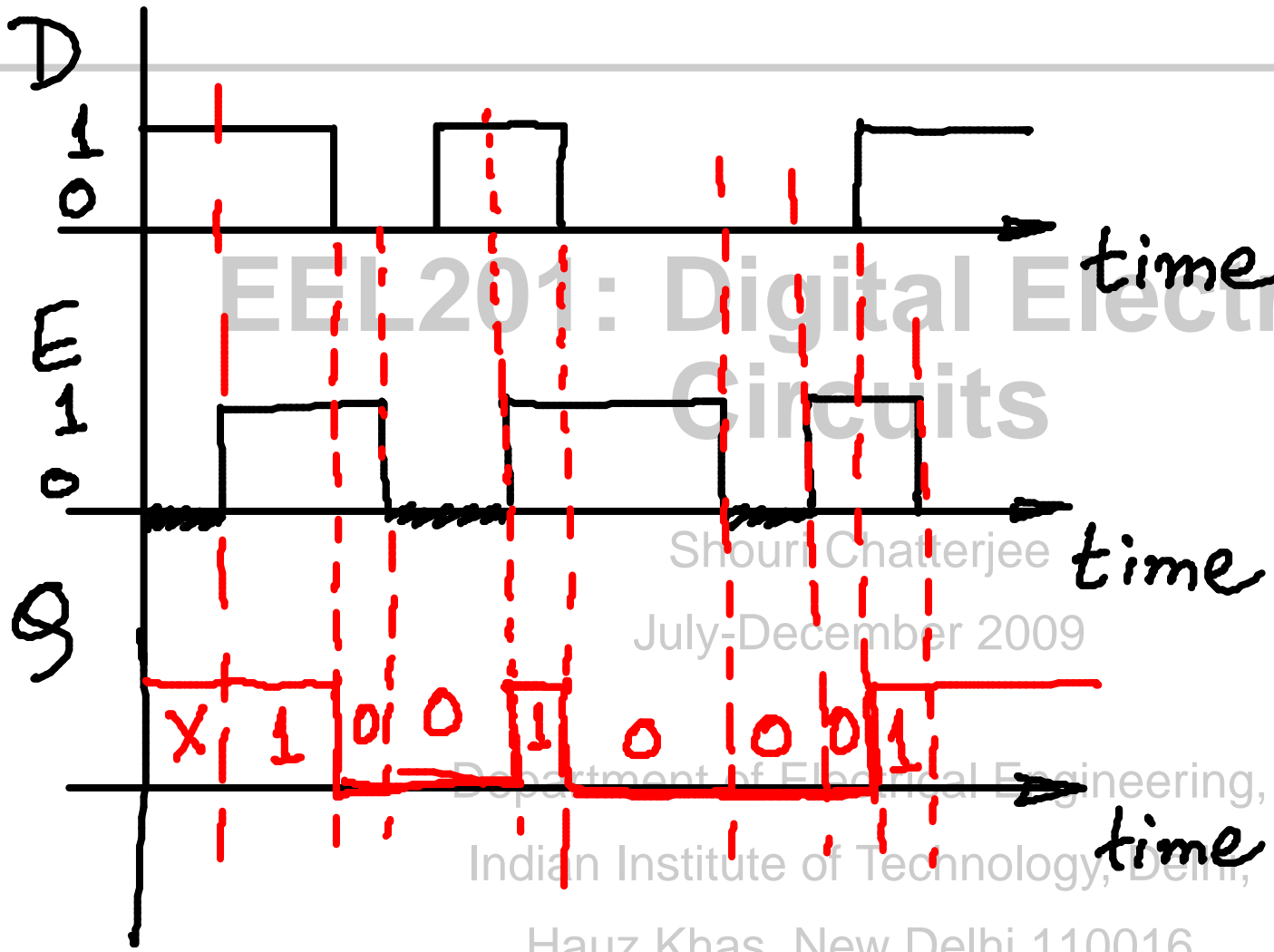
Enable = 0

memory  $\begin{cases} X = 1 \\ Y = 1 \end{cases}$



D	E	Q	Q̄
X	0	Q	Q̄
0	1	0	1
1	1	1	0





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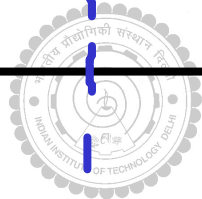
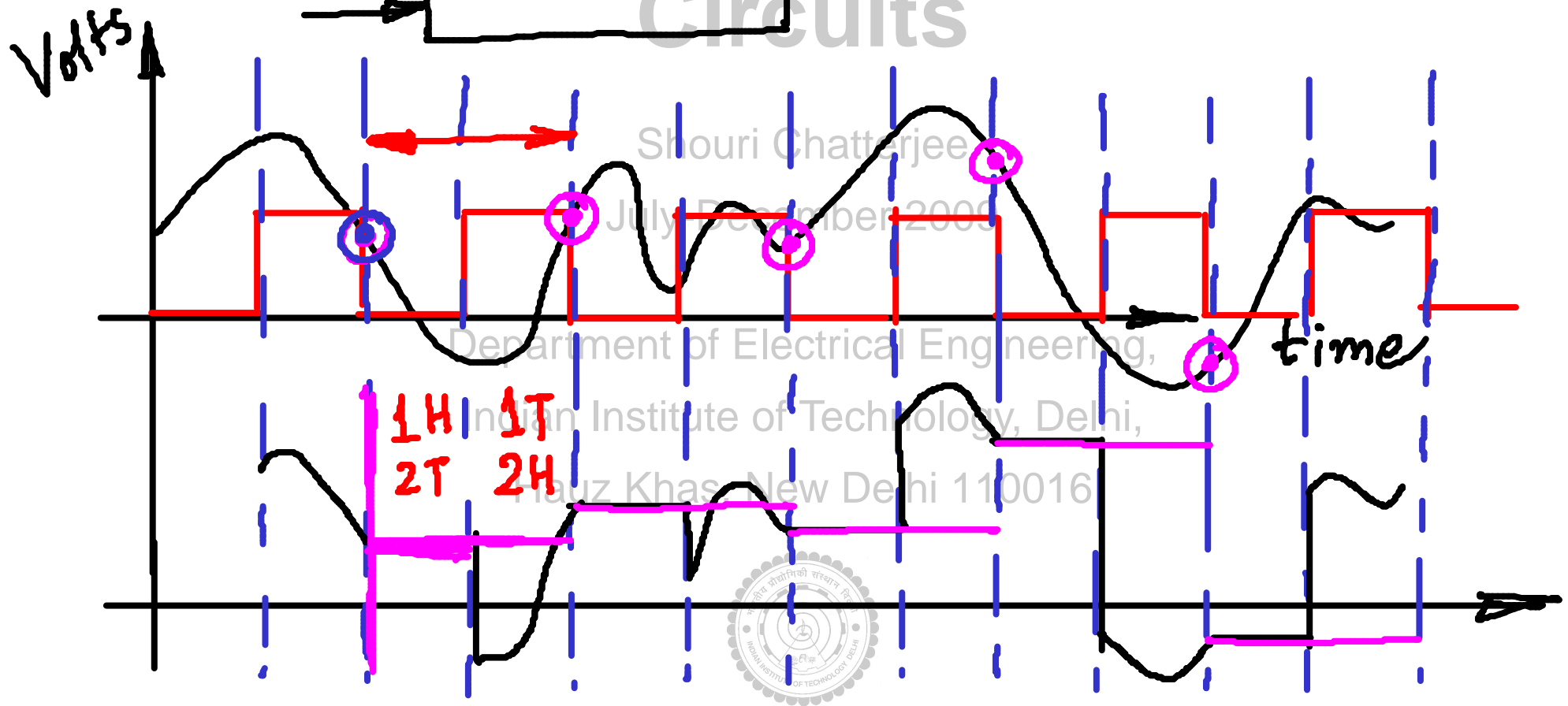
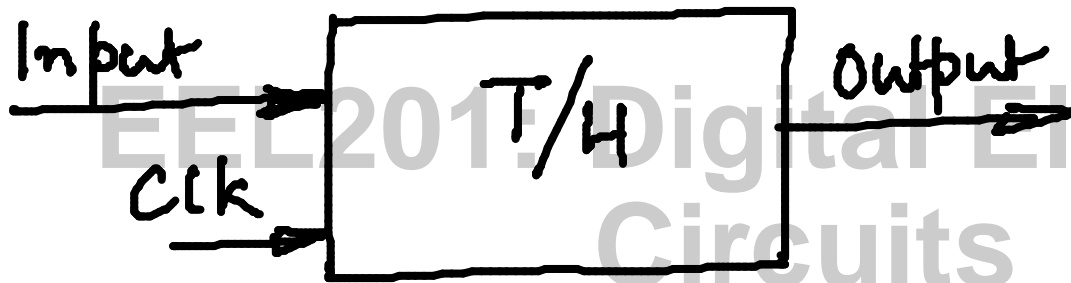
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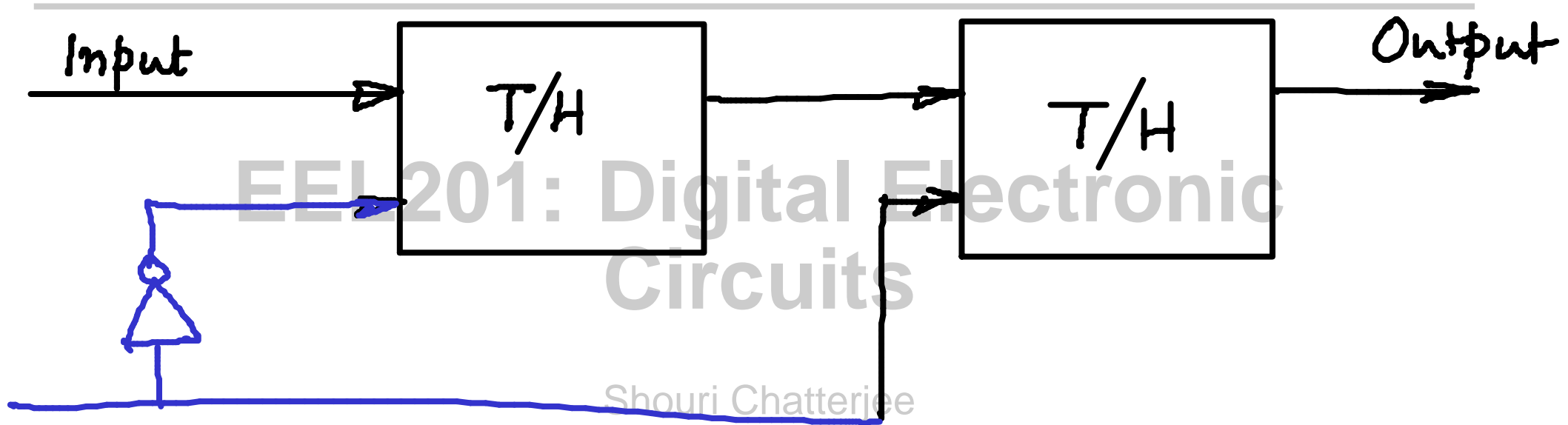
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# Track-and-Hold



# Sample and Hold



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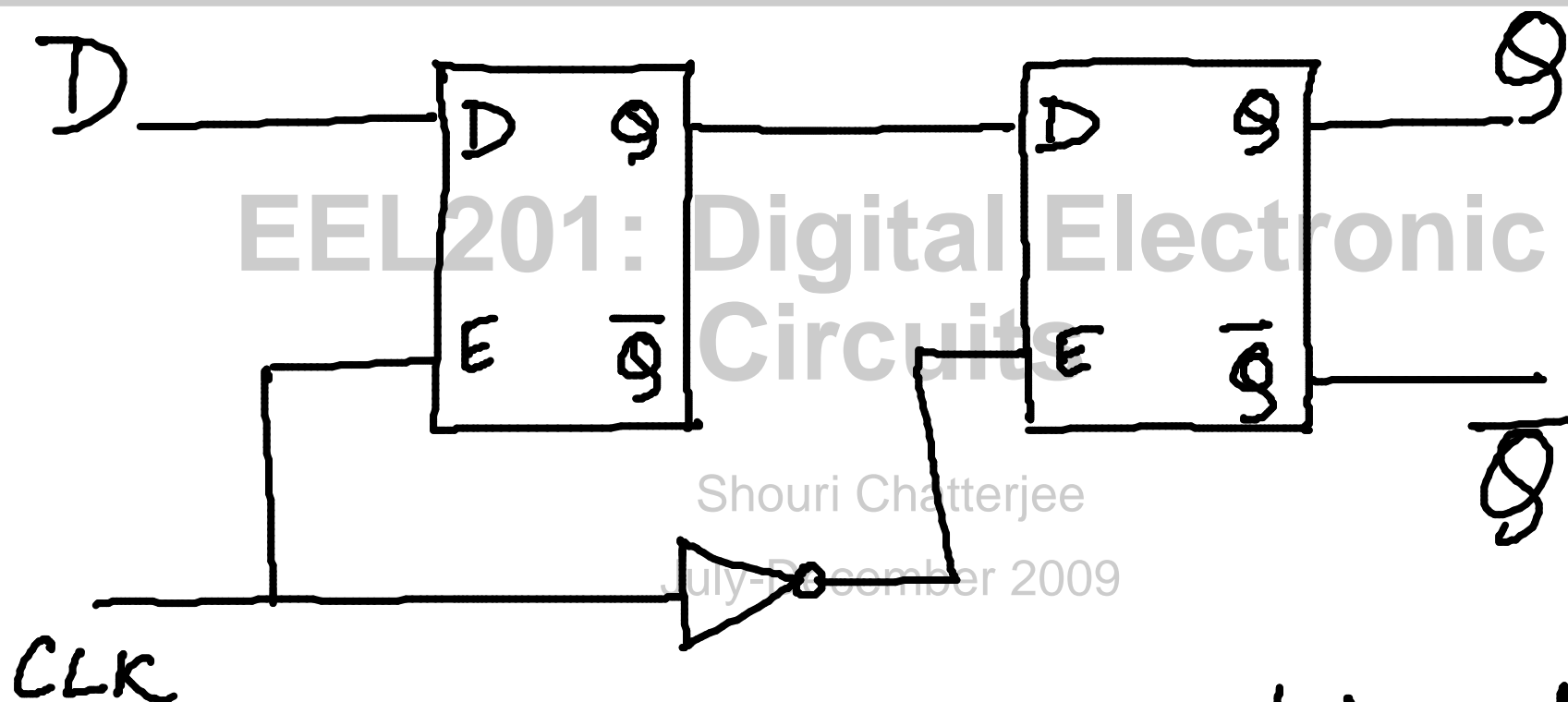
Rising edge

Falling edge

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# Master-Slave



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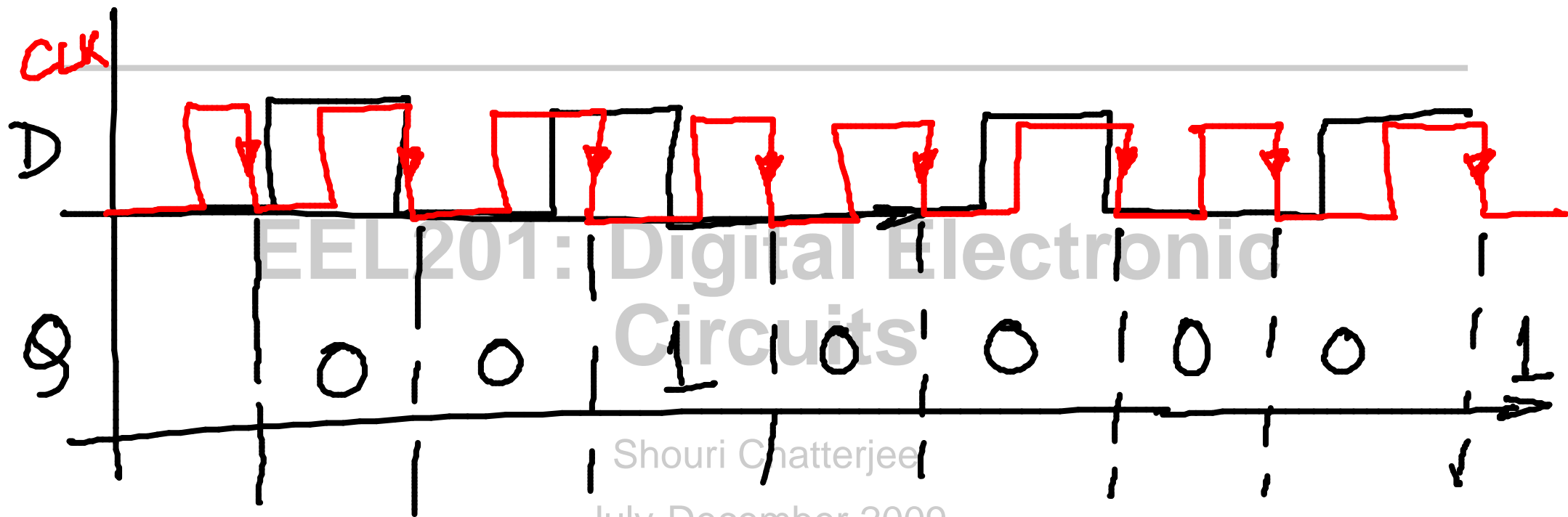
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Falling Edge triggered flip-flop  
Rising

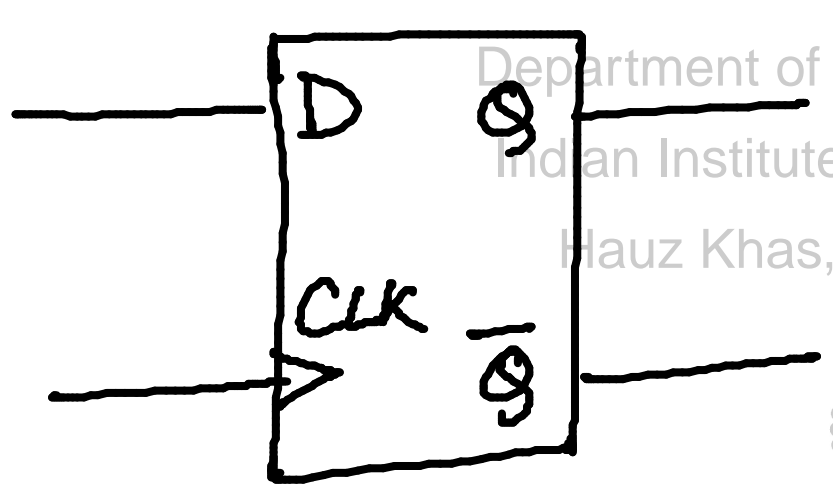




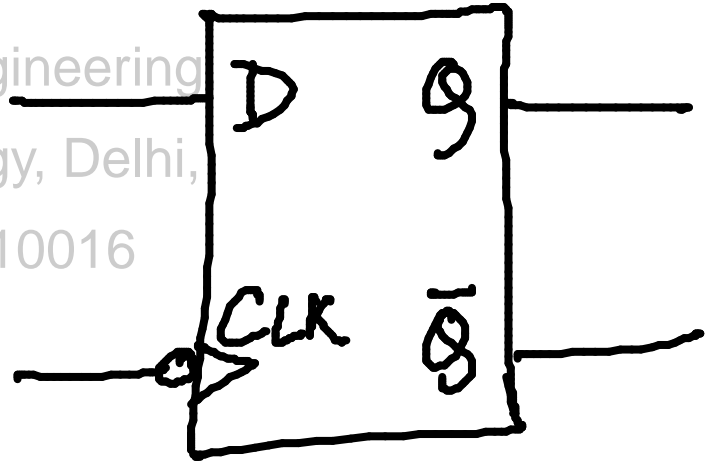
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rising edge



falling edge