Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Minor 1, 3rd September, 2008

Instructions: Read the questions carefully. Answer all of them.

1. The state of an 8-bit register is 11011011. What does it represent if the binary number was (a) unsigned (b) in sign-magnitude notation (c) in 2's complement notation (d) in 1's complement notation (e) in offset binary notation?
   (5×1 marks)

2. Consider the two functions

$$f_1(A, B, C, D) = \Pi(1, 3, 5, 11, 15)$$

$$f_2(A, B, C, D) = \Pi(1, 3, 5, 7, 8, 9, 11)$$

   Express $f_3 = f_1 + f_2$ as a product of max-terms. (3 marks)
   Minimize the function $f_4 = f_1 \cdot f_2$ using a Karnaugh map. (3 marks)
   How will you generate f_4 using an 8-1 MUX? (3 marks)

3. Two decimal numbers, both between 0 and 99, need to be added to each other. Design a logic circuit that performs a BCD addition of these two numbers. Use block diagrams for adders and other components that you need, use any combinational logic gates that you require. (4 marks)

4. Consider a 4-bit ripple carry adder. Each full-adder is implemented using a 3-input XOR gate, three 2-input AND gates, and one 3-input OR gate.
   (a) Draw the circuit diagram for the full-adder. (1 mark)
   (b) Consider the delay of each 3-input XOR gate to be 3 nsec, the delay of each 2-input AND gate to be 1 nsec, and the delay of each 3-input OR gate to be 1 nsec. What will be the total time taken by the 4-bit ripple carry adder to perform a successful addition operation? (2 marks)
   (c) Suppose the two numbers to be added are $(F)_{16}$ and $(1)_{16}$. Evaluate the sum as a function of time, starting from the beginning of the addition, at every nano-second. Assume that the sum was $(0)_{16}$ before the addition started. (4 marks)