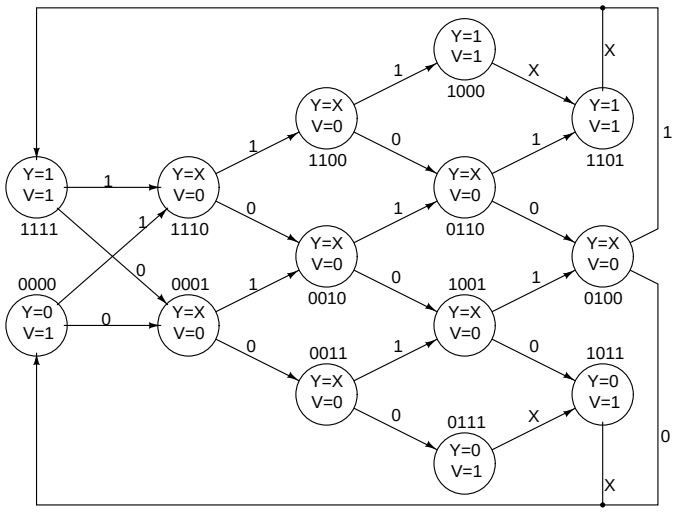
Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Minor 2, 19th October, 2008

Instructions: Answer all of them sequentially.

1. Construct a set-reset latch using only NOR gates. Write out its truth table. (3 marks)

2. Consider an error correction scheme that can CORRECT for 2-bit errors, in addition to 1-bit errors. For every valid 5-bit word, how many invalid words can occur? Then, how many valid words are possible? Can you come up with a coding scheme for the check bits? (2+1+3 marks)

3. Consider the Moore machine represented by the state diagram shown in the figure. The Moore machine always starts from the state 0000, using an asynchronous start mechanism. The input stream is R, the outputs are V and Y. The outputs are as indicated within the states. For invalid states, assume Y=X, V=0, and the next state is 0000.



   (a) If the input sequence, R, is 110110000011001111010, what are the outputs V and Y? (3 marks)

   (b) Assume the number of states has already been reduced. The machine needs to be designed using D-flip-flops. Write out the state table, and express $D_3D_2D_1D_0$ as functions of $Q_3Q_2Q_1Q_0R$ in the sum-of-products form. (No minimization required.) Use K-maps to minimize the expressions for Y and V. (3+4+4 marks)

   (c) What do you think this state machine does? (2 marks)