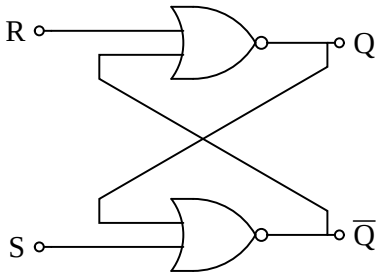
Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Solutions to Minor 1 Exam, 3rd September, 2008

1.



S	R	Q	$\overline{Q}$	
0	0	q	$\overline{q}$	Hold State
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Invalid State

2. 5-bit word. For every valid word, 2-bit errors cause ${}^5C_2$ invalid words. For every valid word, 1-bit errors cause ${}^5C_1$ invalid words. In total, for every valid word, there are ${}^5C_2 + {}^5C_1 = 15$ invalid words. That means, the number of valid words are:

$$\frac{2^5}{{}^5C_2 + {}^5C_1 + 1} = 2$$

There are only 2 possible words. This means that, really, there is only 1 bit of information. The rest are all "check" bits. The simplest coding scheme that one can think of is a "majority". The two valid words are "00000" and "11111", when the information bit is "0" and "1" respectively. With a maximum of two errors, the decoder will now have to find out the majority.

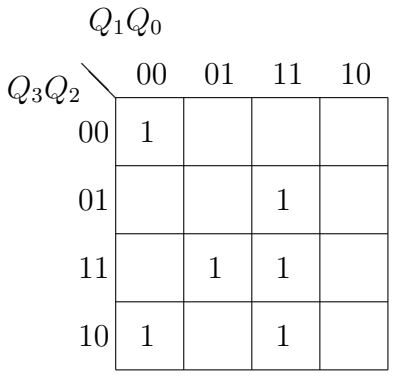
3. (a)

R	11011	00000	11001	11101	0
V	100011	00111	00001	00111	0
Y	0xxx11	xx000	xxxx1	xx111	x

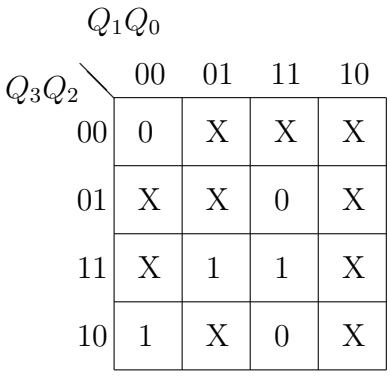
(b)

$Q_3Q_2Q_1Q_0R$	D_3	D_2	D_1	D_0
0	0	0	0	1
1	1	1	1	0
2	0	0	1	1
3	0	0	1	0
4	1	0	0	1
5	0	1	1	0
6	0	1	1	1
7	1	0	0	1
8	0	0	0	0
9	1	1	1	1
10	0	0	0	0
11	0	0	0	0
12	0	1	0	0
13	1	1	0	1
14	1	0	1	1
15	1	0	1	1
16	1	1	0	1
17	1	1	0	1
18	1	0	1	1
19	0	1	0	0
20	0	0	0	0
21	0	0	0	0
22	0	0	0	0
23	0	0	0	0
24	0	1	1	0
25	1	0	0	0
26	1	1	1	1
27	1	1	1	1
28	0	0	1	0
29	1	1	0	0
30	0	0	0	1
31	1	1	1	0

$$
\begin{aligned}
D_3 &= \Sigma 1, 4, 7, 9, 13, 14, 15, 16, 17, 18, 25, 26, 27, 29, 31 \\
D_2 &= \Sigma 1, 5, 6, 9, 12, 13, 16, 17, 19, 24, 26, 27, 29, 31 \\
D_1 &= \Sigma 1, 2, 3, 5, 6, 9, 14, 15, 18, 24, 26, 27, 28, 31 \\
D_0 &= \Sigma 0, 2, 4, 6, 7, 9, 13, 14, 15, 16, 17, 18, 26, 27, 30
\end{aligned}
$$



V



Y

$$V = Q_2Q_1Q_0 + Q_3Q_1Q_0 + Q_3Q_2Q_1 + \overline{Q_2}\ \overline{Q_1}\ \overline{Q_0}$$

$$Y = Q_3\overline{Q_1} + Q_3Q_2$$

(c) This state machine detects the majority of the last five input bits in X, starting from the idle state.