Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Quiz, 19th November, 2008

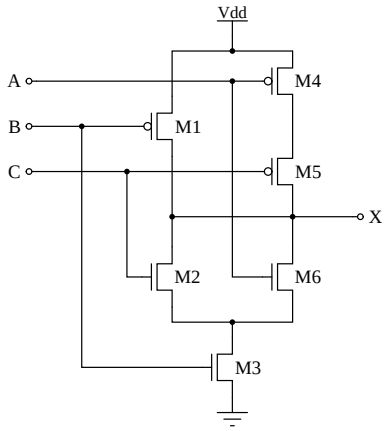
Each question or fill-in-the-blank carries 1 mark. A wrong answer will warrant -0.3 marks. Total is 20.

A. Consider the following piece of Verilog code:

```
module quiz (output myoutput1, output myoutput2, input myinput1,
input myinput2, input clk);
reg myoutput1;
reg [2:0] myoutput2;
reg [3:0] current_state, next_state;
reg internal_var1, internal_var2;

always @(posedge clk)
        current_state <= next_state;

always @(myinput1, current_state)
begin
        if(myinput1 == 1) next_state <= current_state + 1;
        else next_state <= current_state - 1;
        myoutput1 <= ~current_state[3];
end

always @(myinput2, current_state)
        if(myinput2 == 1) internal_var1 <= current_state[1];
        else internal_var1 <= current_state[0];

assign internal_var2 = current_state[3] & myinput1;

always @(internal_var1, myinput1, current_state)
        if(internal_var1) myoutput2 <= 3'b001;
        else if (current_state == 3'b010) myoutput2 <= 3'b110;

endmodule
```

1. The number of edge-triggered flip-flops that will be synthesized in the above code are _____.
2. The data-types of `myinput1` and `myinput2` are _____ and _____ respectively.
3. The number of level sensitive flip-flops that will be inferred from the code is _____. (Excluding the edge-triggered flip-flops).
4. `myoutput1` is a _____ type output.
5. The combinational logic described in the third `always` statement can also be described in which of the following ways?
   (a) `internal_var1 = current_state[1] & myinput2`
   (b) `internal_var1 = current_state[0] & ~myinput2`
   (c) `internal_var1 = (a) + (b)`
   (d) `internal_var1 = ~((a) & (b))`
6. The output `myoutput1` should be declared as a `wire`, and not as a `reg`. (True/False?)
7. `internal_var2` should be declared as a `wire`, and not as a `reg`. (True/False?)

B. Consider the following circuit diagram:



8. If A=1, B=0, C=0, the device M1 is _____, the device M2 is _____, the device M3 is _____. (On/Off?)
9. If A=1, B=1, C=0, the device M1 is _____, the device M2 is _____, the device M3 is _____. (On/Off?)
10. The circuit implements the function:
    (a) $X = \overline{(A+B)C}$
    (b) $X = \overline{(A+C)B}$
    (c) $X = \overline{AC+B}$
    (d) $X = (\overline{A}+\overline{C})\overline{B}$

C. Answer the following questions:

11. A PLD contains:
    (a) Programmable OR gates
    (b) Programmable AND gates
    (c) Programmable XOR gates
    (d) (a), (b) and (c)
12. In addition to all the gates and flip-flops available in a CPLD, an FPGA will also contain _____.
13. In a particular FPGA, the set-up and hold times of all the flip-flops are 10 pico-seconds, and 20 pico-seconds respectively. In my design, the total worst case gate-delay of all the combinational logic between the "Q" outputs of the flip-flops, and the "D" inputs of the flip-flops is 170 pico-seconds. The maximum clock frequency that I can possibly use is _____ Hz.
14. I am designing an integrated circuit with several edge-triggered flip-flops, all timed by the same 3 GHz clock. The maximum phase difference, between the clocks of two edge-triggered flip-flops, that I can tolerate is 45^0. Assume that the signals travel at the speed of light (in vacuum = 3×10^8 m/s). The maximum length of the wire used for the clock signal is _____.
15. For TTL (transistor-transistor-logic), a BJT (bipolar-junction transistor) can be viewed as a _____–controlled switch.