Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Solutions to the Quiz, 19th November, 2008

1. The number of edge-triggered flip-flops that will be synthesized in the above code are 4.
2. The data-types of `myinput1` and `myinput2` are wire and wire respectively.
3. The number of level sensitive flip-flops that will be inferred from the code is 3. (Excluding the edge-triggered flip-flops).
4. `myoutput1` is a Moore type output.
5. (c)
6. FALSE
7. TRUE
8. If A=1, B=0, C=0, the device M1 is ON, the device M2 is OFF, the device M3 is OFF.
9. If A=1, B=1, C=0, the device M1 is OFF, the device M2 is OFF, the device M3 is ON.
10. (b)
11. (a) and (b). It is okay to mark (d).
12. In addition to all the gates and flip-flops available in a CPLD, an FPGA will also contain Look-up tables.
13. In a particular FPGA, the set-up and hold times of all the flip-flops are 10 pico-seconds, and 20 pico-seconds respectively. In my design, the total worst case gate-delay of all the combinational logic between the "Q" outputs of the flip-flops, and the "D" inputs of the flip-flops is 170 pico-seconds. The maximum clock frequency that I can possibly use is 5 G Hz.
14. I am designing an integrated circuit with several edge-triggered flip-flops, all timed by the same 3 GHz clock. The maximum phase difference, between the clocks of two edge-triggered flip-flops, that I can tolerate is 45^0. Assume that the signals travel at the speed of light (in vacuum = 3×10^8 m/s). The maximum length of the wire used for the clock signal is 12.5 mm.
15. For TTL (transistor-transistor-logic), a BJT (bipolar-junction transistor) can be viewed as a current– controlled switch.