Indian Institute of Technology, Delhi
EEL 201: Digital Electronic Circuits
Tutorial 5, 31st August, 2009

1. For the S-R latch, assume each NAND gate has a delay of 1 nsec. The inputs to the S-R latch are applied as follows. At every 1 nsec, the value at $\overline{\text{S}}$ is given by 0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1. At every 1 nsec, the value at $\overline{\text{R}}$ is given by 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1. Find out the waveform at the outputs, Q, $\overline{Q}$ as functions of time. What is the "hold time" of this latch? (Here "hold time" is the minimum pulse-width at the input for a reasonable output.)

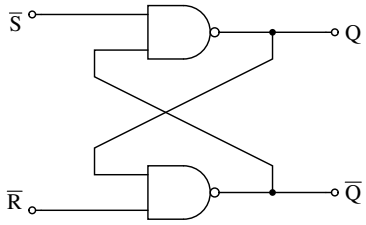

Figure 1: Set-reset latch

2. Now assume that the top NAND gate has a delay of 1 nsec, while the bottom NAND gate has a delay of 2 nsec. Rework the above problem.

3. Assume that the delay of each NAND gate is 1 nsec, the delay of each NOT gate is 0.5 nsec. Compute the "setup time" of the D-latch. (Here "setup time" is the minimum time for which the input has to be constant before the clock becomes inactive.)

4. Compute the "setup time" and the "hold time" of a falling-edge-triggered master-slave D-flip-flop. (Assume NAND gates have a delay of 1 nsec, NOT gates have a delay of 0.5 nsec.)

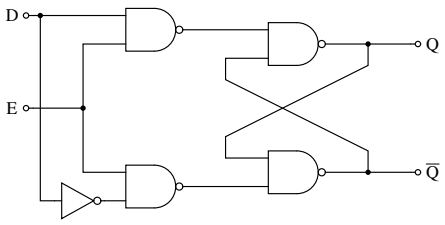

Figure 2: D-latch