Indian Institute of Technology, Delhi
EEL 204: Analog Electronic Circuits
Tutorial 5, March 6, 2011

For the nMOSFETS, assume the following I_D characteristics:

$$I_D = K(V_{GS} - V_T)^2$$

where K is 16 mS/V, and the V_T of the device is 0.5 V. The MOSFET remains in saturation as long as $V_{DS} > V_{GS} - V_T$. Adapt these characteristics for pMOS devices as well. K for pMOS devices is 8 mS/V. Assume r_{ds} is such that $g_m r_{ds}$ of any given MOS device is 20.

For the BJTs, β is 100, η is 1. Assume r_o of each BJT is 50 kΩ.

All nodes labelled "A" are connected, all nodes labelled "B" are connected, etc.

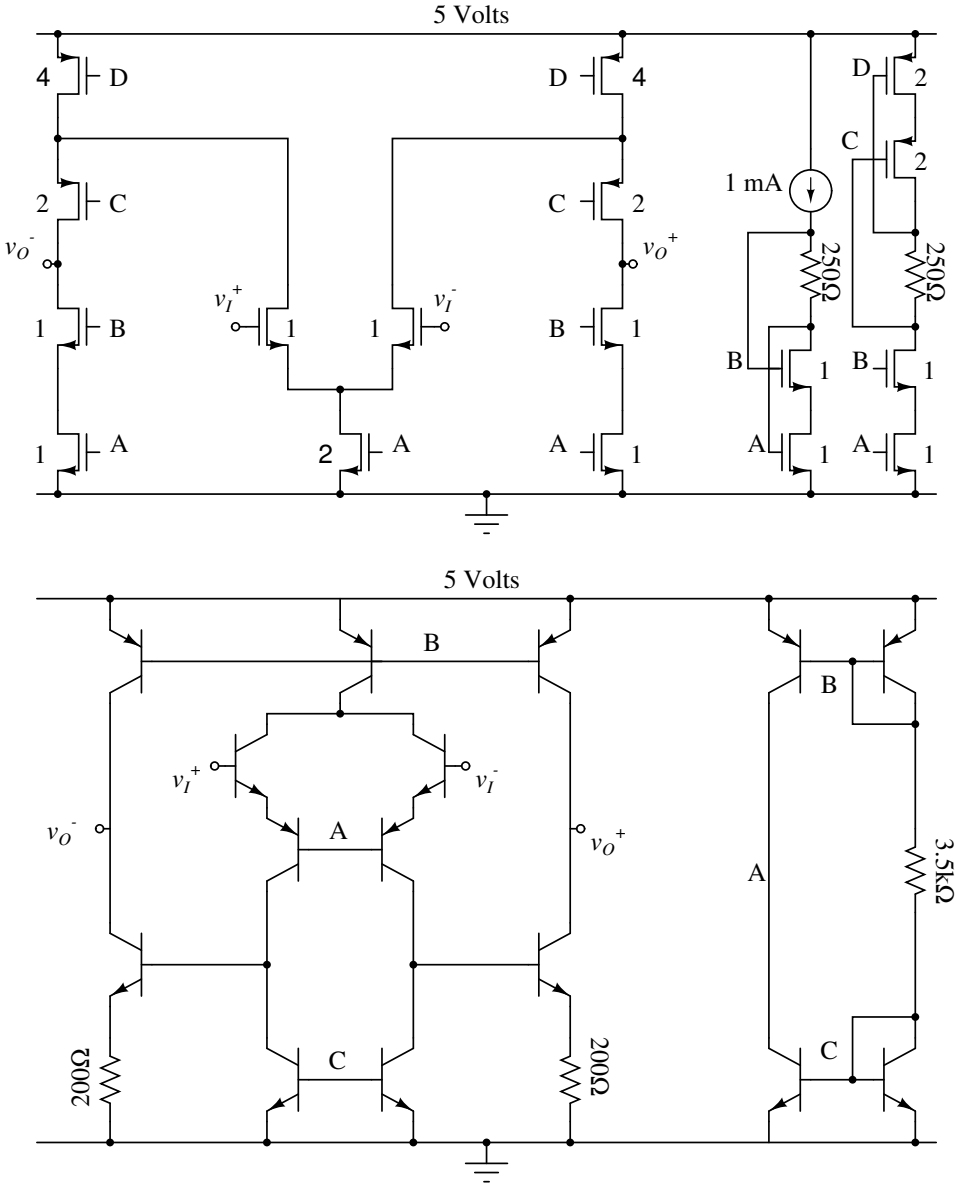
Find the following for each of the structures:

1. Bias conditions: currents through every branch and voltages at every node. If you cannot find the voltage at a node, assume it is at the middle of its maximum and minimum limits.

2. Draw the differential mode half circuit (if any) and the common mode half circuit (if any).

3. Find the differential mode and common mode gains.

4. If v_I^+ is 2.5 Volts + 10 mV $\cos \omega t$, and v_I^- is 1.5 Volts - 2 mV $\cos \omega t$, find out v_O^+ and v_O^-. Assume ω is small enough that all parasitic capacitances can be treated as open circuits.


5 Volts
4 D
2 C
1 B
1 A
v_O^-
v_I^+
v_I^-
1
1
2 A
D 4
C 2
B 1
A 1
v_O^+
1 mA
D 2
C 2
250Ω
250Ω
B 1
A 1
B 1
A 1
5 Volts
B
v_I^+
v_I^-
v_O^-
A
v_O^+
200Ω
C
250Ω
B
A
3.5kΩ
C