Indian Institute of Technology, Delhi
EEL 204: Analog Electronic Circuits
Tutorial 6, March 15, 2011

For the nMOSFETS, assume the following I_D characteristics:

$$I_D = K(V_{GS} - V_T)^2$$

where K is 16 mS/V, and the V_T of the device is 0.5 V. The MOSFET remains in saturation as long as $V_{DS} > V_{GS} - V_T$. Adapt these characteristics for pMOS devices as well. K for pMOS devices is 8 mS/V. Assume r_{ds} is such that $g_m r_{ds}$ of any given MOS device is 20.

All nodes labelled "A" are connected, all nodes labelled "B" are connected, etc.

Find the following:

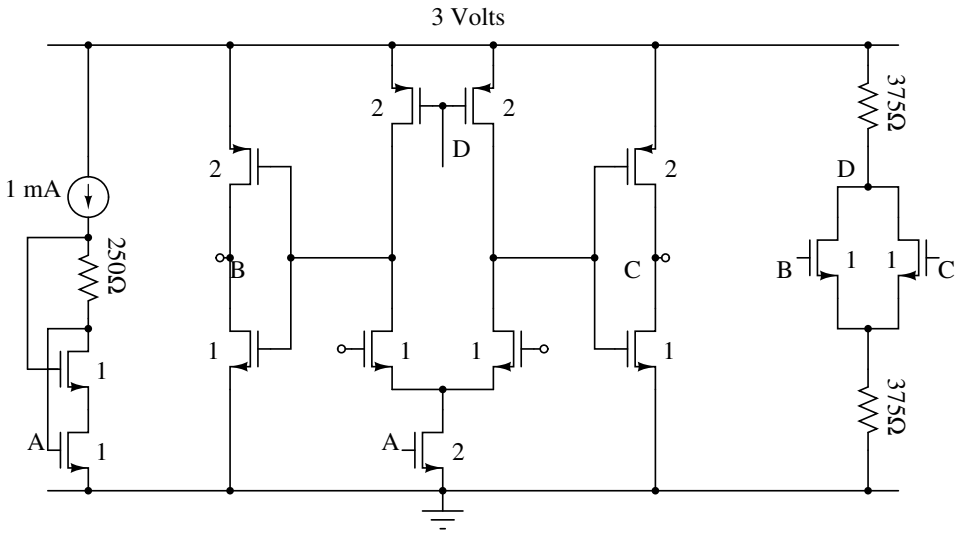
1. Begin by evaluating the bias conditions, and by evaluating g_m, r_{ds} of the different devices (if you can find them).

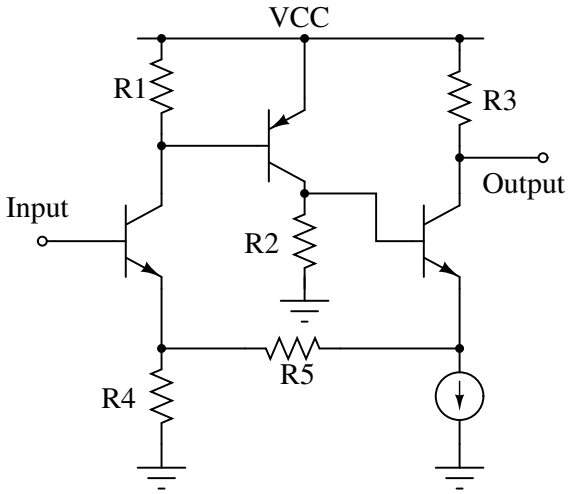
2. Find the differential mode and common mode gains with the connection labelled as 'D' not present. Assume any suitable constant voltage for the gates of the pMOS devices.

3. Find the differential mode and common mode gain with the connection labelled as 'D' present. What kind of feedback topology is this?

For the BJT circuit, assume all devices have β of 100. The biasing details of the circuit are not shown. Assume the three devices, starting from the input side to the output side, are biased at 1 mA, 2 mA, 3 mA.

What kind of feedback is being used? What is the approximate voltage gain in terms of resistor values? Solve the circuit using the classical two port parameters, as well as, using the loop gain technique.


3 Volts
1 mA
250Ω
2
2
D
2
2
375Ω
D
B
C
B
1
1
C
1
1
1
1
1
A
1
A
2
375Ω


VCC
R1
R3
Output
Input
R2
R5
R4