To reduce input ref noise of an OTA

1) Increase gain of stage 1

→ 2) De-coupling caps for bias points

(3) Increase g_m of i/p devices → increase tail current

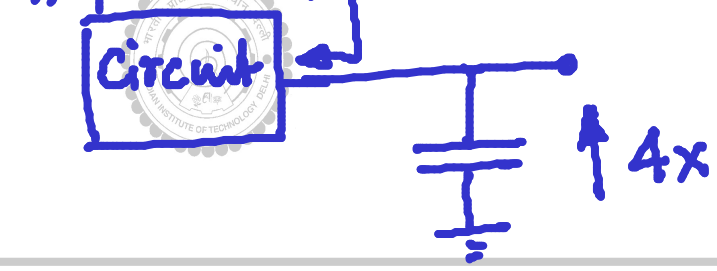
→ 4) Improve matching → larger devices W and L

Decrease mean sq input refd noise 2×

⇒ Increase g_{m_1} 2× $g_m = \sqrt{2 I \mu C_{ox} \frac{W}{L}}$

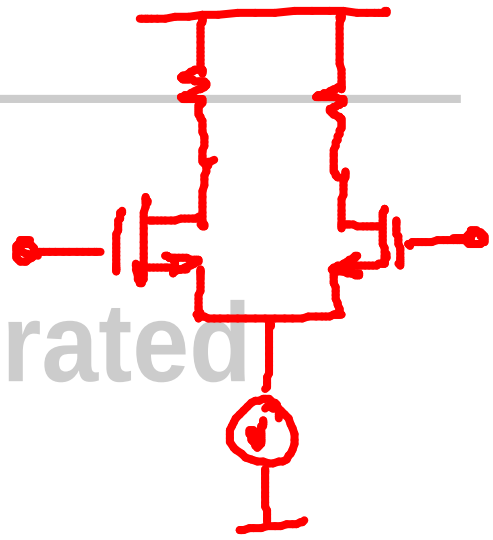
2× area, 2× current

4× power R/4



$\sqrt{\frac{kT}{C}}$

Flicker or 1/f noise



→ reduce 1/f noise by increasing area.

root mean sq noise voltage ↓ 2x

area ↑ 4x

Clock jitter