

To reduce input ref noise of an OTA

- 1) Increase gain of stage 1
- 2) De-coupling caps for bias points
- ③ Increase  $g_m$  of i/p devices → increase tail current
- 4) Improve matching → larger devices  
W and L

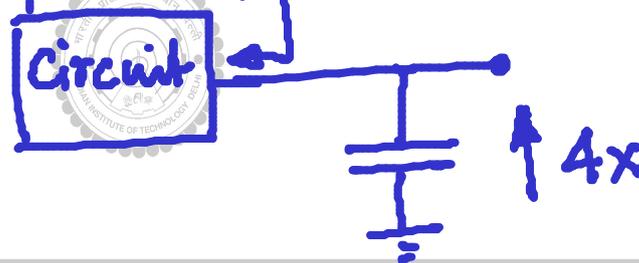
Decrease mean sq input refd noise  $2x$

⇒ Increase  $g_m$ ,  $2x$   $g_m = \sqrt{2I\mu C_{ox} \frac{W}{L}}$

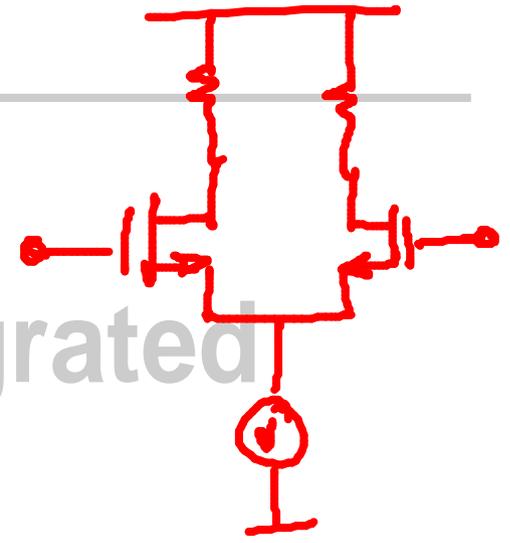
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4x power  $R/4$  2x area, 2x current

$$\sqrt{\frac{kT}{C}}$$



# Flicker or $1/f$ noise



EEL782: Analog Integrated Circuits

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→ reduce  $1/f$  noise by increasing area.  
root mean sq noise voltage  $\downarrow 2x$  area  $\uparrow 4x$

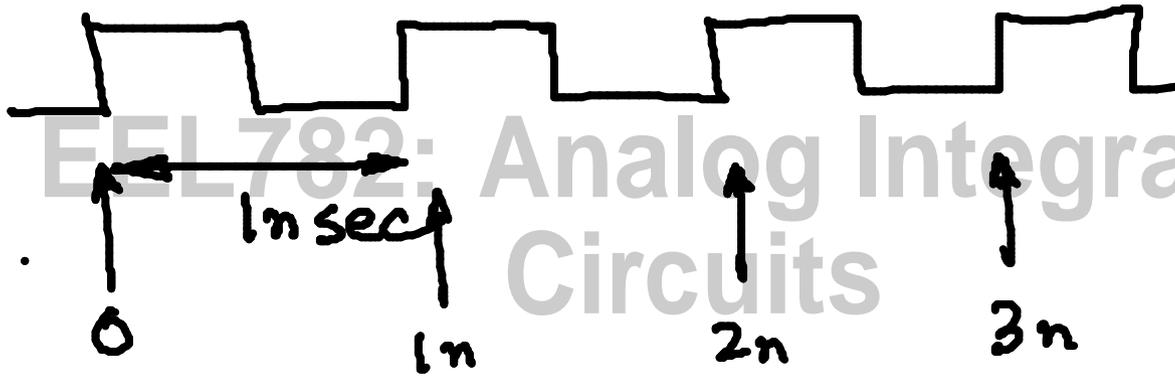
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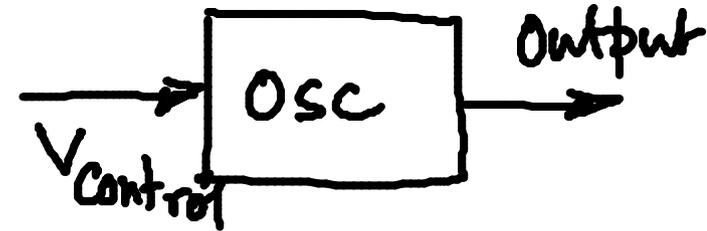
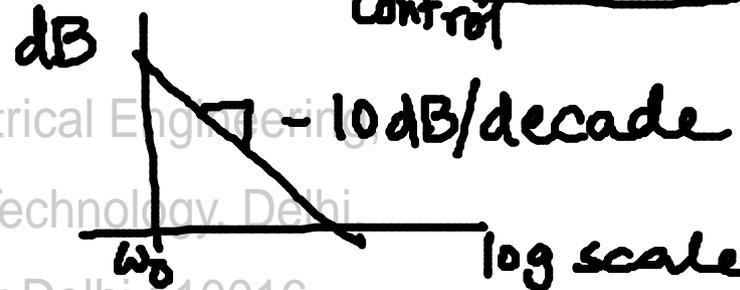
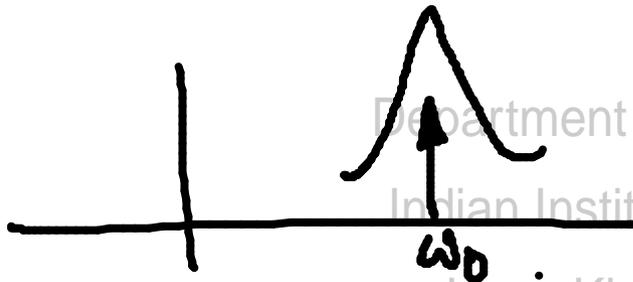


# Clock jitter

1 GHz



$$\cos(\omega_0 t + \phi)$$



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