

Indian Institute of Technology, Delhi
EEL782: Analog Integrated Circuits
Minor 2, March 20, 2009
(Continuation of Minor 1)

Answer all the questions. Full marks is 40. Good luck!

Consider the following circuit diagram. All nMOS and pMOS devices in the circuit are in weak inversion and follow the device equation given by:

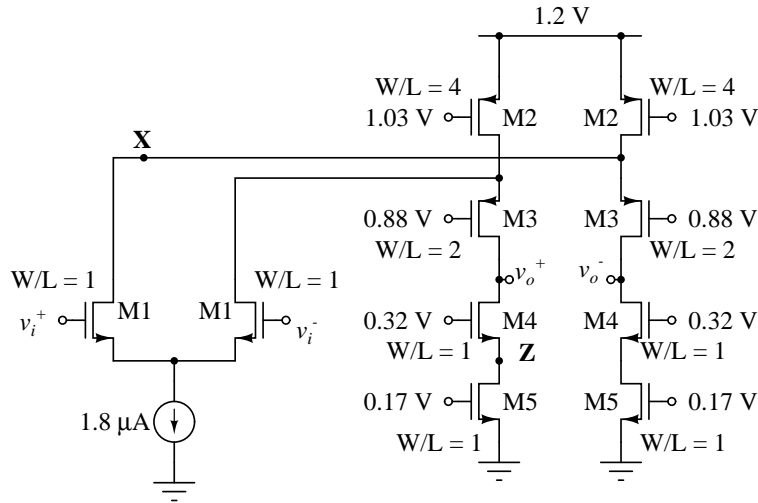
$$I_{DS} = I_0 \exp\left(\frac{|V_{GS}|}{\zeta v_T}\right) \left(1 - \exp\left(-\frac{|V_{DS}|}{\eta v_T}\right)\right)$$

$v_T = kT/q = 25$ mV at 300 K, $\zeta = 1$, $\eta = 2$. For nMOS devices $I_0 = W/L \cdot 1$ nA, and for pMOS devices $I_0 = W/L \cdot 0.5$ nA. Assume g_{mb} of all devices is equal to 0 S. Assume the nominal quiescent voltage at v_o^+ and v_o^- to be 0.6 V. Also assume that the sources of the input devices marked as M1 are at 0.6 V.

Under weak inversion, $C_{GS} = C_{GD} = 1/2 \cdot C_{ox}$, where C_{ox} is the oxide capacitance. The oxide capacitance is given by $W \cdot L \cdot C'_{ox}$. Assume C'_{ox} to be 8 fF/sq. μm . Assume all other capacitances to be zero. The mean square thermal noise current between the drain-source is given by $2qI$, where I is the current through the device, and q is the charge of an electron, i.e., 1.6×10^{-19} Coulombs.

Use the following table for essential parameters.

Device	g_m [μS]	r_{ds} [$\text{M}\Omega$]	V_{GS} [V]	V_{DS} [V]	W [μm]	L [μm]
M1	36	10	0.17	0.45	1	1
M2	72	0.6	-0.17	-0.15	4	1
M3	36	10	-0.17	-0.45	2	1
M4	36	10	0.17	0.45	1	1
M5	36	1.2	0.17	0.15	1	1



1. Draw the small signal differential mode half circuit. (3 marks)
2. Find the pole frequencies contributed by the output node, node X and node Z. Assume that the circuit is driving a load capacitance of 1 pF. (4 + 4 + 4 marks)
3. Is there any zero in the design? Compute the frequency of the zero. (1 + 4 marks)
4. Estimate the input referred noise contribution of each of the individual devices: M1, M2, M3, M4 and M5. Find the total input referred noise for the differential half circuit. (mean-square noise voltage per unit frequency) (3×5+2 marks)
5. If the maximum allowable signal at the input is of a 0.1 Volt amplitude, what is your assessment of the design? (3 marks)