

Indian Institute of Technology, Delhi
EEP 201: Digital Electronic Circuits Laboratory
Experiment 3, July-Dec 2008
Exercise with Adders

Pre-lab exercises:

1. Read the material in full.
2. Evaluate the truth table for a half-adder.
3. Evaluate the truth table for a full-adder.

Experiment:

- A half-adder has two inputs, A and B. There are two outputs - the sum, S, and the carry, C. $S = \text{XOR}(A, B)$. $C = AB$.

Implement a half-adder circuit using the schematic entry tools. Simulate and verify that the half-adder is functioning properly.

- A full-adder has three inputs, A, B and the carry-in, Cin. There are two outputs - the sum, S, and the carry-out, Cout. $S = \text{XOR}(\text{XOR}(A, B), C)$. $\text{Cout} = AB + \text{BCin} + \text{ACin}$.

Implement a full-adder circuit using the schematic entry tools. Simulate and verify that the full-adder is fully functional.

- Arrange four full-adders as shown in the figure. This is a binary 4-bit adder. Implement the 4-bit adder using the schematic entry software. Simulate and verify that the 4-bit adder is working. Set the two 4-bit inputs of the adder to 0111 and 1011 respectively. Explain the observed output.

