Indian Institute of Technology, Delhi
EEP 201: Digital Electronic Circuits Laboratory
Experiment 5, July-Dec 2008
Latches and Flip-Flops

- Connect the circuit as shown in Fig. 1. Simulate the circuit when the two inputs (J and K) are sequentially 00, 01, 10, 11, 11, 10, 01, 00 over time, for every period of the clock CLK. This circuit is known as a level-sensitive J-K flip-flop.

- Connect two level-sensitive J-K flip-flops one after the other, with the CLK as shown in Fig. 2. Simulate its performance and identify its truth table. The first flip-flop is called a master, the second is called a slave, and the combination is known as a master-slave J-K flip-flop.

- An alternate approach is shown in Fig. 3. The CLK signal is activated only for a brief period of time. This approach is known as an edge-triggered J-K flip-flop. Simulate its performance. Is there any difference in the truth table, from that of the master-slave J-K flip-flop?

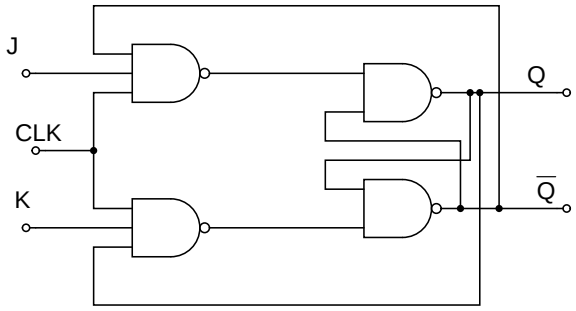

Figure 1:

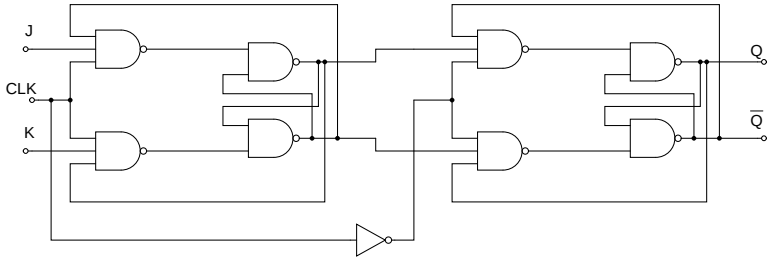

Figure 2:

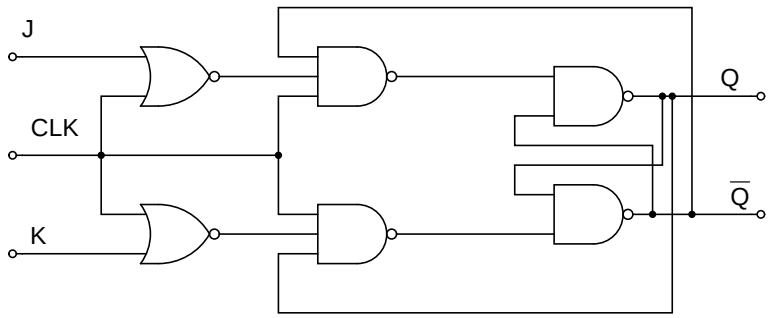

Figure 3: