Indian Institute of Technology, Delhi
EEP 201: Digital Electronic Circuits Laboratory
Experiment 7, July-Dec 2008
Shift Registers

Serial data is fed one bit at a time over only one wire at a constant rate, in phase with a clock reference. Parallel data, on the other hand, has one line or wire for each bit in the binary word and does not have to be referred to a clock. The frequency of the reference clock for serial data transfer is usually called the Baud rate of the serial transfer.

Parallel data transmission is much faster, even though serial data transfer is used more often. Why? Find out where it is convenient to use parallel data transfer, and where serial data transfer would be preferred.

A parallel-in, serial-out shift register is shown in Fig. 1. To build this, first simulate the master-slave edge-triggered D-flip-flop shown in Fig. 2.

To operate the parallel-load, serial-out shift register, first apply the data that you would like to load onto your 8-bit input. Next, set the signal "LOAD" to 1. After the data is loaded into the flip-flops, reset the "LOAD" signal to 0. Now apply the clock periodically to the inputs of the D-flip-flops, and watch the output coming one bit at a time, synchronous to the clock.

Build two versions of the parallel-load, serial-out shift register. The first version should use the master-slave D-flip-flops designed by you. The second version should use D-flip-flops from the library.

If the clock frequency is 5 MHz, what should be the data-rate at the parallel-load input?

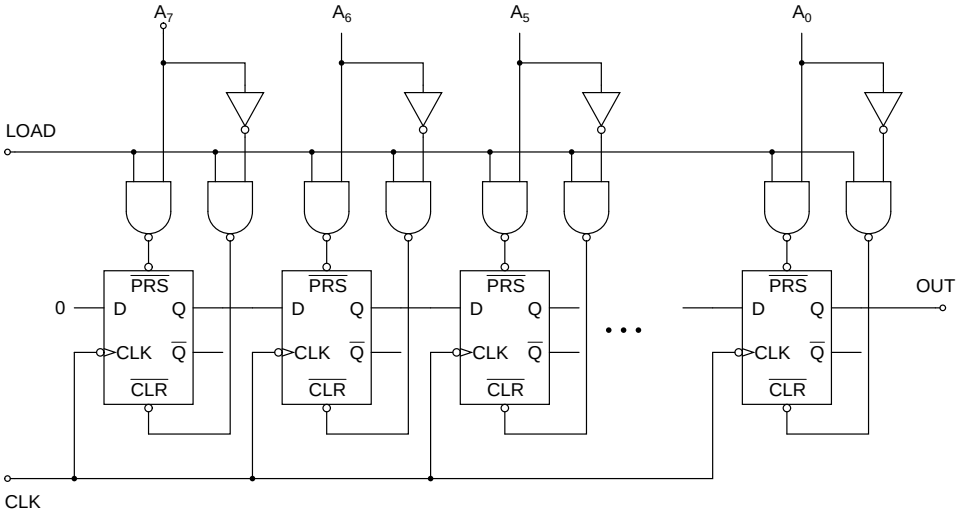

Figure 1:

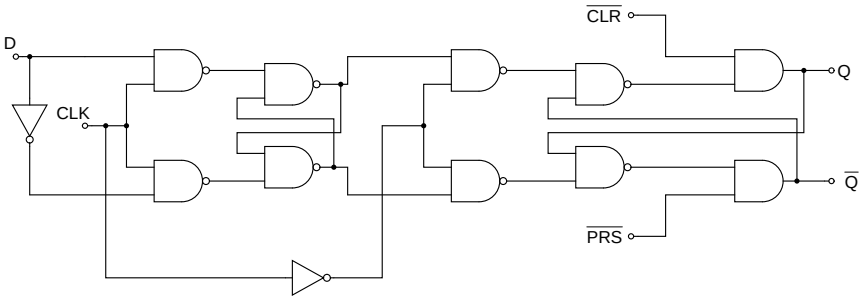

Figure 2: