Indian Institute of Technology, Delhi
EEP 201: Digital Electronic Circuits Laboratory
Experiment 8, July-Dec 2008
Sequence Generator

Design a sequence generator that generates the following sequence: {1, 1, 0, 1, 1, 0}.

Design steps:

- The circuit has one input, X, and one serial output, Y. If X is 1 at the rising clock edge, the machine should generate the desired output sequence as Y. If X is 1 while the circuit is busy generating its output sequence, the input X should be ignored. If X is 0, and the circuit is idle, the output Y should be 0.
- Construct a state diagram for the finite state machine. Consult the instructor or the TAs after you design the state diagram.
- How many flip-flops will you need?
- Assign values to each state in the state diagram.
- Construct the state table from the state diagram. Use D-flip-flops.
- Use Karnaugh maps to generate each of the inputs to each of the flip-flops.
- Use 74LS74 D-flip-flops, and only 74LS00 NAND gates to wire up your circuitry. Use a debouncer circuit to generate the clock.