Indian Institute of Technology, Delhi
EEP 201: Digital Electronic Circuits Laboratory
Experiment 9, July-Dec 2008
Sequence Detector

Design a sequence detector that detects the sequence {1, 1, 0, 1, 1, 0}.
Design steps:

- The circuit has one serial input, X, and one output, Y.
- Construct a state diagram for the finite state machine. Consult the instructor or the TAs after you design the state diagram.
- How many flip-flops will you need?
- Assign values to each state in the state diagram.
- Construct the state table from the state diagram. Use D-flip-flops.
- Use Karnaugh maps to generate each of the inputs to each of the flip-flops.
- Use D-flip-flops from the library, and only NAND gates to wire up your circuitry.
- Test your circuit using the following input data stream for X: {0, 0, 0, 0, 0, 0, 1, 0, 0, 1, 0, 1, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 0, 1, 1, 0, 0, 1, 0, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 0, 0, 1}