Indian Institute of Technology, Delhi
ELL304 Analog Circuits
Laboratory Exercise 1, 23-29 July 2015

All of the following exercises have to be simulated using ngspice.

1. Find the unit step response ($v_2(t)$, when $v_1(t)$ is an unit step) of the circuit shown in Fig. 1.

2. Find the magnitude and phase response of the circuit in Fig. 2. ($V_2(j\omega)$, when $V_1(j\omega)$ is a 1 Volt rms signal.)

3. Simulate the circuit shown in Fig. 3. The switch is to be implemented as described in 3.2.4 of the ngspice manual. (Page 72-75). Simulate for at least 100 clock cycles before you declare the result to be steady state. Plot $v_1(t)$, $i_1(t)$, $v_2(t)$, at steady state, over one period of the clock. Estimate the average DC input resistance of the circuit, R_{in}. (Refer to 15.4.7 of the ngspice manual for average measurements.)

4. In the unit step response of the circuit of Fig. 1, find a way to compute the 0% to 90% rise time of the circuit. (Refer to 15.4.6 of the ngspice manual.) Now sweep the value of the resistor and simulate for different values of the resistor. Plot the rise time as a function of the resistor value. You should refer to the ngspice manual section 17.8.7 for this purpose.

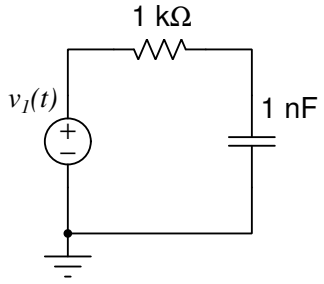

Figure 1

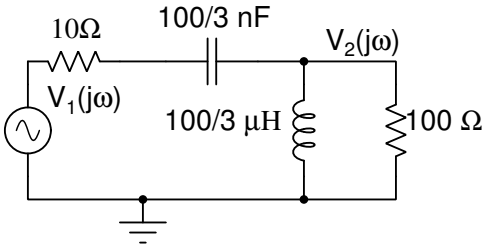

Figure 2

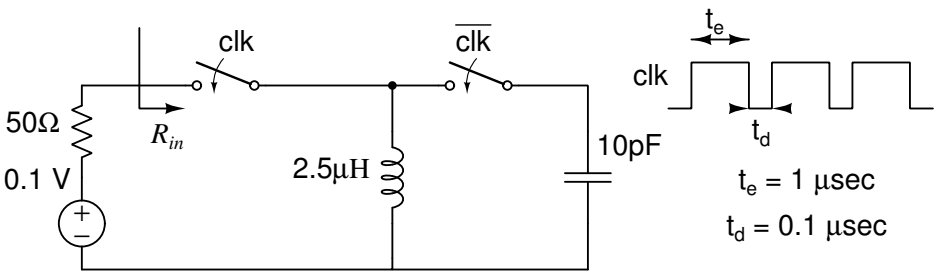

Figure 3