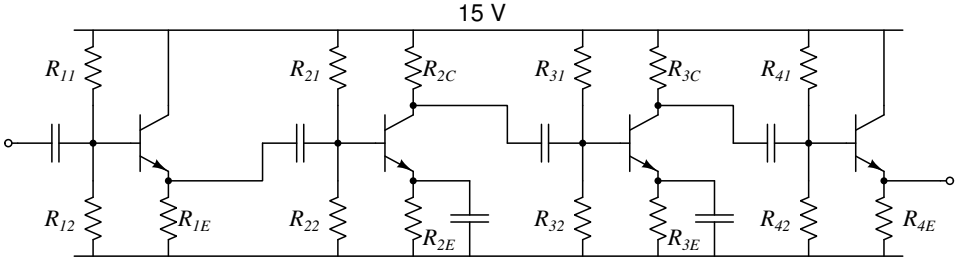
**Indian Institute of Technology, Delhi**
**ELL304 Analog Circuits**
**Laboratory Exercise 3, 12 August 2015**

A multi-stage amplifier has to be designed, as shown in the circuit below, with an input stage (common collector), two gain stages (common emitter), followed by an output stage (common collector).




The following overall specifications are required for the complete multi-stage amplifier.

- Overall mid-frequency gain $\geq 150$.
- Input impedance $\geq 30$ k$\Omega$.
- Output impedance $\leq 15$ $\Omega$.
- Low frequency cut-off of each stage $\leq 100$ Hz.

Proceed in the following steps.

1. Partition the overall required gain into the different stages. Expect a gain of 1 from the common-collector stage.

2. Decide on small signal parameters that you will need, and the operating points of the transistors. As a guideline, a minimum $I_{CQ}$ of 2 mA will be useful. Further, a minimum $V_{CEQ}$ of 7.5 V will help you remain in the active region and get a large swing.

3. Design the common emitter gain stages with the requisite gains. (On paper)

4. Design (on paper) the common collector stages with the requisite input impedance (and/or output impedance).

5. Simulate your design using ngspice. Obtain the gain, the input impedance, the output impedance, and the low frequency cut-offs of each stage.

6. Implement and test the first common emitter stage (stage 2).

7. Implement and test the first common collector stage.
8. Implement and test the last common collector stage.
9. Implement and test a cascade of stages 1, 2, 4.
10. Implement and test the second common emitter stage (stage 3).
11. Implement and test a cascade of stages 1, 3, 4.
12. Finally, implement and test a cascade of stages 1, 2, 3, 4.