Indian Institute of Technology, Delhi
ELL304 Analog Circuits
Some practice problems

1. In the circuits of Fig 1 and Fig 2, all MOS (nMOS and pMOS) devices have a nominal K of 1 mA/V^2, and are proportional to the indicated W/L ratios. C_{gs} of the devices are 200 fF, C_{gd} is 50 fF, C_{db} is 100 fF and C_{sb} is 150 fF. $|V_T|$ of all the devices are 0.5 V.

   (a) Perform a DC operating point analysis and obtain the operating conditions of each device.

   (b) Estimate the small signal parameters (g_m, r_{ds}) of each device. To compute r_{ds}, assume that the intrinsic gain ($g_m r_{ds}$) of each and every device is 50, as long as the device is in its flat region of operation.

   (c) Estimate the DC gain of the circuit. Also estimate the common mode gain of the circuit, and CMRR. (CM gain is output divided by sum of inputs. Differential gain is the output divided by the difference of inputs.)

   (d) Find expressions for the locations of poles and zeros in the circuit.

   (e) What should be the relative locations of the poles for a phase margin of 60°?

   (f) Find the value of C_C for which the circuit will have a phase margin of 60°.

   (g) An extra right-half-plane zero is to be removed. How? Draw the complete circuit diagram, with all values.

   (h) For the value of C_C obtained, find the unity gain bandwidth of the circuit.

2. The (differential mode small signal half) circuits drawn in Fig 3 and Fig 4 need to have a phase margin of 75°, for a unity gain bandwidth of 100 MHz (remember, 1 Hz is 2π radians/second).

   (a) Arrive at approximate expressions for the locations of the two poles, based on circuit parameters.

   (b) What should be the locations of the two poles, given the unity gain bandwidth, and the phase margin specifications?

   (c) What should be the g_m of the first stages of the two circuits?

   (d) What should be the g_m of the second stages of the two circuits?

   (e) Given maximum allowed and minimum allowed W/L ratios of 100 and 1 respectively, arrive at the bias currents required for the first and second stages. Use MOS parameters as in question 1.

   (f) Finish the design and draw the complete differential circuit.

   (g) What is the power consumption of the circuit?

   (h) From your understanding so far, what will happen to the power consumption of the circuit if the required unity gain bandwidth was 200 MHz as opposed to 100 MHz, for the same phase margin?

3. Problems from the book: 13.1, 13.3, 13.8, 13.16, 13.17, 13.19.

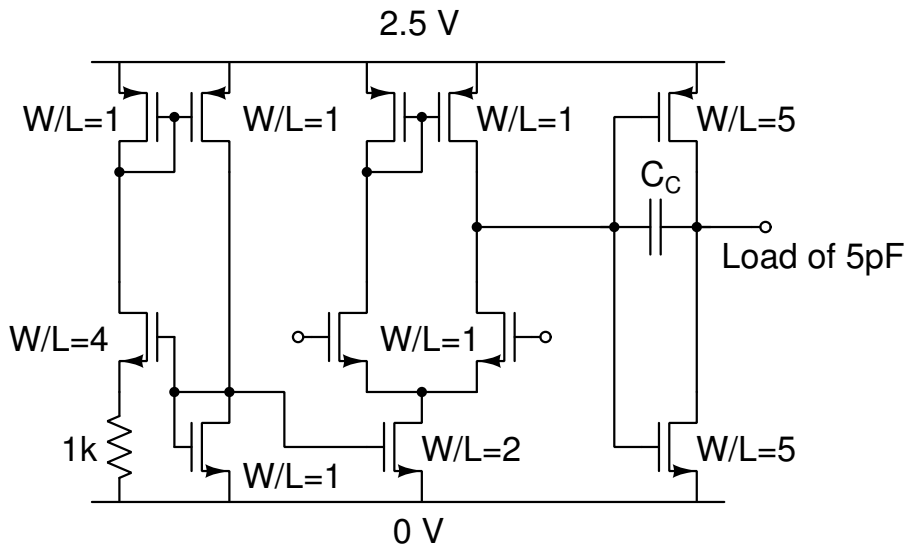

Figure 1

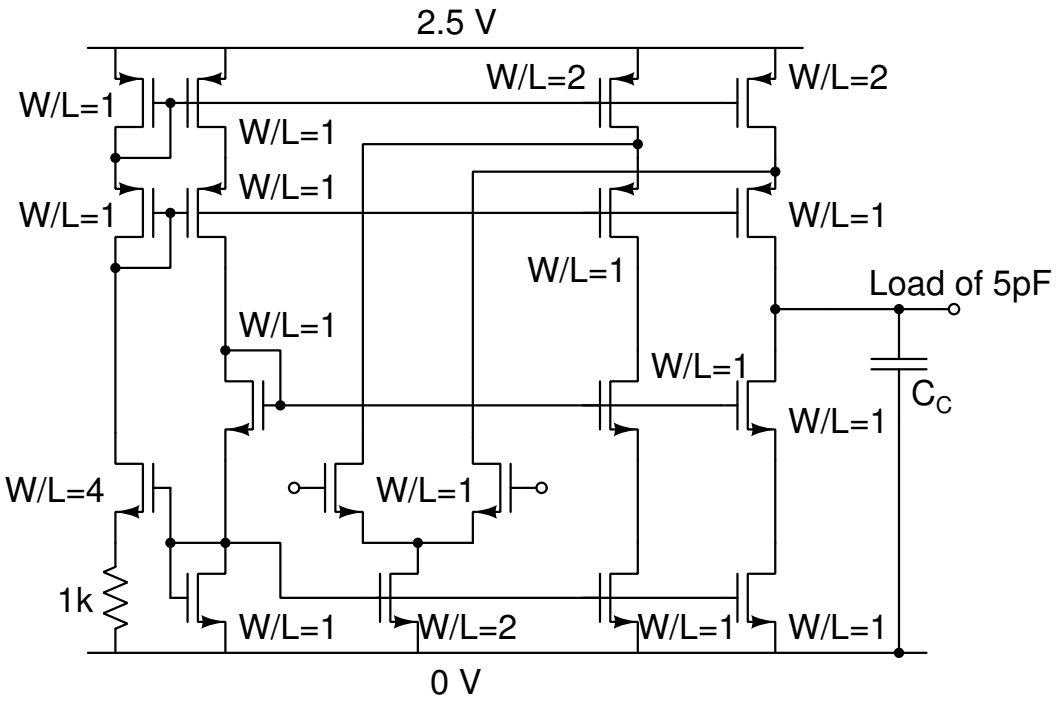

Figure 2

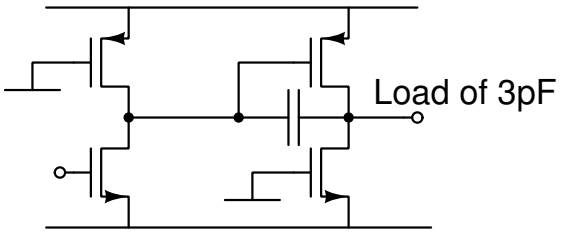

Figure 3

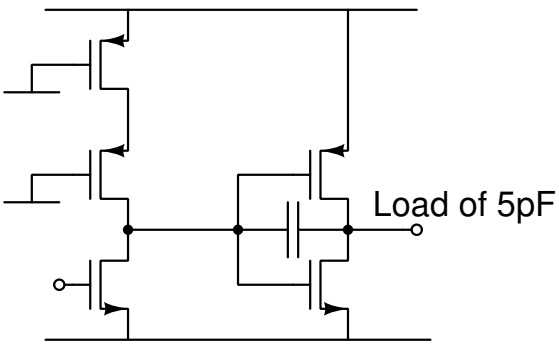

Figure 4