

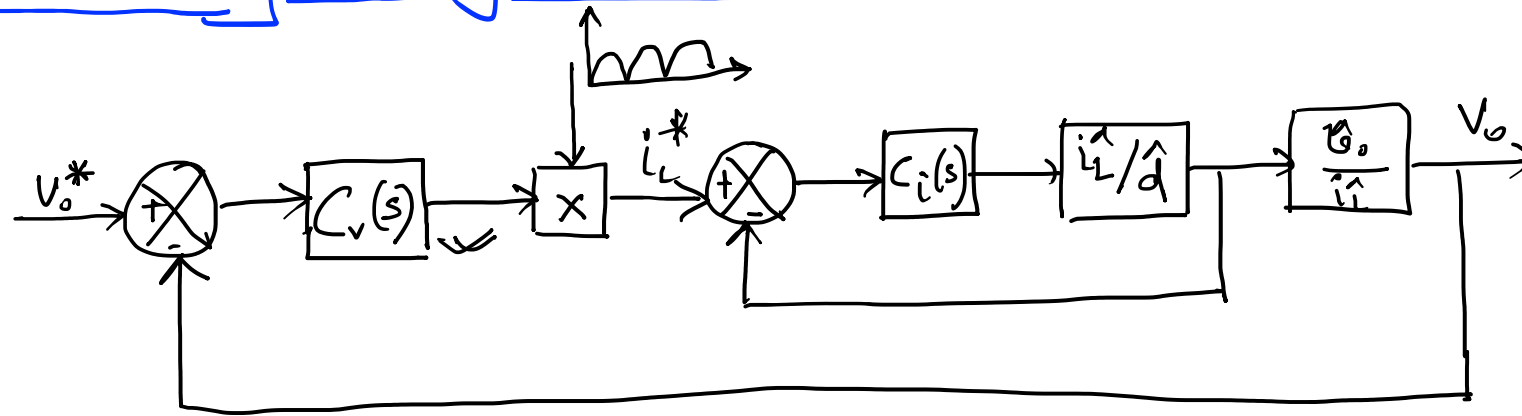
Switched Mode Power Conversion

Semester II Academic Year 2025-26

Lecture 18

17th February 2026

Improving voltage controller bandwidth



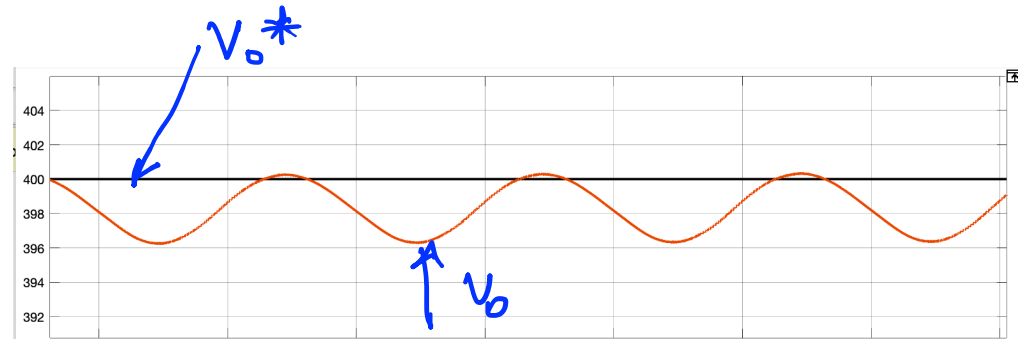
— V_o has double line frequency ripple

— V_o^* is a constant value

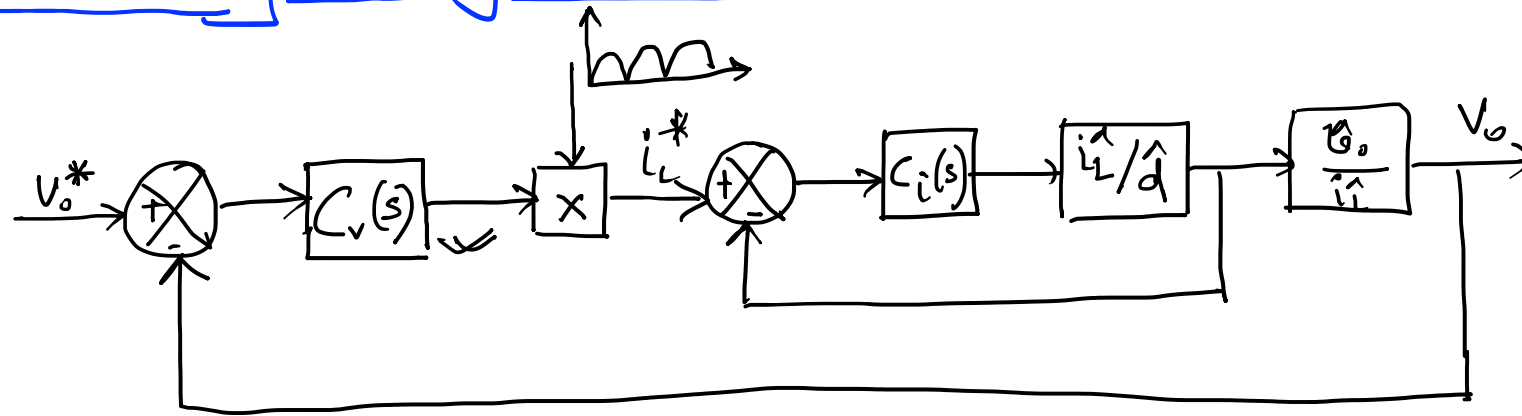
— Thus, voltage error will have double line frequency component

← $C_v(s)$ has to reject this component

← Reduction in bandwidth

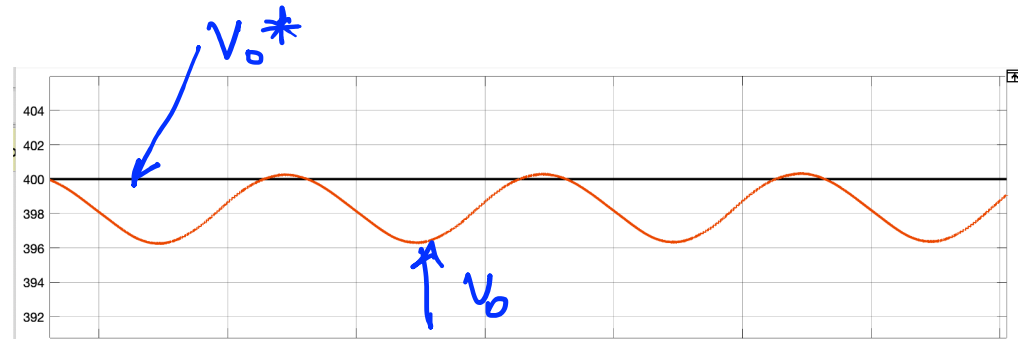


Improving voltage controller bandwidth



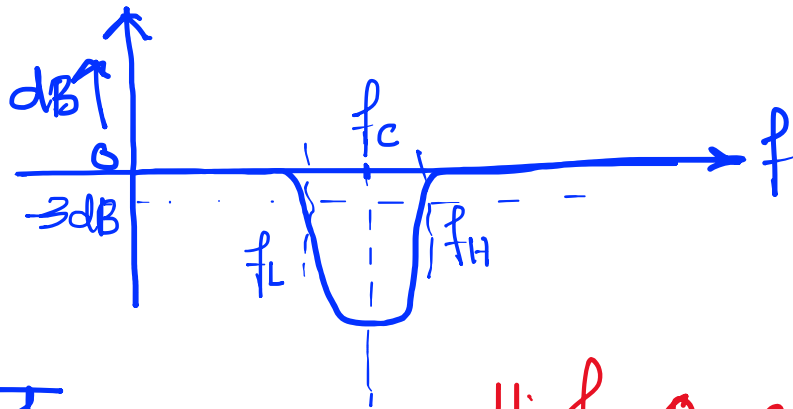
→ what if the double line frequency ripple is rejected from the feedback

[Notch filter at double line frequency in feedback]



Improving voltage controller bandwidth [Notch filter]

→ Gain of notch filter



$$f_c = \sqrt{f_L f_H}$$

$$f_{bw} = f_H - f_L$$

$$\text{Quality factor} = \frac{f_c}{f_{bw}}$$

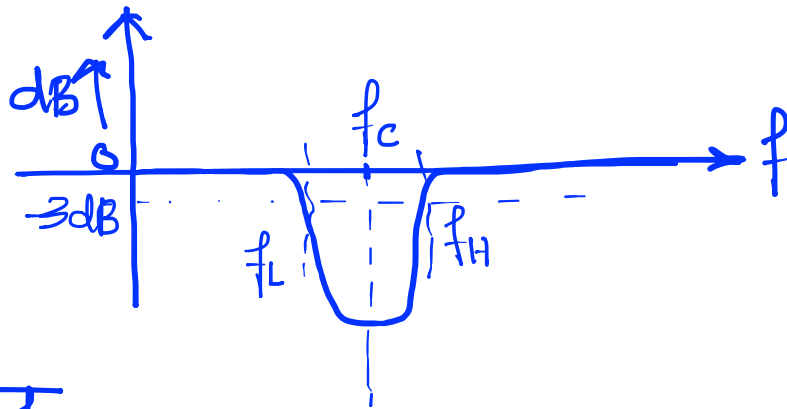
(Q)

High Q notch filter
designed at double line
frequency will attenuate
only the double line
frequency ripple

Improving voltage controller bandwidth [Notch filter]

→ Gain of notch filter

→ Second Order notch filter



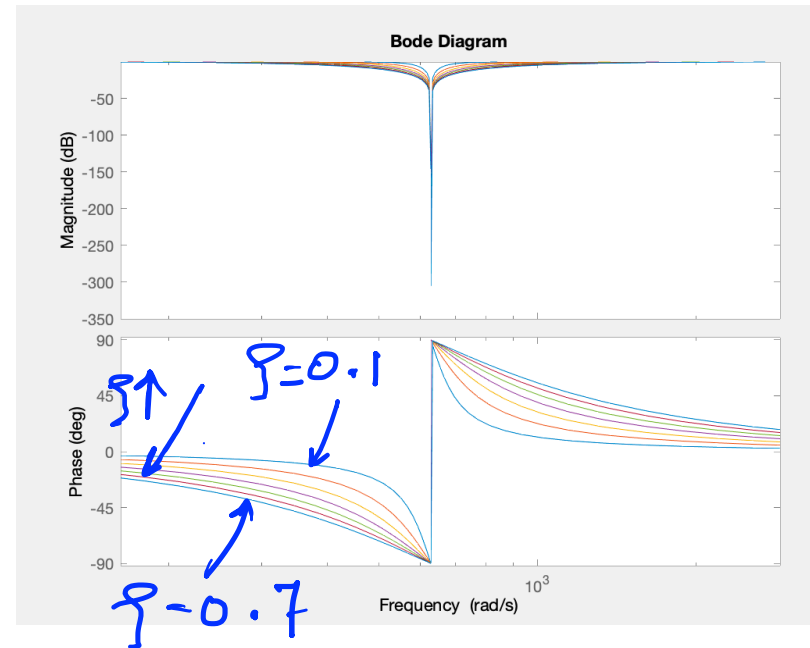
$$\frac{s^2 + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$f_c = \sqrt{f_L f_H}$$

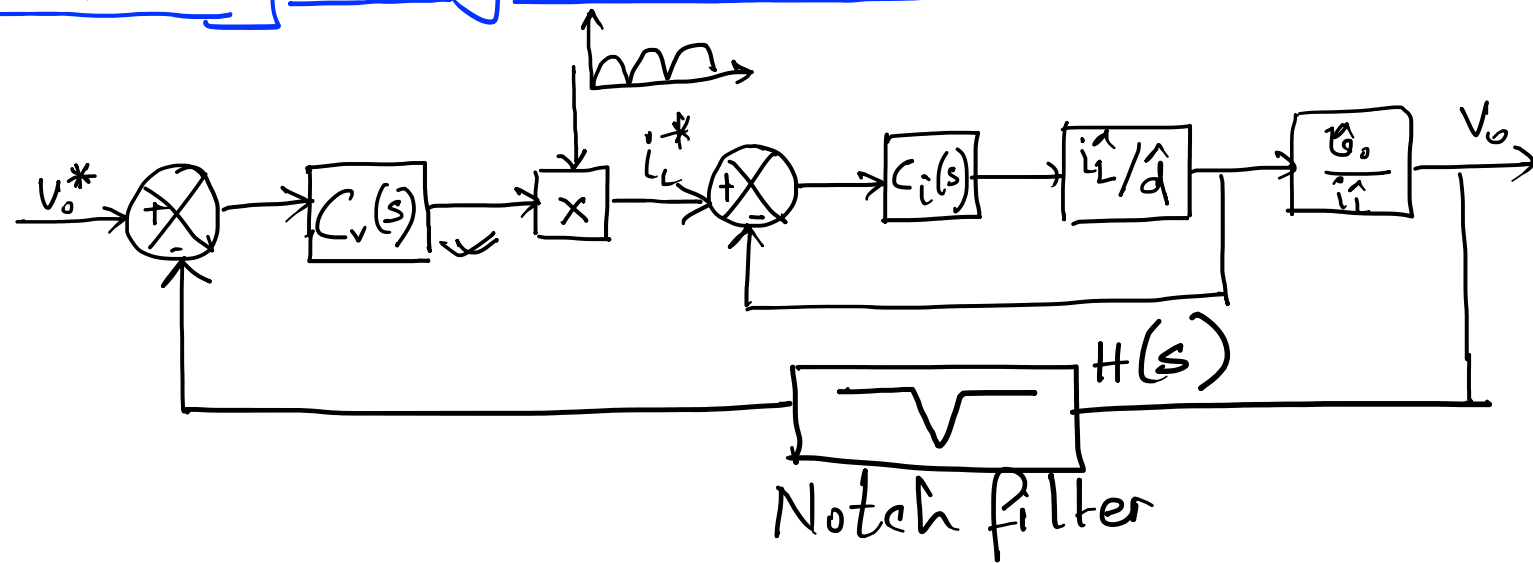
$$f_{bw} = f_H - f_L$$

$$\text{Quality factor} = \frac{f_c}{f_{bw}}$$

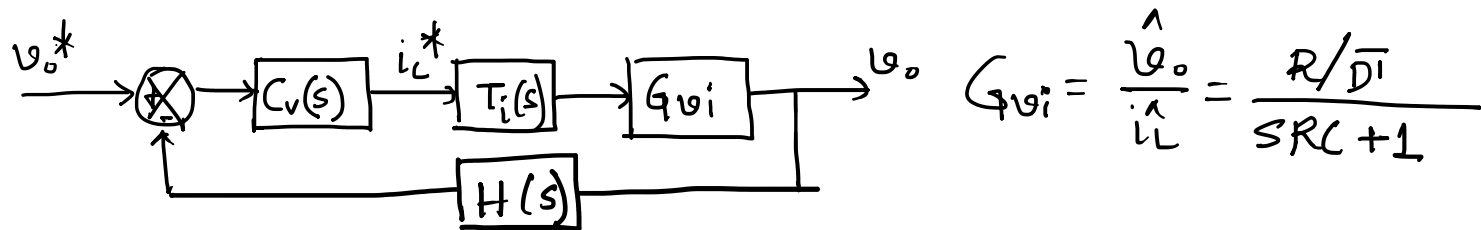
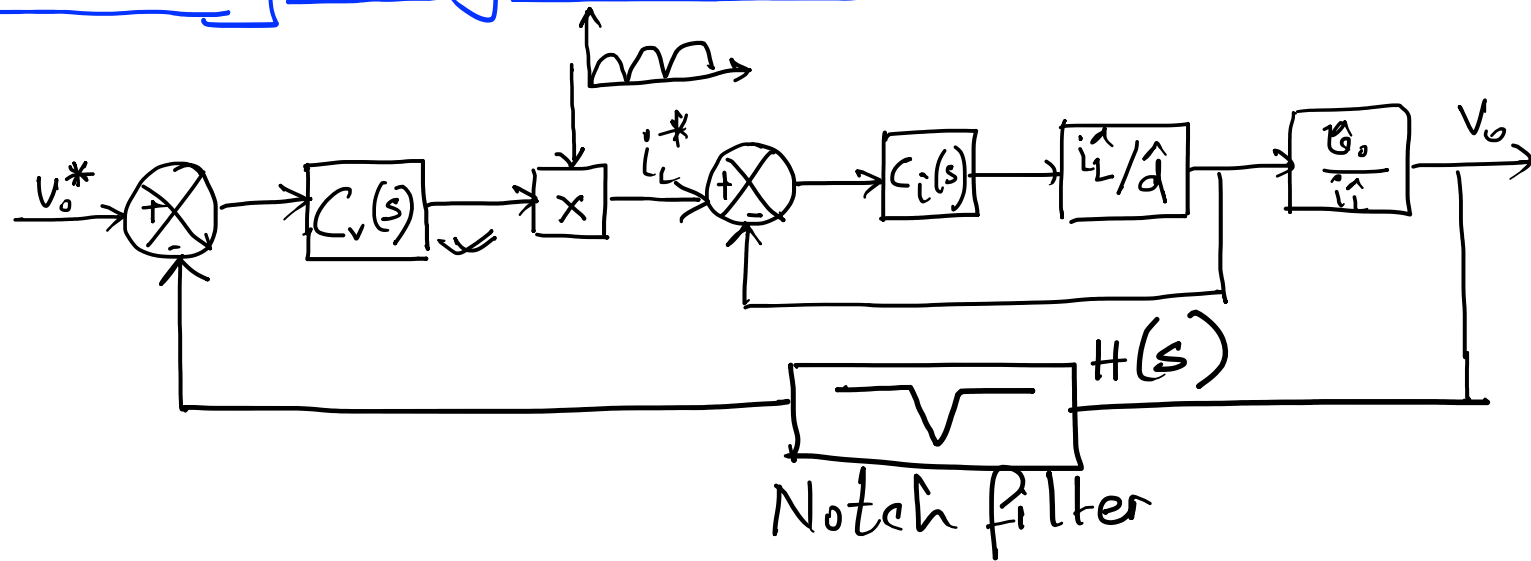
(Q)



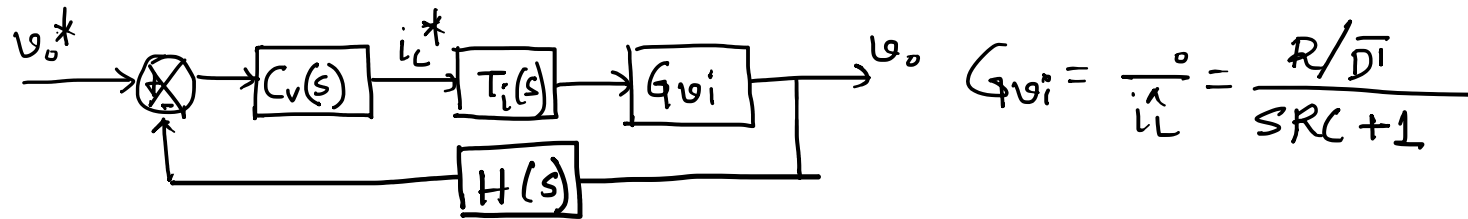
Improving voltage controller bandwidth



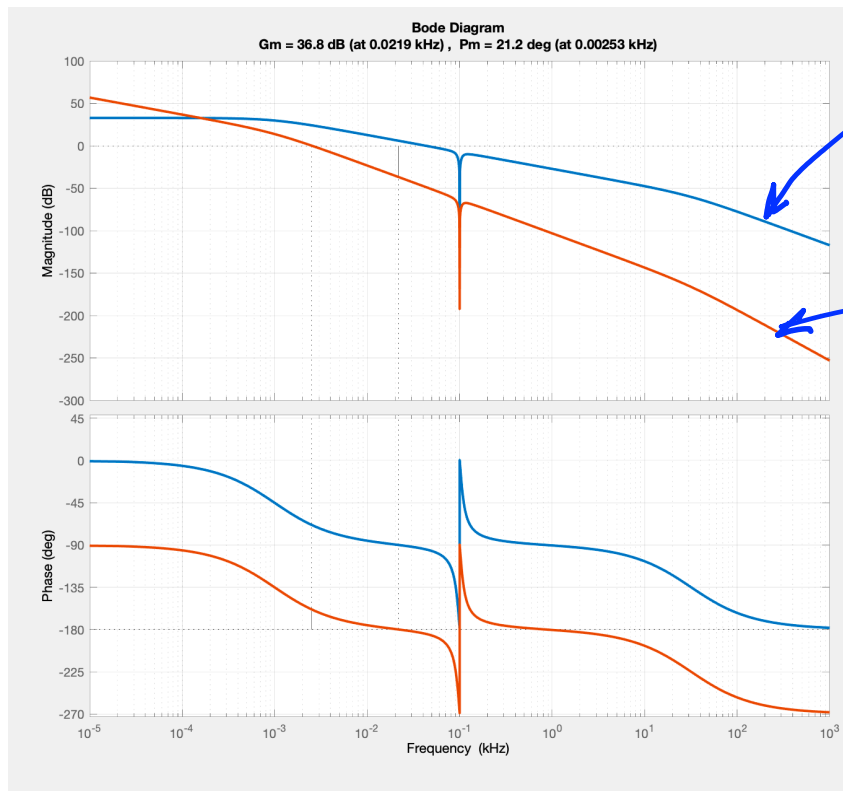
Improving voltage controller bandwidth



Improving voltage controller bandwidth



$$G_{vi} = \frac{v_o}{i_L} = \frac{R/\overline{D}'}{sRC + 1}$$



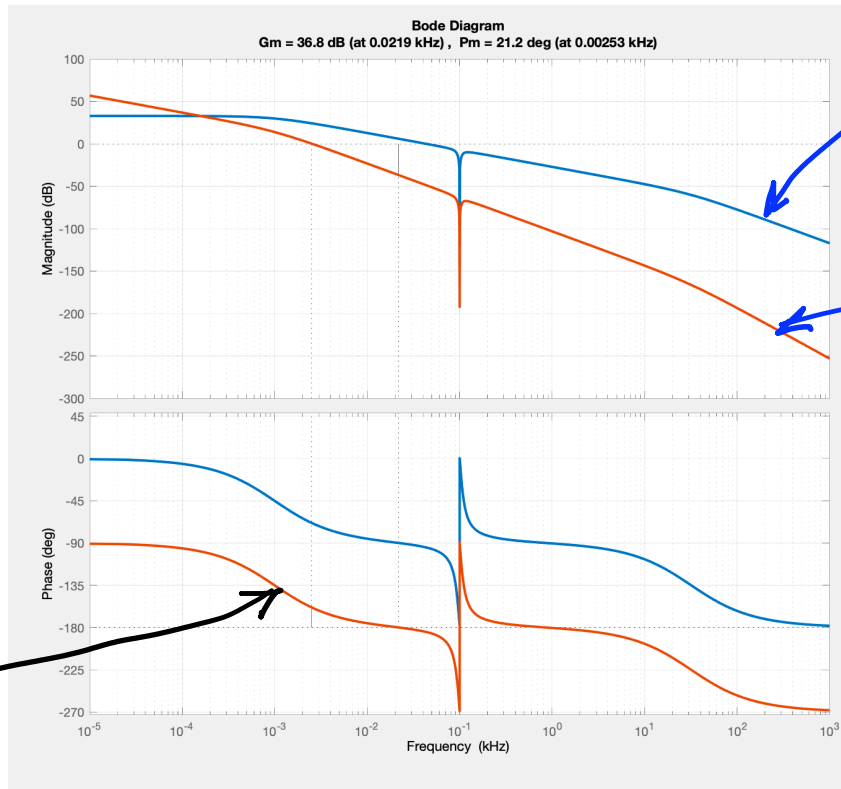
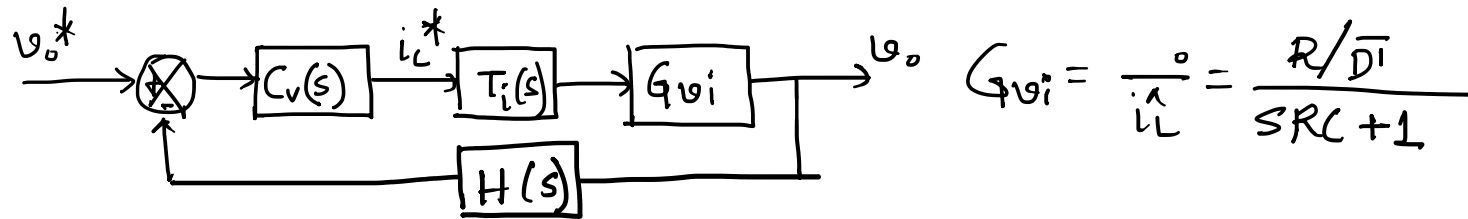
open loop gain
(uncompensated)

Compensated
open loop gain

$$C_v(s) = \frac{1}{s}$$

[Zero steady
state error]

Improving voltage controller bandwidth



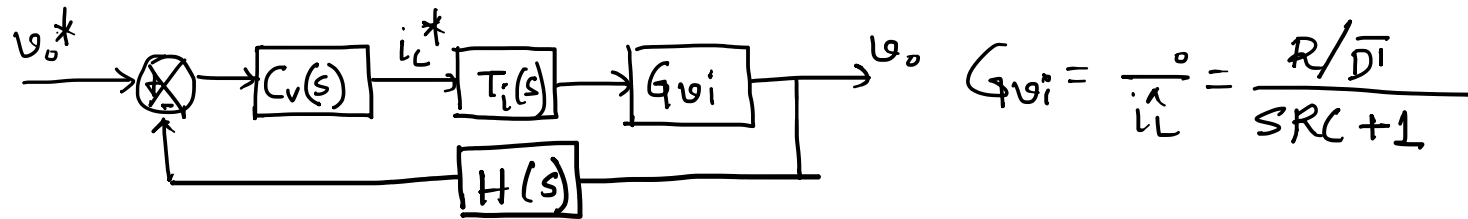
open loop gain
(uncompensated)

Compensated
open loop gain

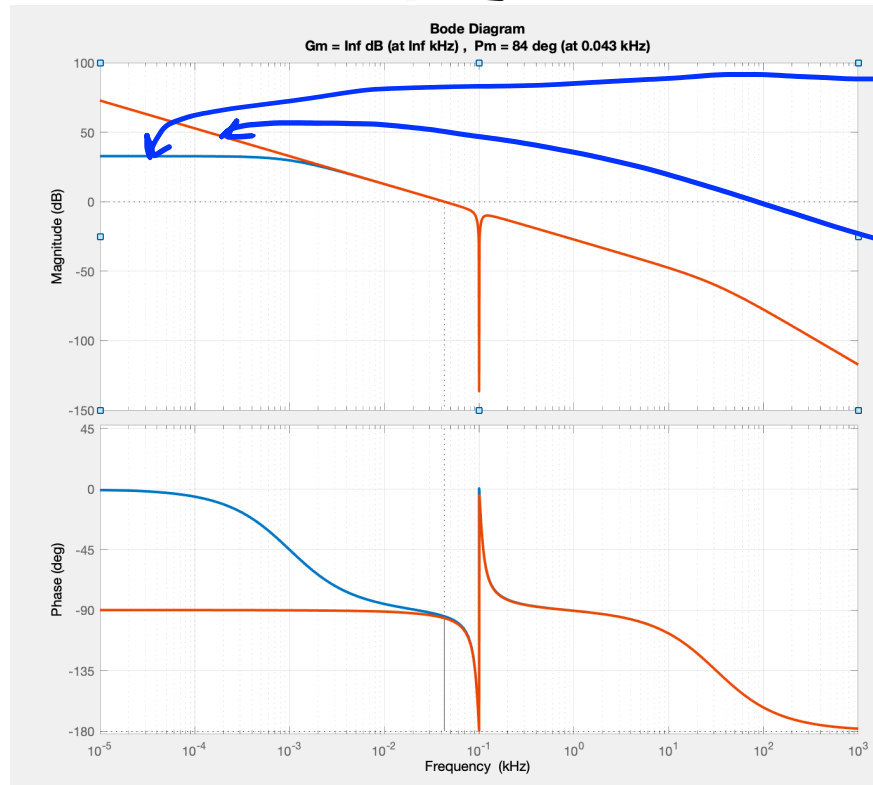
$$C_v(s) = \frac{1}{s}$$

Insert
zero

Improving voltage controller bandwidth



$$G_{vi} = \frac{v_o}{i_L} = \frac{R/\bar{D}^*}{sRC + 1}$$

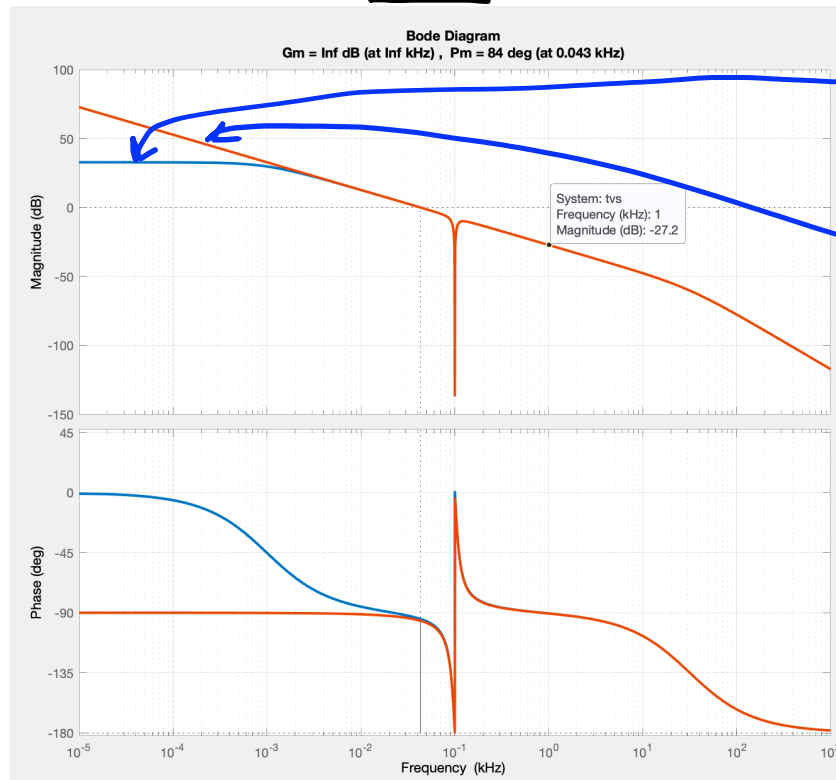
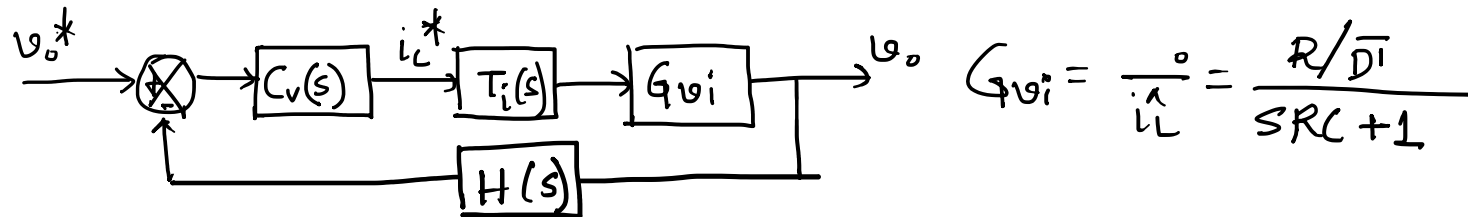


open loop gain
(uncompensated)

Compensated
open loop gain

$$C_v(s) = \frac{s + 6.2832}{s}$$

Improving voltage controller bandwidth



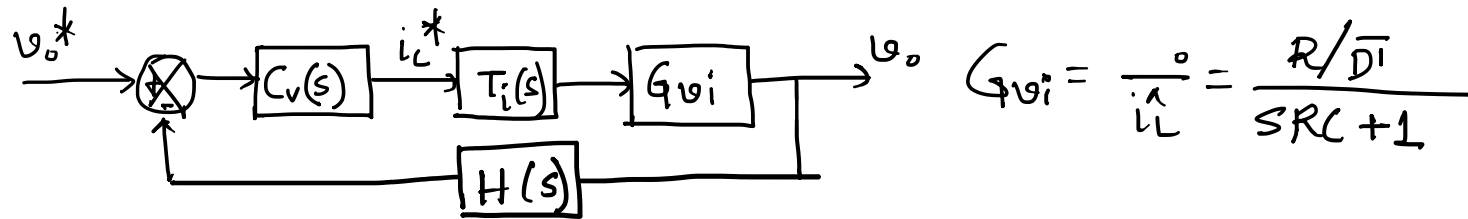
open loop gain
(uncompensated)

Compensated
open loop gain

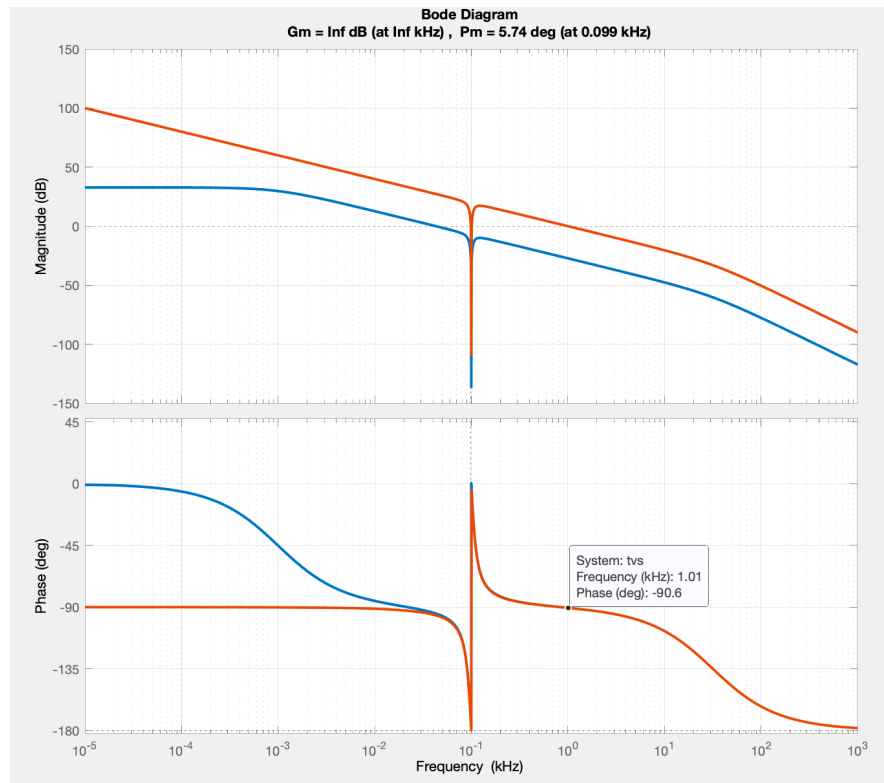
$$C_v(s) = \frac{s + 6.2832}{s}$$

To design the bandwidth at
1 kHz gain to be added?

Improving voltage controller bandwidth



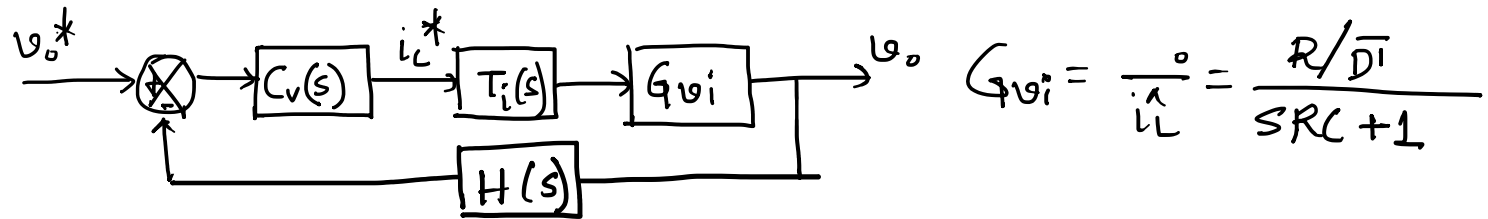
$$G_{vi} = \frac{v_o}{i_L} = \frac{R/\overline{D}^2}{sRC + 1}$$



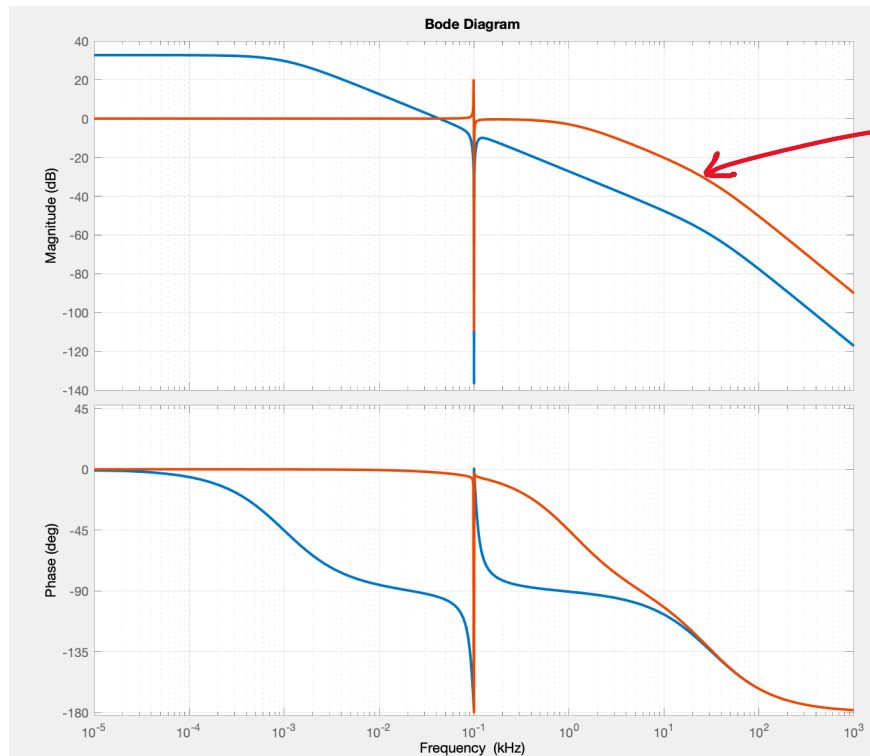
$$C_v = \frac{23(s + 6.28)}{s}$$

Phase margin $\approx 90^\circ$

Improving voltage controller bandwidth



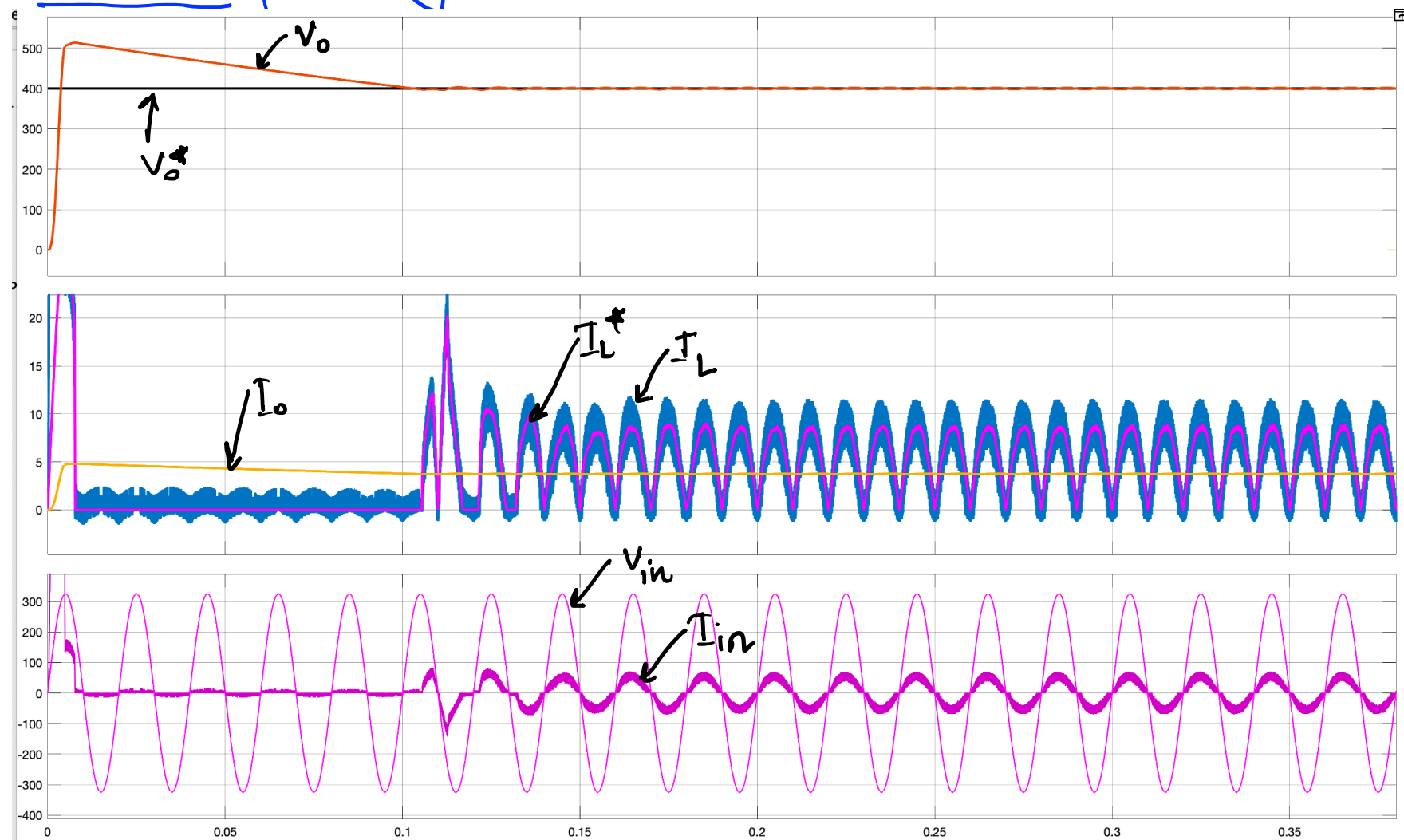
$$G_{vi} = \frac{v_o}{i_L} = \frac{R/\bar{D}^*}{sRC + 1}$$



Closed loop transfer function of the compensated system

$$C_v = \frac{23(s + 6.28)}{s}$$

Improving voltage controller bandwidth



Improving voltage controller bandwidth

